High-efficiency of MHz Inverter Constructed from Frequency Multiplying Circuit

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***Abstract*— This paper discusses a verification of an inverter outputs MHz frequency which is over the switching frequency. The proposed inverter consists of a multi-phase inverter using silicon switching devices and multi-core transformers. By the frequency multiplying, high switching frequency compared with the output frequency is not required. Moreover, the series resonance using a leakage inductance of the multi-core transformers and a resonant capacitor is applied in order to achieve sinusoidal output voltage. A prototype circuit is experimentally verified and theoretically analyzed in terms of zero voltage switching (ZVS). As a result, it is confirmed that the prototype circuit can output sinusoidal output voltage of 2.5 MHz with the switching frequency of 500 kHz. In addition, a required dead time for zero voltage switching is theoretically analyzed and experimentally verified using the prototype circuit.**

I. INTRODUCTION

Recently, high-efficiency high-frequency inverters which output MHz frequency are increasingly received attentions for applications of plasma generators and wireless power transfer [1-3]. For those applications, voltage with MHz band frequency is required.

As one of conventional high frequency inverters, power linear amplifiers using transistors are used. However, the efficiency of the power linear amplifier is low in principle. On the other hand, Class E inverters have been studying because they can achieve very high efficiency due to ZVS and zero-derivative switching (ZDS) [4, 5]. In addition, wide band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) are used recently. As a result, increasing its efficiency is accelerating even though the output frequency is several MHz to several tens of MHz because their switching speed is higher than that of conventional Si devices [6]. In addition, in order to obtain higher efficiency by reducing switching losses, ZVS or zero current switching (ZCS) is applied. However, the output frequency is limited by the switching frequency even though the wide band gap semiconductors are used because their performance is limited.

This paper verifies experimentally the effect of ZVS on the proposed circuit based on the frequency multiplying method [7] by measuring the input power and the output power. The proposed circuit outputs a frequency which is over a switching frequency while other circuit cannot achieve high output frequency which is over the switching frequency. Therefore, not only wide band gap semiconductors are used but also conventional Si devices can be used in the proposed circuit because the switching frequency is lower than the output frequency. This paper is organized as follows; first, the principle of the proposed circuit is described. Then, an operation of the proposed circuit is theoretically analyzed using an equivalent half-bridge circuit in terms of ZVS for high efficiency. Finally, a validity of the condition which achieves ZVS is experimentally verified at series resonant condition by measuring the input power and the output power.

II. PROPOSED CIRCUIT BASED ON FREQUENCY MULTIPLYING METHOD

Figure 1 shows the circuit configuration of the proposed circuit in a five-phase inverter model. The primary side of the multi-core transformer [8] is connected in parallel. A common connection point of the primary side of the transformer is connected to the neutral point of DC link capacitors C_{dc}. On the other hand, the secondary side of the multi-core transformer is connected in series. The resonant capacitor which is used for the series resonance with the leakage inductance of the multi-core transformer is connected to the secondary side of the multi-core transformer. Note that the magnetizing inductance is neglected.

Figure 2 shows the principle the proposed frequency multiplying method. In the five phase voltage-type inverter, each of the voltage phases is shifted by 72 degree and operated with square wave modulation. As a result, the output frequency f_{out} is expressed as following

$$f_{out} = N \times f_{sw} \tag{1}$$

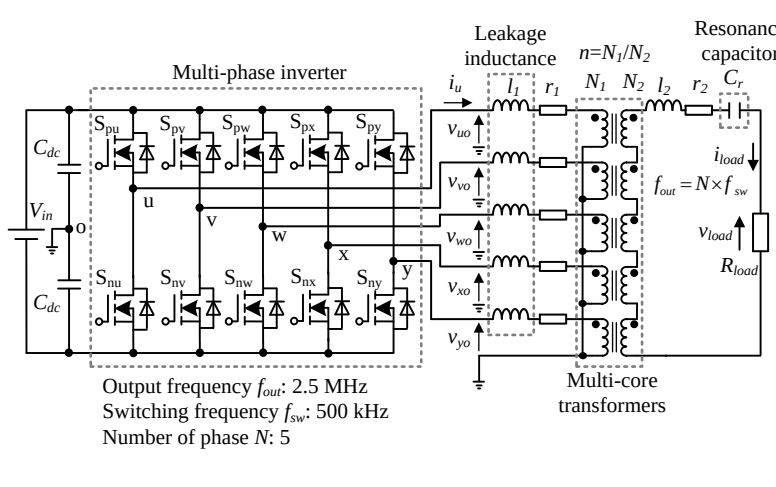


Figure 1. Configuration of proposed circuit.

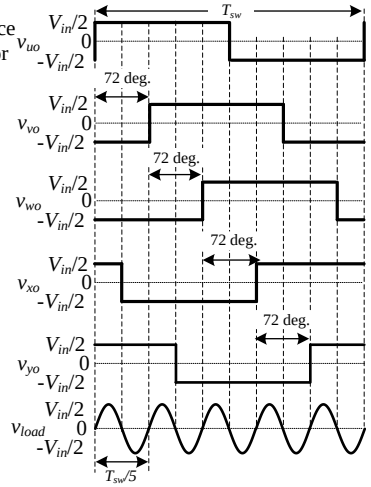


Figure 2. Principle of frequency multiplying.

where f_{sw} is the switching frequency and N is the number of phase in the multi-phase inverter.

Therefore, the multi-phase inverter outputs high frequency which is over the switching frequency even though low switching frequency is applied. In addition, cooling is easier because the heat which is generated from the multi-phase inverter can be dissipated for a number of switches.

III. Principle Of Zero Voltage Switching

This chapter describes the principle of ZVS in the proposed circuit for reduction of the switching loss.

Fig. 3(a) shows a half bridge equivalent circuit of the proposed circuit. In Fig. 3(a), an upper switch is S_1. On the other hand, a lower switch is S_2. A DC link capacitor C_{dc} is assumed to be a voltage source. R is resistance components transformed to the primary side of the multi-core transformer, which includes a wire resistance r_1 and r_2 and a load resistance R_{load}. L is inductance components transformed to the primary side of the multi-core transformer, which includes a leakage inductance l_1 and l_2. C is an equivalent resonant capacitor. Cr is a resonant capacitor connected to the secondary side of the multi-core transformer. By analyzing the operation of the proposed circuit, R, L, C and C_r are expressed by (2), (3), (4) and (5) using the turn ratio of the winding in the multi-core transformer n and the resonant frequency f_r.

$$R = N \times r_1 + n^2 \times \left(R_{out} + r_2\right) \quad (2)$$

$$L = N \times l_1 + n^2 \times l_2 \quad (3)$$

$$C = \frac{1}{\left(2\pi f_r\right)^2 L} \quad (4)$$

$$C_r = \left(\frac{N_1}{N_2}\right)^2 C = n^2 C \quad (5)$$

Fig. 3(b) shows two gate signals of the equivalent circuit with the dead time T_d. In this paper, ZVS when S_2 is turned on is focused.

Fig. 3(c) and (d) show the gate signals, two corresponding drain-source voltage and the current of a neutral point of the DC link voltage when hard-switching occurs or ZVS is achieved.

A. Operation modes

Figure 4 shows operation modes of the proposed circuit. A condition which achieves ZVS is decided by the dead time and circuit parameters. By analyzing Fig. 4, the required dead time T_d which achieves ZVS is obtained as following.

1) Mode I

The Mode I is a period before the dead time starts. In the Mode I, the switch S_1 is on-state and the switch S_2 is off-state. Note that the current I_{Sw} flows to the S_1. In this paper, the period which the Mode I ends is defined as t=0.

2) Mode II

In the Mode II, the S_1 is turned off and the period of the dead time starts. The Mode II is kept until the voltage of parasitic capacitance in S_1 is charged up to the input voltage or the voltage of the parasitic capacitance in S_2 is discharged to zero. Note that the period which the Mode II ends is defined as $t=T_1$. Therefore, T_d should be longer than T_1 because the parasitic capacitance of drain-source is still charged or discharge until $t=T_1$.

3) Mode III

First, note that the period which the Mode III ends is defined as $t=T_2$. The current polarity of the neutral point of the DC link voltage is changed at $t=T_2$. When the dead time T_d is shorter than T_1+T_2, S_2 is turned on while the drain-source voltage of S_2 is zero. Therefore, ZVS is achieved.

4) Mode IV

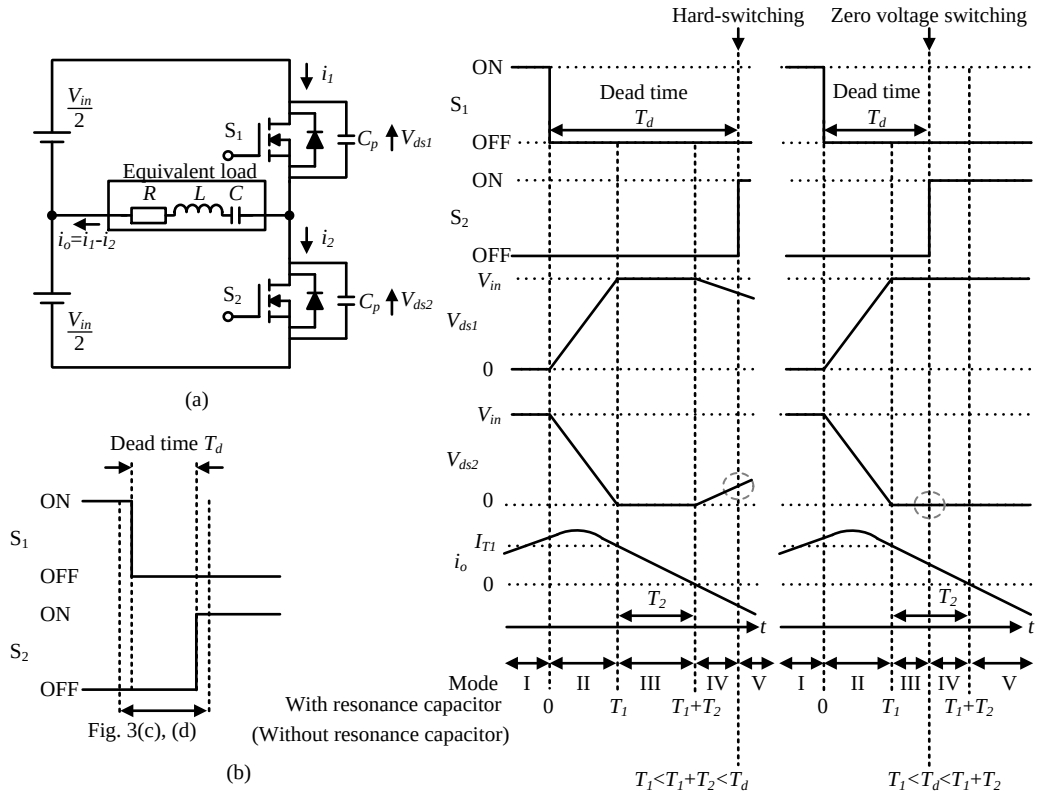
If the dead time T_d is larger than T_1+T_2, the parasitic capacitance of drain-source in S_2 is charged. In this case, S_2 is turned on while the drain-source voltage of S_2 is not zero. Therefore, ZVS is not achieved.

The required dead time which achieves ZVS T_d is expressed by (6) using T_1 and T_2. It is noted that the circuit parameters satisfy (7).

$$T_1 \le T_d \le T_1 + T_2 \tag{6}$$

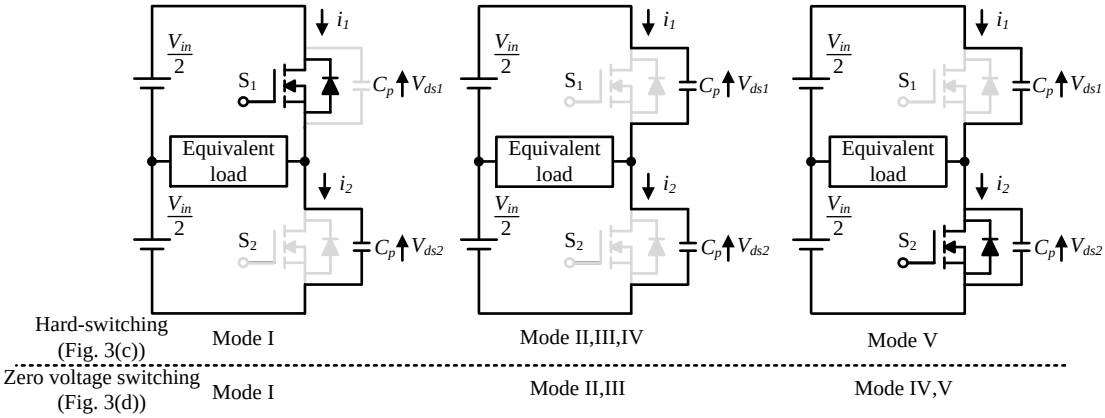
$$C_p R \ll 2\frac{L}{R} \tag{7}$$

$$T_1 = \sqrt{2LC_p}\,Sin^{-1}\frac{4V_{in}}{\left\{\left(\frac{V_{in}}{\sqrt{\frac{L}{C_p}}}\right)^2 \frac{1}{I_{sw}} + 2I_{sw}\right\}\sqrt{2\frac{L}{C_p}}} \tag{8}$$



(a) Half bridge equivalent circuit.
(b) Gate signals with dead-time.
(c) Enlarged waveforms at hard-switching.
(d) Enlarged waveforms at zero voltage switching.

Fig. 3. Principle of zero voltage switching.



(a) S_1:On, S_2:Off. (b) S_1:Off, S_2:Off (During dead time) (c) S_1:Off, S_2:On

Fig. 4. Operation modes of the proposed circuit.

$$T_2 = \frac{1}{\omega} Tan^{-1}\left(-\frac{\omega}{K}\right) \quad (9)$$

$$\omega = \sqrt{\frac{1}{2LC} - \left(\frac{R}{2L}\right)^2} \quad (10)$$

$$K = \frac{\frac{V_{in}}{2} - V_c(T_1)}{LI_{T1}} - \frac{R}{2L} \quad (11)$$

where T_1 is the period which the Mode II ends, T_2 is the period of the Mode III. In other words, At T_2, the current polarity of equivalent load is changed. ω is the natural angular frequency, K is the coefficient, I_{T1} is the current of the equivalent load at t=T_1, $V_c(T_1)$ is the voltage of the equivalent resonant capacitor at t=T_1.

IV. Experimental Results

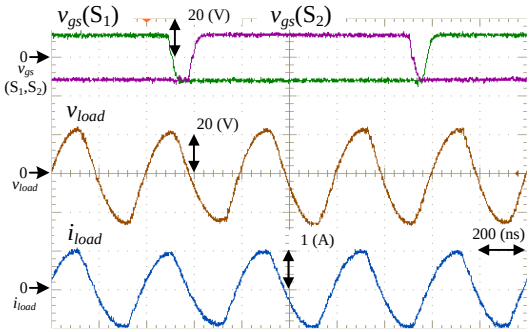
Specifications of a prototype circuit is as following. The number of phase in the multi-phase inverter N is five. In order to obtain the output frequency f_{out} of 2.5 MHz, the switching frequency f_{sw} is 500 kHz. The input voltage V_{in} is 48 V. A load resistance is 33.3 Ω which is a non-inductive resistance.

A. Operation waveforms

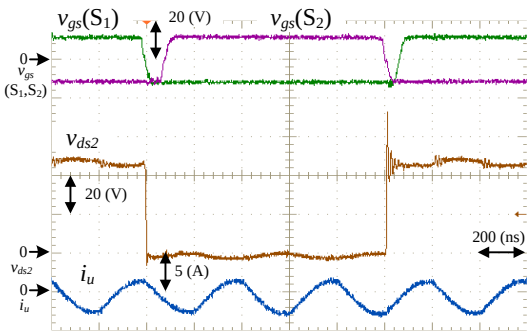
Figure 5 shows the experimental waveforms at ZVS condition. The dead time T_d = 97.1 ns which satisfies (6) is used. From Fig. 5(a), it is confirmed that the load voltage is almost sinusoidal waveform due to the series resonance.

Fig. 5(b) and (c) show two gate signals, the drain-source voltage of S2 and the primary current of the multi-core transformer. From the result, there is no rise of v_{ds2} during the dead time because the dead time which satisfies (6) is used.

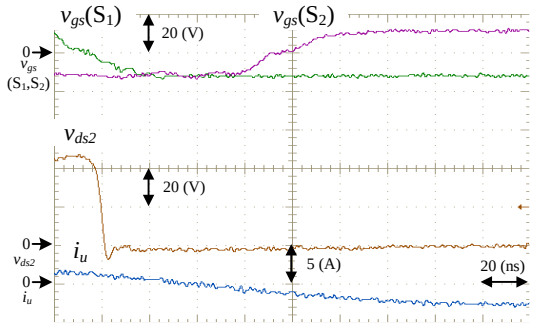
Figure 6 shows the experimental waveforms at hard-



(a) Load voltage and load current.

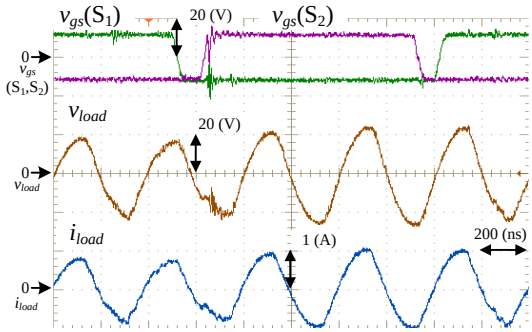


(b) drain-source voltage and primary current of multi-core transformer.

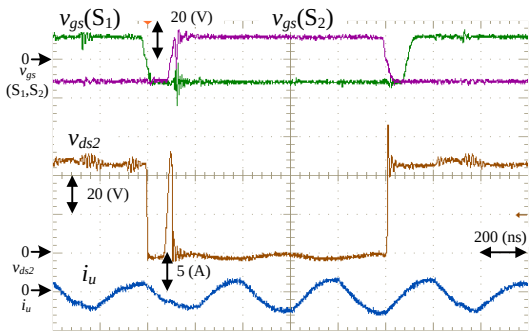


(c) Enlarged waveforms of (b)

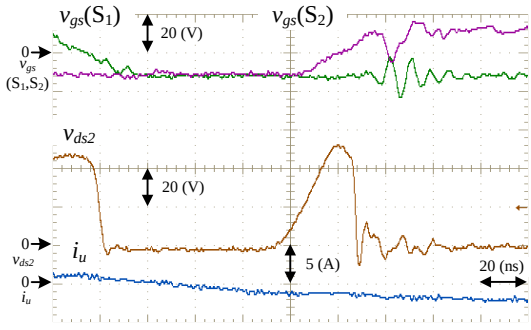
Figure 5. Experimental waveforms at ZVS (T_d=97.1 ns).



(a) Load voltage and load current.



(b) drain-source voltage and primary current of multi-core transformer.



(c) Enlarged waveforms of (b)

Figure 6. Experimental waveforms at hard-switching (T_d=117.6 ns).

switching condition which does not satisfy (6). In Fig. 6, the dead time T_d = 117.6 ns. Therefore, hard-switching occurs because v_{ds2} is increased during the dead time.

From these experiments, the proposed circuit obtains high efficiency because zero voltage switching is achieved even though the output frequency is 2.5 MHz.

B. Input and output power measurement

Figure 7 shows the measured input and output power of the prototype circuit at low power when the dead time varies. It is noted that the load resistance is constant. The input and output power are the highest at ZVS condition because the switching loss is the lowest and dead time is the shortest. On the other hand, at hard-switching condition, the input power is decreased with the increasing dead time. In addition, the output power is decreased because the switching loss becomes higher.

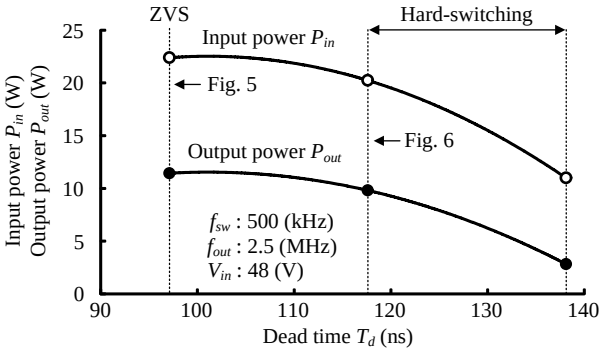


Figure 7. Input power and output power.

V. CONCLUSION

This paper described the high-frequency inverter which outputs MHz frequency based on the multiplying frequency method. By the frequency multiplying, the proposed circuit outputs high frequency which is over the switching frequency. First, the required dead time which achieves ZVS was derived by using the equivalent circuit. Finally, the prototype circuit was experimentally verified. It was confirmed the prototype circuit can output 2.5 MHz with the switching frequency of 500 kHz at ZVS condition.

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