Revelation of Soft-Switching Operation for Isolated DC to Single-phase AC Converter with Power Decoupling

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***Abstract*— This paper discuses soft-switching range in an isolated single-phase matrix converter with a center-tapped transformer for HVDC (high voltage direct current) power feeding systems. The proposed converter consist of a full bridge inverter, a high frequency transformer and a matrix converter which it does not require a bulky electrolytic capacitor. The power decoupling operation is accomplished by the center-tapped transformer and a small LC buffer. In comparison with a conventional DC to single-phase AC converter without power decoupling operation, the proposed circuit partly achieve the Zero Voltage Switching (ZVS) operation of the full bridge inverter on the primary side of the transformer. In this paper, a principle of ZVS using the LC buffer circuit is described. From a simulation result, the soft-switching operation is confirmed at low load current region by using the LC buffer. Meanwhile it is experimentally confirmed that the proposed power decoupling method reduces the DC bus current ripple by 85.1%. In addition, the ZVS operation on the primary side of the proposed DC to single-phase AC converter is confirmed in experiment.**

Keywords—matrix converter; power decoupling; Zero voltage switching;

I. INTRODUCTION

Recently, power consumption of ICT (information and communication technology) equipment in buildings and factories has been drastically increased. As a solution for energy saving, a High Voltage Direct Current (HVDC) power feeding system has been developed previously [1-2]. In the HVDC power feeding system, a DC bus of 380 V is applied in order to obtain high efficiency and low cost due to the reduction of converters and cables, compared to conventional AC or DC 48 V power feeding system. A DC to single-phase AC converter is required because the HVDC power feeding system is considered to not be able to replace entirely the conventional AC power feeding system in the near future. In addition, the DC to single-phase AC converter requires isolation capability between the DC bus and the AC output side for safety.

One of the most significant problems, a power ripple which is generated by a single-phase load becomes a twice of a commercial frequency. In past works, some circuit topologies with power decoupling capability have been studied [3-5]. However, these circuits restrict the down-sizing because the circuits employ not only passive components but also additional switching devices for the power decoupling. In order to overcome this problem, the authors have already proposed the power decoupling method for the isolated DC to single-phase AC converter in [6-7]. The proposed system consists of a full bridge inverter, a center- tapped transformer, a small LC buffer and a matrix converter. The proposed converter does not require extra switching devices for the power decoupling. In addition, smaller size compared to the conventional system is also expected because the bulky electrolytic capacitor is not required.

The modulation method of the matrix converter used in [7] is applied with PDM (Pulse Density Modulation)which is ZVS (Zero Voltage Switching) is achieved by synchronization of the gate pulses of the matrix converter with zero voltage term of the secondary voltage of the transformer. Therefore, the PDM can drastically reduce the switching loss in the secondary side. However, in order to achieve higher efficiency, the switching loss in the primary side is also necessary to be reduced in the proposed converter.

This paper discusses the achievement of the ZVS condition at the primary side of the isolated DC to single-phase AC converter using matrix converter. The primary converter can partly achieve ZVS even when a differential current which delivers the power to the secondary side of transformer is below the lower limit value. Moreover, when the matrix converter output voltage is zero, the proposed converter can partly achieve ZVS. These reason is that there is the constant common current of the buffer circuit is overlapping to the transformer current.

This paper is organized as follows; first, the circuit configuration of the proposed DC to single-phase AC converter and the principle of the power decoupling are described; second, the ZVS condition at the primary inverter are method; finally, the fundamental operation waveforms of the proposed system when the ZVS condition is achieved at the primary side is evaluated by simulations and experiments.

II. CIRCUIT TOPOLOGY

Fig. 1 shows a conventional isolated DC to single-phase AC converter. The conventional circuit comprises a full bridge inverter, a high frequency transformer and a rectifier-inverter system. The full bridge inverter outputs square voltage at high frequency in order to reduce the transformer volume. The secondary rectifier converts the high frequency voltage to DC voltage and the PWM inverter controls the output filter capacitor voltage by feedback control. When the load current is sinusoidal waveform and achieves the unity power factor, the instantaneous output power p_{out} is expressed by (1).

$$\begin{aligned} p_{out} &= \sqrt{2}V_{load}\sin(\omega_o t)\cdot\sqrt{2}I_{load}\sin(\omega_o t) \\ &= V_{load}I_{load}\{1-\cos(2\omega_o t)\} = P_{out}\{1-\cos(2\omega_o t)\} \end{aligned} \quad (1)$$

where, V_{load} is the load voltage (RMS), I_{load} is the load current (RMS), P_{out} is the output mean power and ω_o is the output angular frequency. A ripple component shown in the second term of (1) should be bypassed in order to obtain a constant DC current in the DC bus. Hence, this system has to adopt a bulky electrolytic capacitor C_{dc} to absorb the power ripple.

Fig. 2 shows the isolated DC to single-phase AC converter using a matrix converter and a small LC buffer which is proposed in this paper. The matrix converter is employed as a secondary converter in order to eliminate the DC-link capacitor which is used in Fig. 1. In addition, a center-tapped transformer links the full bridge inverter to the matrix converter for isolation and the power decoupling which results in reducing the DC bus current ripple. A buffer circuit including a buffer capacitor C_{buf} and a buffer inductor L_{buf} is used to absorb the power ripple. It should be noted that a charge and a discharge to compensate the power ripple is implemented at C_{buf}.

Fig. 3 shows the principle of the power decoupling with C_{buf}. In order to yield the DC bus current without the ripple, the relationship among the output power p_{out}, a DC bus power p_{bus} and the charged power p_{buf} is defined as (2).

$$p_{buf} = P_{out}\cos(2\omega_o t) \quad (2)$$

where, the polarity of p_{buf} is defined as positive when C_{buf} is charged. It should be noted that the capacitance of the buffer capacitor is smaller than one in the conventional converter because the power ripple is compensated by varying the buffer capacitor voltage v_{Cbuf} not by the large capacitance. On the other hand, the inductor in the buffer circuit is used for the current control in the power decoupling, which is equivalent to control of p_{buf}. The buffer current control is carried out by the full bridge inverter. The full bridge inverter can outputs independently a differential mode voltage to excite the transformer and a common mode voltage to compensate the power ripple with the LC buffer, owing to the center-tapped transformer. Therefore, the proposed converter does not require additional switching devices for the power decoupling and number of devices in the proposed converter is as same as one of the conventional circuit.

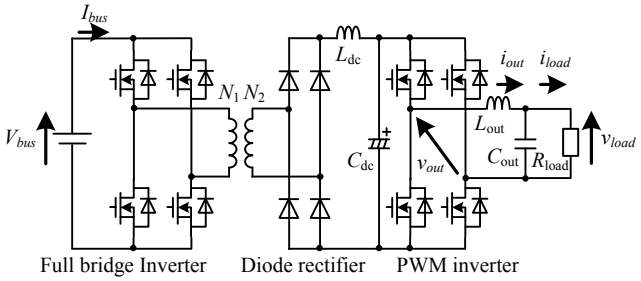


Fig. 1. A Conventional isolated DC to single-phase AC converter. The conventional converter uses a bulky electrolytic capacitor C_{dc} to absorb a power ripple caused by single-phase load.

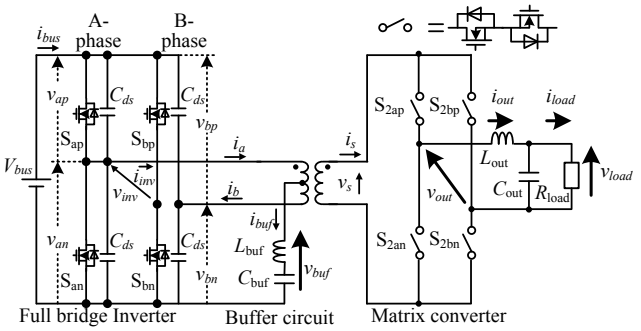


Fig. 2. A Proposed isolated DC to single-phase AC converter. The secondary converter is replaced with a matrix converter in order to eliminate a DC-link smoothing capacitor. In addition, a center-tapped transformer and a small LC buffer are employed to achieve a power decoupling without additional switching devices.

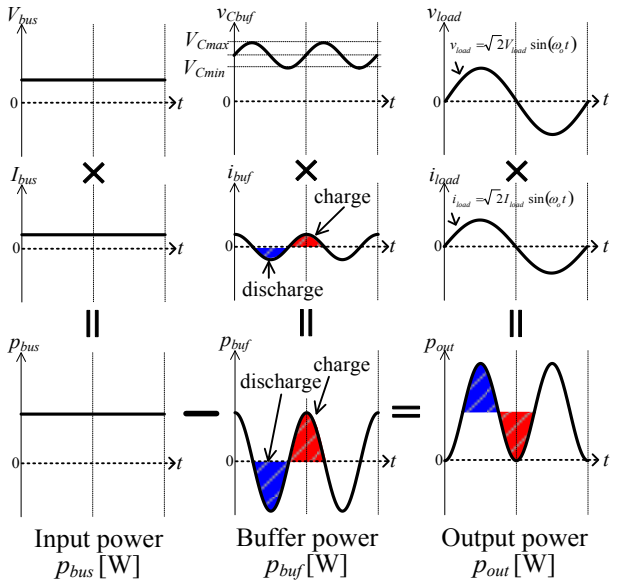


Fig. 3. A principle of the power decoupling with the buffer capacitor. A buffer power to compensate the power ripple is charged or discharged at C_{buf}. As a result, the DC bus current without the ripple component is obtained.

III. CONTROL STRATEGY

A. Full Bridge Inverter

Fig. 4 shows the modulation method of the full bridge inverter. As mentioned above, the full bridge inverter outputs a

differential mode voltage v_{dif} to excite the transformer and a common mode voltage v_{com} to compensate the power ripple. Therefore, a differential mode voltage reference v_{dif}* and a common mode voltage reference v_{com}* are set as input parameters in Fig. 4. It should be noted that the gain of 0.5 is inserted to only the path of v_{dif}* because the reference potential of v_{dif}* is different from one of v_{com}*. In order to obtain the maximum secondary voltage of the transformer, v_{dif}* is set to 1 p.u.. On the other hand, v_{com}* is calculated by a PI controller in the buffer current control to compensate the power ripple as mentioned in chapter IV

Fig. 5 shows the operation modes of the full bridge inverter. The hatched gray line indicates the turned off switch and the black solid line shows the current pathway. Fig. 5 (a) and (b) illustrate the differential mode when the DC bus power is transferred. In this mode, the transformer is excited. In addition, the buffer circuit voltage, which is equivalent to v_{com}, is constant at $V_{bat}/2$. On the other hand, Fig. 5 (c) and (d) show the common mode to control the buffer current i_{buf} in order to compensate the power ripple. In the common mode, the transformer is not excited because v_{dif} becomes zero. By this method, the full bridge inverter can control v_{dif} and v_{com} independently because only one of the differential mode v_{dif} and the common mode v_{com} is varied at one time. This results in that the proposed converter does not require additional switches for the power decoupling.

B. Power Decoupling Method

In order to absorb the power ripple caused by the single-phase load, the buffer current reference i_{buf}^* is calculated from p_{out}^* and the chargeable energy of C_{buf}. First of all, the buffer capacitor energy W_{Cbuf} is presented by (3).

$$W_{Cbuf} = \int_{t_0}^{t} p_{buf} d\tau = \int_{t_0}^{t} P_{out} \cos(2\omega_o \tau) d\tau \tag{3}$$

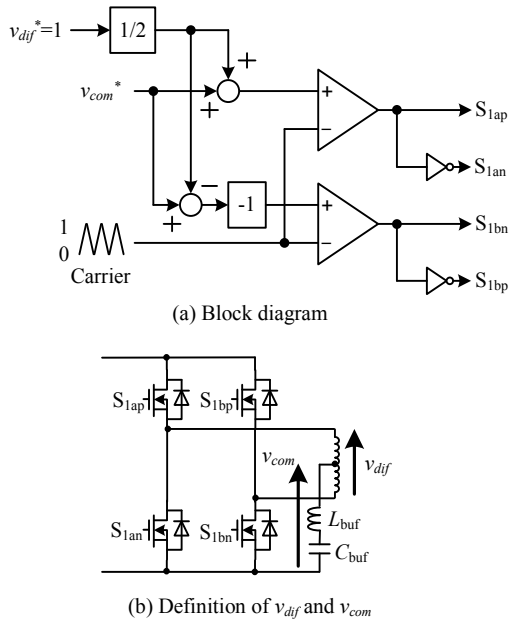
where, t_0 is the start time of operation. If t_0 is zero, v_{Cbuf} which need to compensate the power ripple is calculated as following by using (3).

$$v_{Cbuf} = \sqrt{\frac{V_{bus}^{\ 2}}{4} + \frac{P_{out}}{\omega_o C_{buf}} \sin(2\omega_o t)} \tag{4}$$

where, V_{C0} is the initial voltage of C_{buf} and V_{C0} is $V_{bus}/2$. Finally, i_{buf}^* is derived by using the output power reference P_{out}^*.

$$i_{buf}^{\ *} = C_{buf} \frac{dv_{Cbuf}^{\ *}}{dt} = \frac{P_{out}^{\ *} \cos(2\omega_0 t)}{\sqrt{\frac{V_{bus}^{\ 2}}{4} + \frac{P_{out}^{\ *}}{\omega_o C_{buf}} \sin(2\omega_o t)}} \tag{5}$$

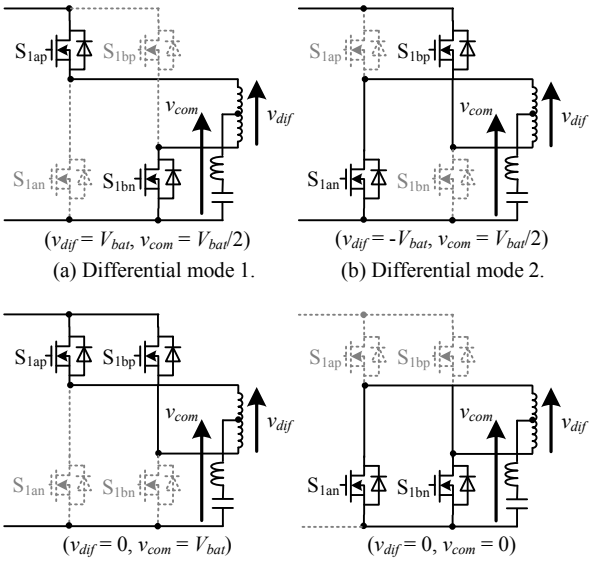
It should be noted that P_{out}^* is calculated by a load resistance. Therefore, the power ripple is compensated by using the buffer current control with the current reference i_{buf}^* as shown (5).



(a) Block diagram

(b) Definition of v_{dif} and v_{com}

Fig. 4. A modulation method of a full bridge inverter. A differential mode voltage reference v_{dif}^* excites the transformer and a common mode voltage reference v_{com}^* is used to compensate the power ripple with the LC buffer.



($v_{dif} = V_{bat}$, $v_{com} = V_{bat}/2$)
(a) Differential mode 1.

($v_{dif} = -V_{bat}$, $v_{com} = V_{bat}/2$)
(b) Differential mode 2.

($v_{dif} = 0$, $v_{com} = V_{bat}$)
(c) Common mode 1.

($v_{dif} = 0$, $v_{com} = 0$)
(d) Common mode 2.

Fig. 5. Operation modes of the full bridge inverter at the primary side. The primary side of the proposed system has two mode; a differencial mode which delivers the power to the secondary side of transformer and a common mode which reduce the the power ripple.

C. Matrix Converter

The matrix converter used as a secondary converter in the proposed system is applied with the PDM of [7]. The PDM is suitable for the direct AC to AC converter which provides a sinusoidal voltage at commercial frequency from a high frequency voltage, such as the proposed system. The PDM treats the high-frequency input voltage as pulses and synthesize the output voltage with a density of the input voltage pulses. A half cycle of the input voltage pulses are used as the minimum unit

of the output voltage waveform. The matrix converter switches are turned on in zero voltage period of the input voltage waveform. In consequence, the matrix converter achieves ZVS (zero voltage switching) which results in decreasing a switching loss. This is the reason that the PDM is applied to the matrix converter in this paper.

IV. ZVS Operation Of Primary Converter

The basic operation of ZVS for the proposed converter is explained in this chapter. In the proposed circuit, if the transformer current discharges in the drain-to-source capacitance C_{ds} during dead time, the switching becomes ZVS. It should be noted that if the buffer current which flows power decoupling circuit as shown in chapter III discharges in C_{ds} during dead time, the switching also becomes ZVS.

A. Conduction Mode at Secondary Side of Transformer

The effects of parasitic elements in the transformer and the load inductance L_{load} are neglected for the simplicity. In this condition mode, the matrix converter does not output zero voltage and the load current flows to the secondary transformer. In order to achieve ZVS in primary side, the relationship among the buffer current, the output current of MC and the current in each other arm of the full-bridge current is required.

In the conventional DC to AC converter without the power decoupling circuit in reference [8], the load current equals to the transformer current by assuming that the exciting current is small enough to be neglected. Therefore, the switching devices which achieve ZVS are determined by the pole of the transformer current. The relationship between the pole of the transformer current and the ZVS-achieving switching devices is as follows.

1) $i_a > 0$: S_{an}, S_{bp}
2) $i_a < 0$: S_{ap}, S_{bn}

On the other hand, in the proposed converter, the transformer current overlaps with the common current. Thus, the currents i_a, i_b in each arm are presented by (6)-(7).

$$i_a(t) = i_{dif}(t) + \frac{1}{2} i_{buf}(t) \tag{6}$$

$$i_b(t) = i_{dif}(t) - \frac{1}{2} i_{buf}(t) \tag{7}$$

where, i_{bif}(t) is the transformer current and changes according to the output current of MC, i_{buf}(t) is the buffer current in the power decoupling circuit and changes according to the output power. If the maximum output current is I_m, (6)-(7) are rewritten as (8)-(9).

$$i_a(t) = I_m \sin(\omega_o t) + \frac{1}{2} \frac{P_{ave} \cos(2\omega_0 t)}{\sqrt{\frac{V_{bus}^{\ 2}}{4} + \frac{P_{ave}}{\omega_o C_{buf}} \sin(2\omega_o t)}} \tag{8}$$

$$i_b(t) = I_m \sin(\omega_o t) - \frac{1}{2} \frac{P_{ave} \cos(2\omega_0 t)}{\sqrt{\frac{V_{bus}^{\ 2}}{4} + \frac{P_{ave}}{\omega_o C_{buf}} \sin(2\omega_o t)}} \tag{9}$$

As above stated, the phase current in primary inverter is the sum of the buffer current and the output current. Therefore, both the ZVS-achieving switching devices and the ZVS range are determined by the pole of transformer current, the buffer current and phase $\Theta = \omega_o t$.

In order to achieve ZVS in the primary inverter, the current i_a, i_b in each phase are required to be higher than the lower limit value i_{lim}. If the current i_a, i_b in each phase is below i_{lim} the charges in the drain-to-source capacitance C_{ds} cannot be discharged completely during dead time. The lower limit value i_{lim} which achieves ZVS in the primary side is presented by (10).

$$i_{\lim} \geq \frac{C_{ds} V_{bus}}{T_{dead}} \tag{01}$$

B. Zero Voltage Mode at Secondary Side of Transformer

Fig. 6 shows the current path-way of the proposed circuit when the matrix converter outputs zero voltage. When PDM is applied for the secondary converter, the converter outputting zero voltage makes p-n line become open. In the conventional circuit without the power decoupling circuit, the secondary transformer current becomes zero. Therefore, the primary inverter does not have the transformer current meet the condition for (10) to achieve ZVS. On the other hand, in the proposed circuit, by applying the center-tapped transformer and the power decoupling circuit as shown in chapter 3 to compensate the ripple component, the buffer current becomes the sinusoidal wave at 100 Hz. Hence, in the proposed converter, the transformer current flows according to the buffer current even when the matrix converter outputs zero voltage. The pole of the transformer current is decided by the pole of the buffer current. Thus, the ZVS-achieving switching devices are decided by the load current and phase because the buffer current are decided by the load current i_{out} (t). In this paper, the ZVS condition of the ZVS-achieving switching devices which varies depending on the load current i_{out} (t) and the phase are discussed using simulation.

The current to discharge completely the drain-to-source capacitance C_{ds} has to meet (10). Therefore, the boundary condition of the buffer current i_{buf}(t) to achieve ZVS at primary side is presented by (11).

$$i_{buf} \geq \frac{4 C_{ds} V_{bus}}{T_{dead}} \tag{11}$$

As shown above, this proposed converter can achieve both ZVS in the primary inverter and the power decoupling whereas

the in reduction of the DC bus current ripple is also accomplished. In addition, because ZVS can be achieved in the primary inverter, the proposed converter is expected to achieve a downsizing and lower loss.

V. Simulation And Experimental Results

A. Simulation Results in Steady State

In order to verify the proposed ZVS method of the primary inverter described in chapter IV, ZVS achievable range in the inverter at primary side is discussed using simulation.

Table 1 shows the simulation condition for the isolated single-phase matrix converter with the proposed power decoupling method as drawn in Fig. 2. It should be noted that the output voltage of MC is 100 V_{rms}, the output power is 1 kW, the output frequency is 50 Hz, and the power factor of the output current is 1.

Fig. 7 shows the relationship between the absolute value of the output current i_{out} and the phase $\Theta=\omega_o t$. In Fig. 7, in the domain around the highest value of the output current, both legs achieve ZVS, because the current which discharges completely the drain-to-source capacitor C_{ds} is high enough. On the other hand, in the domain around the least value of the output current, the buffer current approaches the maximum value. Therefore, the primary inverter achieves ZVS only if the buffer current meets the criterion shown in (11). In contrast, the red area in Fig. 7 shows the period in which the top arm at the primary inverter do not achieve ZVS during the zero voltage period of the matrix converter, and the other area shows the period in which the bottom arm at the primary inverter do not achieve ZVS during the zero voltage period of the matrix converter. It should be noted that the red area and other area is the region which can get the current to achieve ZVS if the matrix converter do not output zero voltage. In the zero voltage period of the matrix converter, the reason why the ZVS-achieving switching devices change is that the pole of the buffer current changes according to the phase of the output current. As the result, in the proposed converter, the transformer current to achieve ZVS still flows through the buffer circuit even during the zero voltage period of the matrix converter shown in section IV-A. Finally, in the 0 A vicinity of the buffer current, this proposed converter does not achieve ZVS at the primary inverter because the buffer current do not meet (11).

Fig. 8 shows the gate-source voltage and the drain-source voltage at rated load. Fig. 8 (a), (b), and (c) shows the waveform of domain A, B, and C in Fig.7, respectively. In Fig. 8, the gate-source voltage rises after the drain-source voltage drops to zero due to the resonance between the drain-source capacitance and the leakage inductance of the transformer. Therefore, the ZVS of the inverter at primary side is achieved. It is confirmed from Fig. 8, the switching devices which achieve ZVS agree with the domain shown in Fig. 7. As a result, each switches of the primary inverter achieve ZVS in corresponding domain. Thus, it is possible to reduce the switching loss of the inverter at primary side.

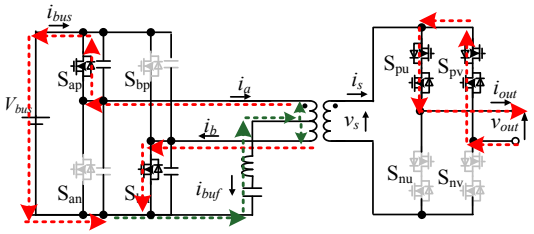


Fig. 6. A relationship between a switching operation and current path-way in the proposed circuit when the matrix converter outputs zero voltage.

TABLE I. Simulation Condition of Proposed System.

Rated power	1.0 kW	DC bus voltage	380 V_{dc}
Buffer L (L_{buf})	0.5 mH	Turn ratio N_1/N_2	1
Buffer C (C_{buf})	400 μF	Drain to source capacitance C_{ds}	1.125nF
Load current	10 A_{rms}		
Carrier frequency of full bridge inverter	100 kHz	Carrier frequency of matrix converter	10 kHz

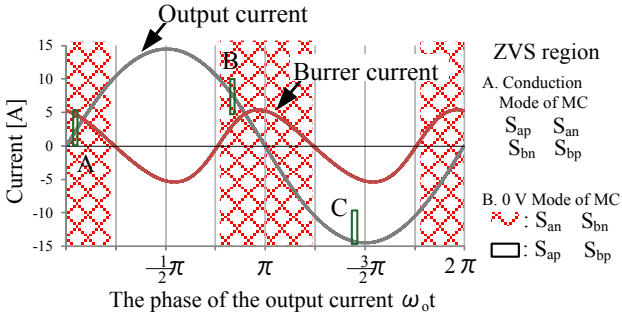


Fig.7. A characteristic of the output current, the buffer current and the phase of the output current. The area which achieve ZVS at primary side is decided the pole of the buffer current.

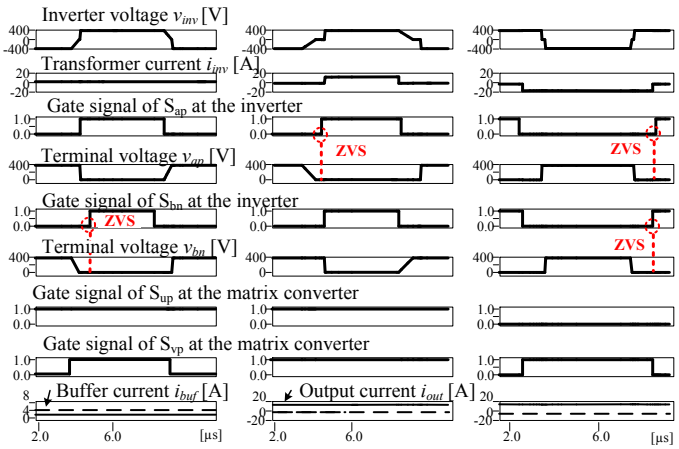


Fig.8. Extended waveform of a switching pattern for each periods of output current. Fig. 8(a), (b), and (c) shows the waveform of domain A, B, and C in Fig.7.

B. Experimental Results in Steady State

Fig. 9 (a) and (b) shows the waveform with and without the power decoupling method. In Fig. 8(a), the buffer capacitor voltage does not change because the full bridge inverter does not output the common mode AC voltage. As a result, the DC bus

current has a power ripple component at 100 Hz. In contrast, the proposed power decoupling method provides the common mode AC voltage to fluctuate the buffer capacitor voltage. As a result, the power ripple component in the DC bus current is decreased.

Fig. 10 shows a harmonic analysis of the DC bus current. It should be noted that the fundamental frequency is the output frequency at 50 Hz. From the result, it is understood that without the power decoupling method, the power ripple component at 100 Hz is 62.6% compared to an average current. In contrast, the proposed method reduces the 100 Hz component to 9.30% because the buffer capacitor voltage fluctuation absorbs the power ripple at 100 Hz. As a result, the ripple of the DC bus current is suppressed by 85.1%.

Fig. 11 shows experimental waveforms of the proposed converter with V_{bus} of 350 V, v_{grid} of 100 V_{peak}, T_{dead} of 500 ns and an R-L load of 500 W. From Fig. 11, the gate-source voltage in S_{bn} rises after the drain-source voltage drops in S_{bn} to zero due to the resonance between the drain-source capacitance of S_{bn} and the buffer inductance. In addition, it is confirmed from Fig. 11 that the switching devices achieve ZVS when the condition of the output current value calculated by (10) is satisfied.

VI. CONCLUSION

In this paper, in order to achieve high efficiency without any additional passive components, ZVS achievable range and the condition for the inverter at primary side of the transformer using the proposed power decoupling circuit are discussed. In this proposed system, even when the transformer's differential current which delivers the power to the secondary side of transformer is below the lower limit value to achieve ZVS or when the matrix converter outputs zero voltage, the proposed converter still achieves ZVS, because there is the buffer current overlapping to the transformer current. In addition, both the ZVS operation and the power decoupling are achieved which results in reducing the DC bus current ripple at the same time. As a result, the ripple of the DC bus current is suppressed by 85.1% by experiments. Moreover, in experimental results, the ZVS operation on the primary side of the transformer is confirmed.

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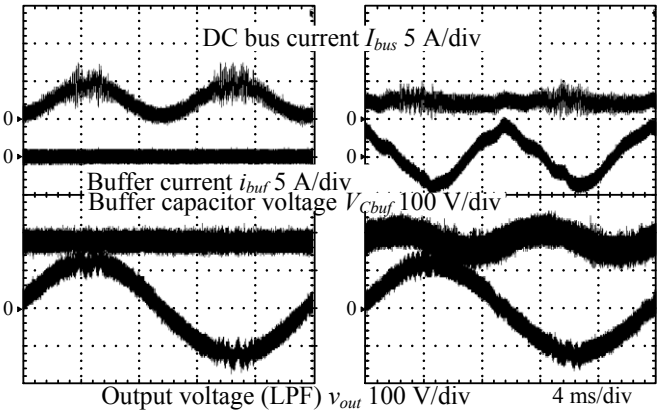

(a) Without the power decoupling method. (b) With the power decoupling method

Fig.9. Input and output waveforms in a steady state.

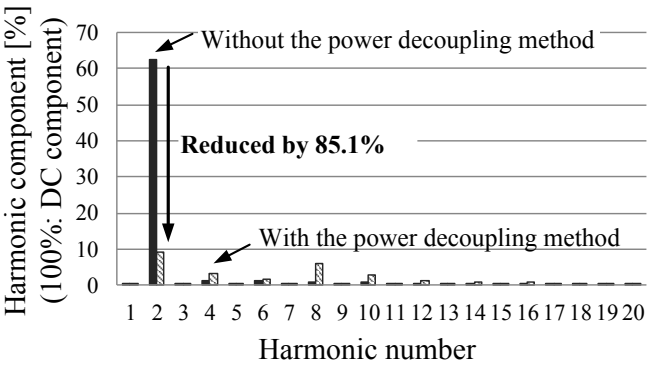

Fig. 10. Harmonic analysis of the DC bus current. The power decoupling method reduces the DC bus current ripple by 85.1% compared to when the power decoupling is not applied.

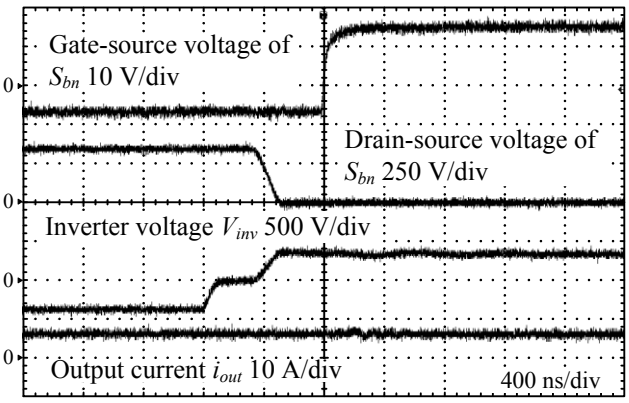

Fig.11. Experimental waveform at 50% rated power. The gate-source voltage in S_{bn} rises after the drain-source voltage drops in S_{bn} to zero due to the resonance between the drain-source capacitance of S_{bn} and the buffer inductance.

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