Clarification of Relationship between Current Ripple and Power Density in Bidirectional DC-DC Converter

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***Abstract*— This paper clarifies the relationship between the current ripple and the power density in bidirectional DC-DC converters. In the conventional power density design method, in order to obtain the pareto-front curve of the power density and the efficiency, the current ripple is designed as constant value, whereas the switching frequency is varied. As a result, the possibilities of higher power density or higher efficiency at different current ripple are not considered. Therefore, in this paper, the current ripple is also varied in order to evaluate all the designable power density. Specifically, a design flow chart is introduced to show step-by-step how to express all the losses and the volume of the converter as functions of the current ripple. Several 1-kW prototypes are constructed in order to confirm the validity of the design flow chart. By varying the current ripple, the highest power density of 10.1 kW/dm^3 with the efficiency of 98.55% is achieved at the current ripple of 60%. Furthermore, the maximum error between the calculated and experimental power density and efficiency are 19.5% and 0.22 pt. respectively.**

Keywords—pareto-front curve; power density; current ripple

I. INTRODUCTION

In recent years, non-isolated bidirectional DC-DC converters are widely applied to battery systems in Hybrid Electric Vehicles (HEVs), or Uninterruptible Power Supplies. This DC-DC converter is required to have small size and high efficiency. The minimization of converters provides not only the material cost reduction but also the easy implementation for applications which requires space-saving power system. Because the passive components such as inductors and capacitors account for the majority of the volume of DC-DC converters, the miniaturization of these passive components leads to compact DC-DC converter. Many minimization methods have been proposed such as high frequency switching, or resonant circuit [1]-[2]. However, higher switching frequency leads to the increase of switching loss, noise level, and also requires high-speed controller [3]-[4].

The boost inductor is one of the components which contributes mainly to the converter volume. By reducing the inductance, the volume of the boost inductor can be reduced. Instead of increasing the switching frequency, the inductance can be reduced by increasing the current ripple with interleaved topology [5]. In the interleaved topology, the total current ripple can still be maintained at small value despite that the current ripple in each phase is increased. This avoids the complexity of the input filter design in the applications where the current ripple is strictly limited [6]. However, many challenges arise when the current ripple is increased such as the high flux density ripple, which increases the core loss. Besides, the high current ripple increases the effective current for the same average current. This leads to higher conduction loss in the semiconductor devices, the boost inductor, and higher current rating for the capacitors, which result in larger volume of the heatsink and the capacitors. Therefore, the increase of the current ripple introduces the tradeoff relationship among the volume of the boost inductor, the power conversion efficiency and the volume of other components in the circuit. In order to design the converter at the high power density with the acceptable power conversion efficiency, the relationship between the current ripple and the power density is necessary to be clarified. According to the knowledge of the author, this relationship has not been researched thoroughly yet.

In this paper, the relationship between the current ripple and the power density of the bidirectional DC-DC converter is clarified by the pareto-front curve of the power density and the efficiency. Specifically, a flow chart is introduced to show step-by-step how to obtain the pareto-front curve when the current ripple is varied. First, the semiconductor devices' losses are calculated in order to design the heatsink volume. Second, the method is explained to design the capacitor volume with the condition that both the current ripple and the voltage ripple are satisfied. One of the most difficult challenges is the design of the inductor. When the inductance is reduced by increasing the current ripple, the winding loss decreases due to the decrease of the winding turns. However, the core loss increases due to the high flux density ripple. This results in another tradeoff relationship between the winding loss and the core loss in the inductor design step. Therefore, the method to achieve the smallest volume of the inductor with the lowest loss is explained. Finally, several 1-kW prototypes are constructed in order to verify the validity and the effectiveness of the proposed power density design flow chart.

II. CIRCUIT TOPOLOGY

Fig. 1 shows the circuit of the non-isolated bidirectional DC-DC converter. In order to achieve the high power density with the acceptable power conversion efficiency, the analysis of the relationship between losses and volume is conducted. In this circuit, four main kinds of loss occur; the conduction loss

and the switching loss due to the on-resistance and the non-ideal switching of the semiconductor devices (P_{cond}, P_{sw}), the core loss and the winding loss of the boost inductor (P_{core}, P_{wind}). On the other hand, there are three factors which contribute to the volume; the heatsink of the semiconductor devices Vol_H, the boost inductor Vol_L and the capacitor Vol_C. By varying both the switching frequency and the current ripple, every possibilities of the designable power density can be evaluated. This paper limits to the one-phase DC-DC converter. However, the optimal phase for the interleaved topology can be calculated simply with the proposed power density design method.

III. Flowchart Of Power Density Design Method

Fig. 2 shows the flowchart to design the power density when both the switching frequency and the current ripple are varied. The main contribution of the paper to the conventional power density design method is to consider the current ripple as a variable. First, the range of the switching frequency f_{sw} and the current ripple ΔI are selected.

Fig. 3 shows the definition of the boost inductor current ripple ΔI and the output voltage ripple $\Delta V_{p\text{-}p}$. In this paper, the switching frequency f_{sw} is kept constant at 50 kHz, whereas the current ripple ΔI is varied in 10%~200%, because the design of the power density by varying the switching frequency f_{sw} at the constant current ripple ΔI is considered as the conventional design method. It should be noted that, when the current ripple is larger than 100%, the DC-DC converter can be operated in either Continuous Current Mode (CCM) or Discontinuous Current Mode (DCM). Second, at certain (f_{sw},ΔI), the variables such as the inductance L, the capacitance C, and the maximum current I_{max} are calculated. Then, the heatsink volume Vol_H is calculated from the semiconductor device losses P_{cond} and P_{sw}. After that, the effective value of the capacitor current I_{C_rms} is calculated. The capacitor volume is designed in the condition that both the capacitance C and the allowable effective current are satisfied.

Next, from the inductance L and the maximum current I_{max}, the required storage energy in the boost inductor is calculated in order to select the core size. Because the high power density is preferred, the minimum designable core size is selected. With certain core size, the evaluation range of the air gap is selected. Next, at certain air gap, the winding turns N is calculated and decided whether this design can be implemented. In case that all the windings can be fit into the window area of the core, the inductor volume Vol_L, and the inductor loss P_{core}, P_{wind} are calculated. After that, the length of the air gap is increased in order to find another combination of P_{core} and P_{wind}. In case that all the windings cannot be fit into the window area of the core, the current ripple and the switching frequency are varied in order to evaluate the losses and the volumes at the next combination of (f_{sw},ΔI).

A. Design of heatsink

The volume of the heatsink changes according to the loss from the semiconductor devices. The estimation of the heatsink volume is conducted based on the Cooling System Performance Index (CSPI) [7]. CSPI is defined as the inverse factor of the thermal resistance per unit volume. Furthermore,

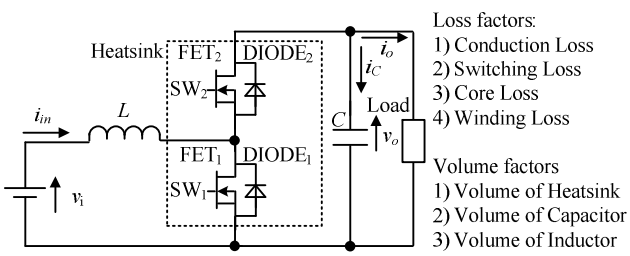


Fig. 1. Non-isolated bidirectional DC-DC with simple buck-boost topology. The losses and volume is calculated in order to design the power density and the power conversion efficiency.

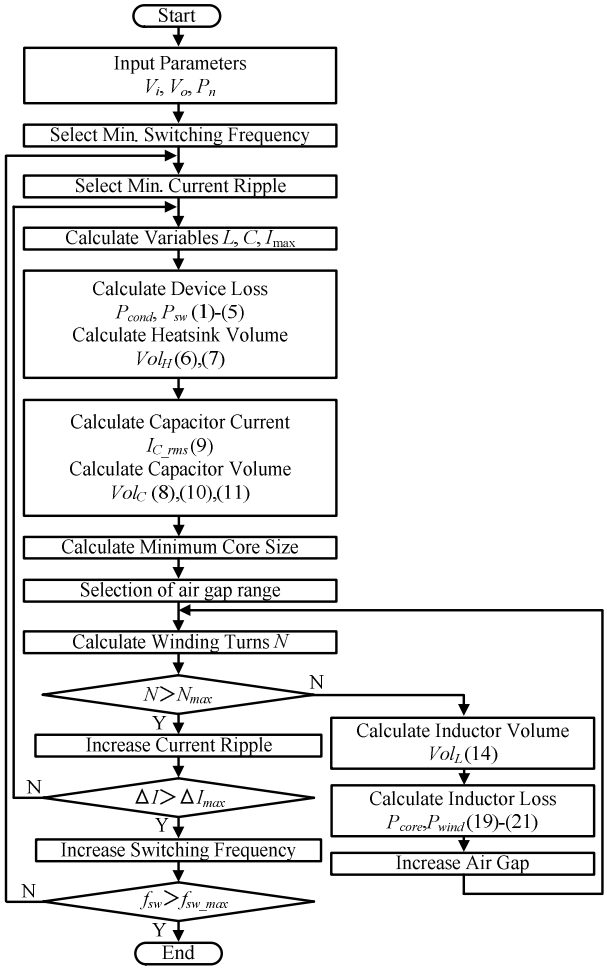


Fig. 2. Flowchart to design power density when both switching frequency and current ripple are varied. By this method, every possibilities of the designable power density can be evaluated.

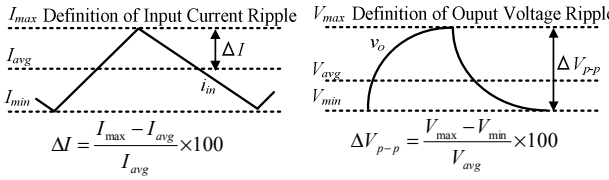


Fig. 3. Definition of boost inductor current ripple and output voltage ripple. By increasing the current ripple, the inductance of the boost inductor is decreased. This leads to the size reduction of the boost inductor.

the higher CSPI becomes, the more effective the heat is dissipated through the heatsink.

First, the conduction loss P_{cond} and the switching loss P_{sw} of the semiconductor devices are derived as follows. In this paper, MOSFET is chosen as the semiconductor devices. The conduction loss P_{cond} is calculated by the effective current flowing through MOSFET and the on-resistance of MOSFET,

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} {i_{in}}^2 R_{on} dt = R_{on} \left({I_{avg}}^2 + \frac{\Delta I^2}{3} \right) \quad (1)$$

Where, T_{sw} is the switching period, R_{on} is the on-resistance of MOSFET, and i_{in}, I_{avg}, ΔI are the instantaneous value, the average value and the ripple of the boost inductor current respectively as shown in Fig. 3.

Fig. 4 shows the pattern of the switching losses when the current ripple is varied. When the current ripple is smaller than 100%, the DC-DC converter is operated in only CCM. However, when the current ripple is larger than 100%, the DC-DC converter is operated in either CCM or DCM. The turn-on loss P_{sw_on} is calculated by,

$$P_{sw\_on} = \frac{1}{T_{sw}} \int_0^{t_r} v_{ds} i_{ds} dt = f_{sw} K_{sw} V_o t_r (I_{avg} - \Delta I) \quad (2)$$

Where, v_{ds} is the voltage applied to MOSFET, i_{ds} is the current flowing through MOSFET, K_{sw} is the coefficient derived from the switching waveform [9], V_o is the output voltage, and t_r is the rise time of the MOSFET current i_{ds}. Similarly, the turn-off loss P_{sw_off} is calculated by,

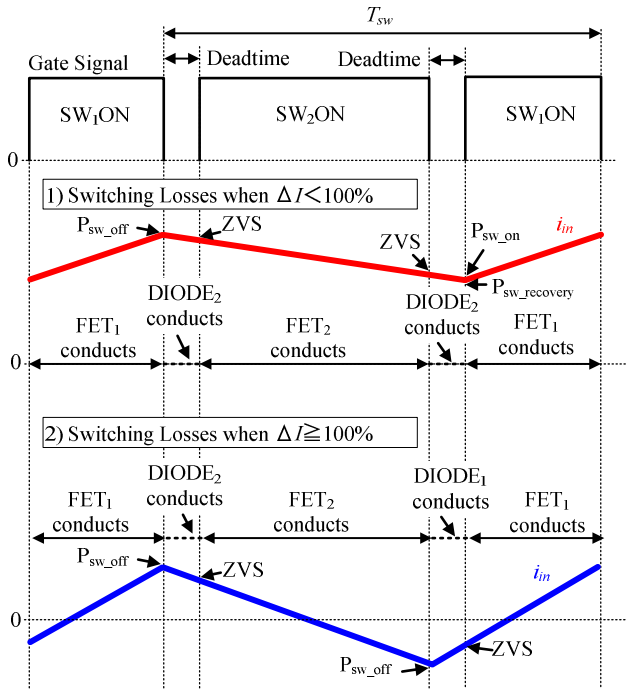
$$P_{sw\_off} = \frac{1}{T_{sw}} \int_0^{t_f} v_{ds} i_{ds} dt = f_{sw} K_{sw} V_o t_f (I_{avg} + \Delta I) \quad (3)$$

Where, t_f is the fall time of the MOSFET current i_{ds}. On the other hand, the reverse recovery loss in the parasitic diode $P_{sw\_recovery}$ is calculated by [8],

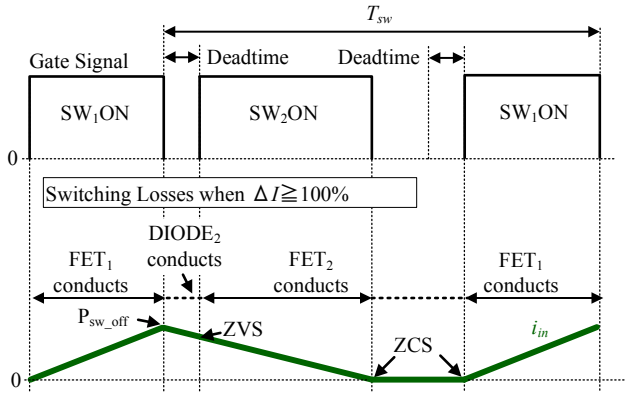
$$P_{sw\_recovery} = f_{sw} V_o \left[\frac{I_{rrm}}{k_{Ifall}} | I_{avg} - \Delta I | + Q_{rr} \right] \quad (4)$$

Where, I_{rrm} is the peak value of the reverse recovery current, k_{Ifall} is the current decrease rate, and Q_{rr} is the reverse recovery charge. The total switching loss of MOSFET changes corresponding to the current ripple, and is classified as shown in Fig. 4,

$$\begin{aligned} &\Delta I < 100\%(\text{CCM}) : P_{sw} = P_{sw1\_on} + P_{sw1\_off} + P_{sw1\_recovery} \\ &\Delta I \geq 100\%(\text{CCM}) : P_{sw} = P_{sw1\_off} + P_{sw2\_off} \\ &\Delta I \geq 100\%(\text{DCM}) : P_{sw} = P_{sw1\_off} \end{aligned} \quad (5)$$



a) Switching losses in CCM.



b) Switching losses in DCM.

Fig. 4. Pattern of switching losses when current ripple is varied. When the current ripple is smaller than 100%, the reverse recovery, which results in high switching loss, occurs in the parasitic diode. When the current ripple is larger than 100%, the DC-DC can be operated in either CCM or DCM.

Fig. 5 shows the relationship between the current ripple and the MOSFET loss. When the current ripple is increased, the effective current also increases. This leads to the increase in the conduction loss. On the other hand, when the current ripple is smaller than 100%, the reverse recovery, which results in high switching loss, occurs in the parasitic diode. Furthermore, when the current ripple is larger than 100%, by applying DCM, not only the switching loss but also the conduction loss are reduced due to the decrease in the effective current. However, the control method for DCM becomes complex due to the nonlinearity in DCM [10].

From (1)-(5), the required thermal resistance between the heatsink and the ambience $R_{th(s\text{-}a)}$ is calculated by [11],

$$R_{th(s-a)} = \frac{T_j - T_a}{P_{cond} + P_{sw}} - R_{th(j-s)} \tag{6}$$

Where, T_j is the junction temperature of the MOSFET, T_a is the ambient temperature, and $R_{th(j-s)}$ is the thermal resistance between the junction and the heatsink. Next, the volume of the heatsink Vol_H is estimated by [7],

$$Vol_H = \frac{1}{R_{th(s-a)} CSPI} \tag{7}$$

Where, CSPI is the coefficient which depends on the cooling methods such as natural cooling or water cooling. CSPI can be extracted from the datasheet of the heatsink or can be obtained in optimal heatsink design [7].

B. Design of capacitor

The volume of the capacitor depends on the capacitance C, the allowable effective current, and the type of the implemented capacitors. There are three main types of the capacitor; the electrolytic capacitor, the film capacitor, and the ceramic capacitor. The film capacitor and the ceramic capacitor are evaluated to have longer life time than the electrolytic capacitor in high temperature environment such as HEVs. Moreover, with the same required capacitance, the ceramic capacitor volume is smaller than the film capacitor volume due to the high dielectric coefficient of the ceramic capacitor. Therefore, in this paper, the ceramic capacitor is applied. First, the capacitance C is calculated as a function of the desired peak-to-peak voltage ripple $\Delta V_{p\text{-}p}$,

$$C = \frac{I_{avg}}{0.5\Delta V_{p-p}} \frac{1}{f_{sw}} D_1(1 - D_1) \tag{8}$$

Where, D_1 is the duty ratio of SW_1. Then, the effective current I_{C_rms} flowing to the capacitor is calculated by,

$$\begin{aligned} I_{C\_rms} &= \sqrt{\frac{1}{T_{sw}} \int_0^{Tsw} i_C^2 dt} \\ &= \sqrt{D_1 \left[\frac{(I_{\max} - I_{\min})^2}{3} + (I_{\max} - I_o)(I_{\min} - I_o) \right] + (1 - D_1) I_o^2} \end{aligned} \tag{9}$$

Where i_C is the instantaneous value of the capacitor current, and I_o is the average output current as shown in Fig. 1.

Fig. 6 shows the relationship between the capacitance change rate due to DC bias voltage from Murata Manufacturer. When the DC bias voltage is applied to the ceramic capacitor, the effective capacitance decreases [12]. Therefore, when applying the ceramic capacitor, the capacitor is necessary to be designed based on the DC bias voltage characteristic in the datasheet. The actual designed capacitance C_{design} is calculated by the capacitance change rate due to DC bias voltage K_{DCbias} and the required capacitance C,

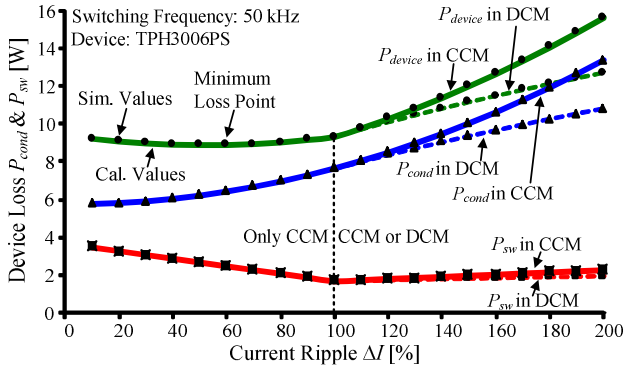
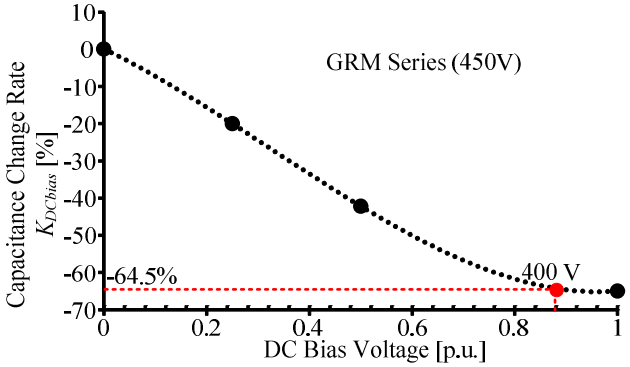


Fig. 5. Relationship between current ripple and MOSFET loss. When the current ripple is increased, the conduction loss increases. On the other hand, when the current ripple is set as 100%, the DC-DC converter is operated in Boundary Conduction Mode. In this mode, the switching loss reaches the smallest value. When the current ripple is larger than 100%, by applying DCM, not only the switching loss but also the conduction loss are reduced due to the decrease in the effective current [10].



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$$C_{design} = C \frac{100}{100 + K_{DCbias}} \tag{10}$$

Fig. 7 shows the ratio between the capacitance and the allowable effective current from the datasheet [12]. It is necessary to make the capacitor current below the allowable effective current. The method to satisfy both the allowable effective current and the actual designed capacitance is to connect capacitors in parallel. However, this might increase the capacitor volume. Therefore, the procedure to achieve the smallest designable capacitor volume is applied. First, the dashed line which shows the designable capacitors in Fig. 7, is calculated by,

$$\frac{I_{rms\_data}}{C_{data}} \geq \frac{I_{C\_rms}}{C_{design}} \tag{11}$$

Where, I_{rms_data} and C_{data} are the allowable effective current and the capacitance for each series of capacitor in the datasheet respectively. From Fig. 7, it is understood that, by connecting

the capacitors with high ratio between the allowable effective current and the capacitance, the allowable effective current is simply satisfied. Then, from the designable capacitors, the capacitor which achieves the smallest volume is selected.

Fig. 8 shows the relationship between the capacitor volume and the actual designed capacitance. It is understood that, the capacitor with the highest ratio between the allowable effective current and the capacitance does not always achieve the smallest volume. By this procedure of capacitor design, the smallest volume of capacitor is achieved with the satisfaction of both the allowable effective current and the actual designed capacitance.

C. Design of boost inductor

1) Estimation of inductor volume

In this section the design of the boost inductor to achieve the smallest volume and lowest loss is explained. First, the inductance L is calculated from the boost inductor current ripple ΔI,

$$L = \frac{1}{f_{sw}\Delta I}\frac{V_i(V_o - V_i)}{2V_o} \tag{12}$$

Where, V_i is the input voltage. The inductor volume Vol_L is calculated by Area Product [13],

$$Vol_L = K_V\left(\frac{LI_{\max}^2}{K_u B_{\max} J}\right)^{\frac{3}{4}} \tag{13}$$

Where, K_V is the coefficient which depends on the shape of the core [13], K_u is the window utilization factor, B_{max} is the maximum flux density of the core, and J is the current density. By substituting (12) into (13), the equation of the inductor volume is rewritten as the function of the current ripple ΔI and the switching frequency f_{sw},

$$Vol_L = K_V\left[\frac{V_i(V_o - V_i)I_{avg}}{2K_u B_{\max} J V_o}\frac{1}{f_{sw}}\left(\sqrt{\Delta I} + \frac{1}{\sqrt{\Delta I}}\right)\right]^{\frac{3}{4}} \tag{14}$$

It is clearly understood from (14) that, the inductor volume depends on both the switching frequency f_{sw} and the current ripple ΔI. Therefore, in case only the switching frequency is varied, the smallest designable inductor volume might be unconsidered.

Fig. 9 shows the relationship between the current ripple and the volume of the DC-DC converter. Because the heatsink volume depends on the MOSFET loss as shown in (6), and (7), the dependence of the heatsink volume on the current ripple is similar to the relationship between the MOSFET loss and the current ripple as shown in Fig. 5. Besides, the capacitor volume is relatively small because the ceramic capacitor with the high dielectric coefficient is applied. On the other hand, the inductor volume reaches the smallest value when the current ripple is designed at 100%. When the current ripple is increased over 100%, the required storage energy in the inductor can be no longer decreased due to the increase of the current peak I_{max} as shown in (13) and (14). In order to achieve the highest power density, the smallest core size which satisfies (15) is selected [13].

$$A_e A_w \geq \frac{LI_{\max}^2}{JB_{\max}K_u} \tag{15}$$

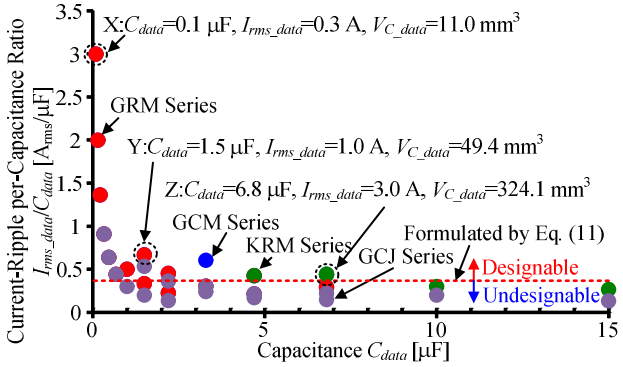


Fig. 7. Relationship between allowable current ripple and capacitance from Murata Manufacturer [12]. The higher the ratio between the allowable effective current and the capacitance becomes, the more simply the allowable effective current is satisfied.

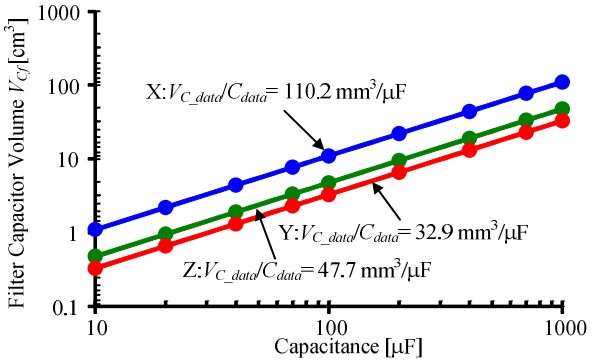


Fig. 8. Relationship between capacitor volume and capacitance. From the designable capacitors shown in Fig. 7, the capacitor which achieves the smallest volume is selected. It should be noted that the capacitor with the highest ratio between the allowable effective current and the capacitance, does not always achieve the smallest volume.

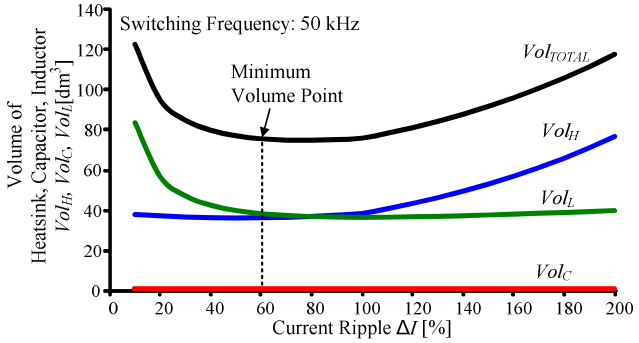


Fig. 9. Relationship between current ripple and converter volume. By varying the current ripple, the smallest volume of the converter is achieved at current ripple of 60%.

Where A_e, and A_w are the cross-sectional area, and the window area of the core.

2) Calculation of winding turns

With selected core, the air gap is varied in order to achieve the smallest inductor loss. This section explained the method to calculate the required winding turns at certain air gap l_g. The winding turns N is calculated by,

$$N = \sqrt{L(R_g + R_c)} \tag{16}$$

Where, R_g and R_c are the reluctance of the gap and the core. In the case that the air gap is applied to avoid the flux saturation, the fringing flux near the gap is necessary to be consider in order to calculate the winding turns accurately. Specifically, the conventional and improved equations to calculate the reluctance of the gap are as follows respectively,

$$R_{g\_conv} = \frac{1}{A_e}\frac{l_g}{\mu_o} \tag{17}$$

$$R_{g\_impr} = \frac{\sigma_x \sigma_y}{A_e}\frac{l_g}{\mu_o} \tag{18}$$

Where, μ_o is the relative permeability of the core material, and σ_x, σ_y are the fringing factors considering the fringing effects in the x-direction and y-direction respectively. The procedure to calculate the fringing factor σ_x and σ_y with certain air gap shape has been explained thoroughly in [14].

3) Calculation of winding loss

The method to calculate the winding loss considering the skin effect is explained in this section. First, the effective cross-sectional area of the winding wire S_{wind} which considers the skin effect is calculated by,

$$S_{wind} = 4\pi\delta \frac{\left[r - \delta\left(1 - e^{-\frac{r}{\delta}}\right)\right]^2}{r - \frac{\delta}{2}\left(1 - e^{-\frac{r}{2\delta}}\right)} \tag{19}$$

Where, r is the radius of the winding wire, and δ is the skin depth at certain switching frequency [13]. Then, the winding loss P_{wind} is calculated by the effective value of the boost inductor current and the resistance of the winding wire R_{wind},

$$P_{wind} = \frac{1}{T_{sw}}\int_0^{T_{sw}} i_{in}^{\,2} R_{wind}\, dt = \frac{1}{\sigma}\frac{l_{wind}}{S_{wind}}\left(I_{avg}^{\,2} + \frac{\Delta I^2}{3}\right) \tag{20}$$

Where, l_{wind} is the length of the winding wire, and σ is the electrical conductivity of the winding material. In this paper, because the switching frequency is limited up to 50 kHz, the proximity effect is considered to be small enough to be negligible.

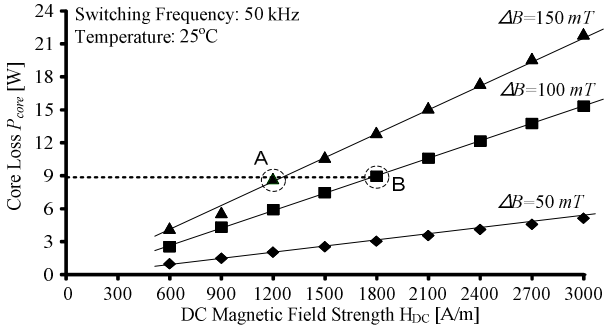


Fig. 10. LOSS MAP under DC bias conditions (ferrite PC40). By increasing the winding turn, the flux density ripple is reduced. However, because the premagnetization H_{DC} is increased, the core loss reduction is not effective.

4) Calculation of core loss

When the current ripple is increased, the flux density ripple becomes high, which leads to the high core loss. The core loss P_{core} is calculated by the improved Generalized Steinmetz Equation (iGSE),

$$P_{core} = V_e k_i' f_{sw}^{\ \alpha} \Delta B^{\beta'-\alpha}\left[\left|\frac{\Delta B}{D_1}\right|^{\alpha} D_1 + \left|\frac{\Delta B}{D_2}\right|^{\alpha} D_2\right] \tag{21}$$

where V_e is the effective core volume, ΔB is the flux density ripple and D_2 is the duty ratio of SW_2, k_i', α, β' are the iGSE parameters. The calculation of the core loss is conducted as following steps:

i) The LOSS MAP, which is the measured core losses of the triangular flux waveforms at different DC bias conditions, is obtained [15]-[16]. In this paper, the LOSS MAP is obtained at 3 different values of ΔB.

ii) The iGSE parameters k_i', α, β' are derived from the LOSS MAP in order to be able to calculate the core loss in various conditions [17].

Fig. 10 shows the LOSS MAP of PC40 (Ferrite) at 25°C. It is understood from Fig. 10 that, in case that the impact of DC bias to core losses cannot be negligible as in ferrite PC40, the reduction of ΔB is not always a good solution to reduce the core loss. Specifically, by increasing the winding turns, ΔB can be reduced from point A to point B; however, this increases the premagnetization H_{DC}, which increases the core loss. As the result, the increase in the winding turns cannot reduce the core loss but only increases the winding loss.

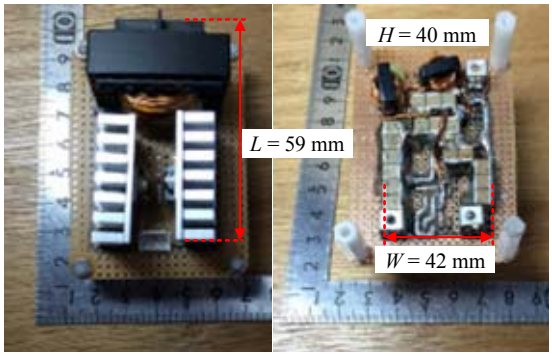
IV. Experimental Results

Table 1 shows the experimental condition and the parameters of the semiconductor devices and the inductor.

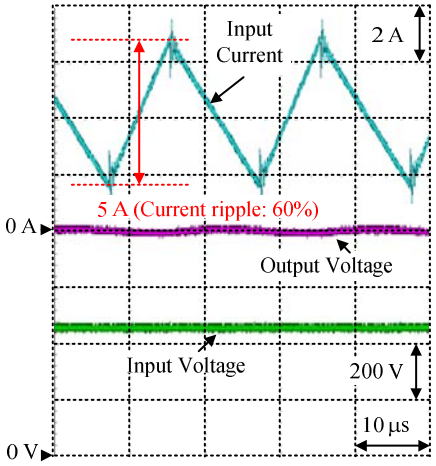
Fig. 11 shows one of the prototypes which are constructed in order to verify the validity of the proposed power density design method. In this paper, both the highest power density of 10.1 kW/dm^3 and the highest efficiency of 98.55% are achieved at the current ripple of 60%. By the waveform of the input current, it is confirmed that the core do not saturate at rated power.

Table 1. Experimental and Design Parameters.

Parameters of Circuit			Parameters of Capacitor		
Input Voltage	V_{in}	240 V	Output Voltage Ripple	$\Delta V_{p\text{-}p}$	5 V
Output Voltage	V_{out}	400 V	Cera. Capacitor GR355DD72W474KW01L		
Rated Power	P_n	1 kW	Parameter of Inductors (PC40)		
Rated Input Current	I_{in}	4.17 A	Saturated Flux Density	B_{max}	0.39 T
Switching Frequency	f_{sw}	50 kHz	Volume factor	K_V	35.8
Parameters of Switch (TPH3006PS)			Current Density	J	6 A/mm^2
On-Resistance	R_{on}	0.33 Ω	Space factor	K_u	0.5
Rated Voltage	V_{DS}	500 V	Gap Length	l_{g1}	0.75 mm
Rated Current	I_{DS}	12 A		l_{g2}	1.25 mm
Reverse Current	I_{rrm}	11 A		l_{g3}	1.5 mm
Reverse Recovery Charge	Q_{rr}	54 nC	Turn Numbers	N_1	33
				N_2	42
Parameters of Heat Sink				N_3	60
Junction Temperature	T_j	80 °C	Parameters of Prototype		
Ambient Temperature	T_a	25 °C	Length	L	59 mm
Junction-to-Case Thermal Resistance	$R_{th(j\text{-}s)}$	1.55 °C/W	Width	W	42 mm
			Height	H	40 mm
Cooling System Performance Index	CSPI	4	Power Density	ρ	10.1 kW/dm^3
			Maximum Efficiency	η	98.55 %



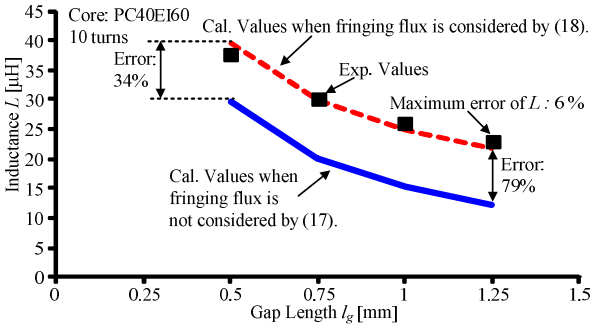
(a) Prototype Layout.



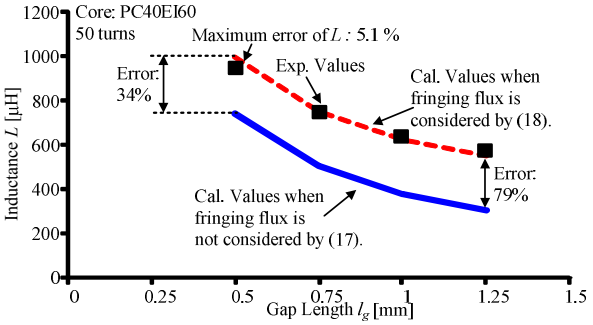
(b) Operation Waveform.

Fig. 11. 1-kW non-isolated DC-DC converter with power density of 10.1 kW/dm^3 and efficiency of 98.55%.

Fig. 12 shows the calculated and experimental inductance when the fringing flux is unconsidered/considered. When the air gap increases from 0.5 mm to 1.25 mm, the error between the calculated and experimental inductance increases from 34% to 79%. Furthermore, when the fringing flux is considered, the error is reduced from 79% to 6%.



(a) Inductance with 10 turns.



(b) Inductance with 50 turns.

Fig. 12. Inductance design with/without consideration of fringing flux around gap. By considering the fringing effect, the desired inductance is designed accurately. The winding turn design step is crucial to the inductor loss design.

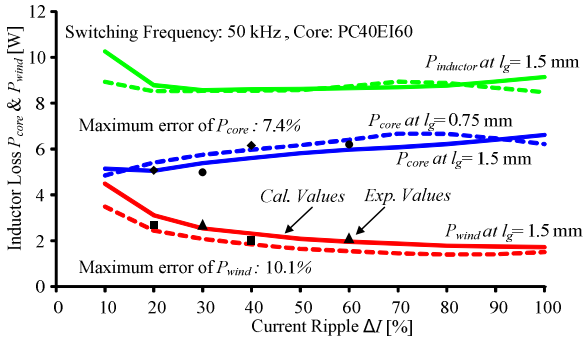


Fig. 13. Relationship between current ripple and inductor loss. The trade-off relationship between the winding loss and the core loss requires the optimal design of both the current ripple and the air gap.

Fig. 13 shows the relationship between the inductor loss and the current ripple. By increasing the air gap, the winding turns can be increased without making the core become saturated. However, the core loss does not always decrease by increasing the winding turns as explained above. The calculation of the winding loss by (20) still results with error of above 10% due to the inconsideration of the proximity effect.

Fig. 14 shows the experimental and calculated total loss. The experimental results agree to the calculated results with the error smaller than 10%. For simplicity, the air gap is designed at constant value (1.25 mm). However, as mentioned above, the air gap should be varied in order to find the lowest inductor loss. By calculating accurately the total loss, the efficiency can be designed simply.

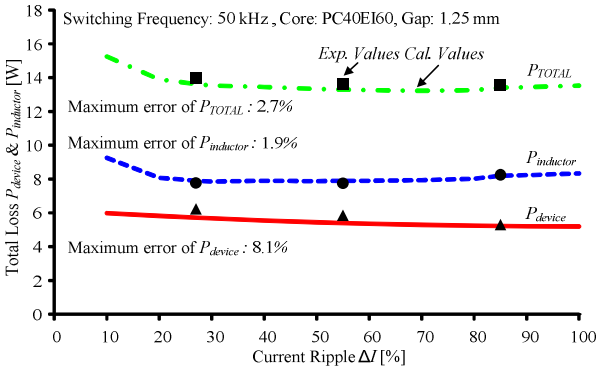


Fig. 14. Experimental and calculated results of total loss. By calculating the total loss accurately, the efficiency can be designed simply.

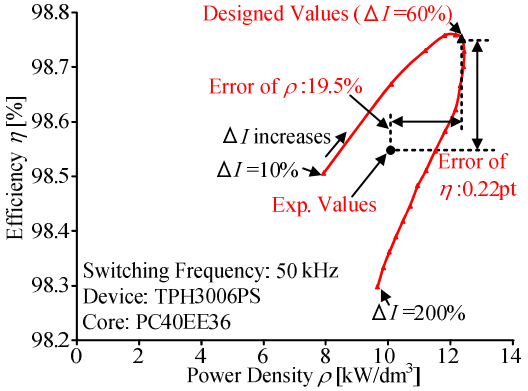


Fig. 15. η-ρ pareto front with current ripple as variable. The proposed power density design method enables to evaluate every possibilities of the designable power density.

Fig. 15 shows the pareto-front curves of the proposed design with the varied current ripple. The maximum errors in the power density and the efficiency are 19.5% and 0.22 pt., respectively. The error of the power density occurs because the air space between the devices is not considered in the proposed power density design method, whereas the errors of the efficiency occurs due to the inconsideration of the proximity effect and the fringing flux loss. However, the experimental power density without the air space almost agrees with the calculated value. This result confirms the validity of the proposed design. Furthermore, in this consideration, the highest power density can be reached with the highest efficiency. However, the parameters such as the switching frequency and the core material should be varied in order to find the optimum point of the power density or the efficiency.

V. Conclusion

In this paper, the relationship between the current ripple and the power density of the bidirectional DC-DC converter was clarified. The flowchart which was used to draw every possibilities of the designable power density in the pareto-front curve was introduced. Furthermore, the method to calculate the ceramic capacitor with condition that both the effective capacitor current and the capacitance are satisfied was explained. Besides, the method to design the smallest inductor with the lowest loss was also explained. Several 1-kW prototypes were constructed in order to verify the validity of the proposed power design method. The highest power density of 10.1 kW/dm^3 was achieved with the efficiency of 98.55% at the current ripple at 60%.

In the future, the consideration of the losses from the proximity effect and the fringing flux will be conducted in case that those losses cannot be neglected. Furthermore, the input filter will also be considered in order to satisfy the regulations of the noises.

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