Minimization of Interconnected Inductor for Single-Phase Inverter with High-Performance Disturbance Observer

Satoshi Nagai, Hoai Nam Le, Tsuyoshi Nagano, Koji Orikawa, Jun-ichi Itoh
Department of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Japan
satoshi_nagai@stn.nagaokaut.ac.jp

***Abstract*— When a inductance of a single-phase grid-connected inverter is minimized, the effect of the disturbance to the current control such as the dead-time error voltage increases. This paper proposes a disturbance compensation method by using a high-performance disturbance observer. In particular, in the control system, the current controller is implemented by the digital signal processor, whereas the high-performance disturbance observer is implemented by the field-programmable gate array in order to suppress the disturbance at high switching frequency. This results in the improvement of the current control performance. With the experimental prototype, in case of the minimized inductance (%Z = 0.5%), the total harmonic distortion (THD) of the output current is improved from 11.1% to 2.9% at rated load by applying the proposed disturbance compensation method. Furthermore, with the proposed disturbance compensation method, it is confirmed that THD of the output current is improved by over 68% at all load range.**

Keywords*— grid-connected inverter; interconnected inductor; disturbance observer; FPGA

I. INTRODUCTION

In recent years, photovoltaics systems (PV) have been actively researched for energy saving. In general, a power conditioning system (PCS) is used to supply power from the PV system to a single-phase grid. PCS has been actively studied in order to reduce the cost and size [1]-[2]. In order to minimize the PCS, an interconnected inductor in the PCS is required to be minimized [3]-[4]. The minimization of the inductor enables the PCS not only to be applied in space-saving applications, but also to reduce cost. The inductor can be minimized by reducing the inductance with high switching frequency. By applying the next generation switching devices, e.g. SiC-MOSFET and GaN-FET, the high frequency switching with low switching loss can be accomplished. However, the disturbance suppression performance decreases with the reduced inductance [5]. As a result, total harmonic distortion (THD) of the inverter output current becomes worse because the effect of the disturbance voltage which is caused by the disturbance sources such as the dead-time error voltage increase.

In a conventional dead-time voltage error compensation method, the error voltage is estimated from the inverter dc-link voltage, the dead-time, the switching frequency and the direction of the output current [6]. However, the conventional method suffers many problems; the disturbance compensation performance is limited by the delay time of a current sensor and an A/D converter, and the voltage drop of the switching device is also unconsidered. These problems worsen THD of the output current when the inductance is small. Furthermore, the error voltage by the dead-time becomes larger due to increasing the switching frequency. Therefore, the PCS requires an effective disturbance compensation method in order to reduce the inductance without worsening THD of the output current.

In order to overcome the above problem, the compensation for the error voltage by a disturbance observer, has been proposed in [7]-[11]. The disturbance observer compares the feedback current and the command in order to estimate the voltage error. Therefore, the disturbance observer is required to be operated as high as the switching frequency because the error voltage caused by the dead-time or the voltage drop of the switching device occurs at the switching frequency. As a result, the cost of the control hardware becomes undesirable when the disturbance observer is implemented with the high speed digital signal processor (DSP).

This paper proposes the concept in which the high-performance disturbance observer is implemented by the field-programmable gate array (FPGA), whereas the current controller is implemented by the slow speed DSP. This avoids the cost increase of the control hardware, whereas the disturbance suppression performance is increased by operating the disturbance observer at the switching frequency by FPGA. This paper is organized as follows; first in section II, the design of the disturbance observer in the s-plane is introduced, and the employment of the disturbance observer into FPGA is explained in detail. Next, in section III and IV, the validity of the proposed method are confirmed by the simulations and experiments with a 1-kW prototype. Finally, the design of the disturbance-observer cutoff frequency is evaluated.

II. Dead-time Voltage Error Compemsation Using Disturbance Observer

A. Control method

Fig. 1 shows a circuit configuration of a single-phase grid-connected inverter. In this paper, an H-bridge single-phase two-level inverter is considered due to its simplicity. When the inductance L is reduced in order to minimize the volume of the interconnected inductor, the effect of the disturbance voltage such as the dead-time error voltage increases. This worsens THD of the output current i_{out}.

Fig. 2 shows a control block diagram of the conventional dead-time voltage error compensation. In the conventional method, the error voltage from the dead-time v_{dead} is estimated in order to compensate for the output voltage of the inverter. The dead-time error voltage is expressed by

$$v_{dead} = V_{dc} T_d f_{sw} sign(i_{Ldet}) \tag{1}$$

where, V_{dc} is the input DC voltage, T_d is the dead-time period, i_{Ldet} is the inductor current detection value of the inverter, f_{sw} is the switching frequency of the inverter, and $sign(x)$ is a sign function. If $x > 0$ then $sign(x) = 1$, if $x < 0$ then $sign(x) = -1$, if $x = 0$ then $sign(x) = 0$. It is noted that the detection delay time of the current sensor, and the drop voltage on the switching devices are not considered in Eq.(1). These factors also become the disturbance to the output current control. The relationship between the disturbance voltage and the inductance is explained by the transfer function from the disturbance voltage to the output current witch is derived as

$$\frac{i_L}{v_{dis}} = \frac{1}{L} \frac{s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2}$$

where, v_{dis} is the disturbance voltage that is sum of the error voltages caused by the dead-time and the drop voltage of the switching device, ζ is the damping factor, ω_n is the angular frequency of the current controller, and s is the Laplace operator. When the inductance L becomes small, the disturbance gain becomes higher. As a result, the accuracy of the voltage error compensation becomes more important when the small interconnected inductor is applied.

Fig. 3 shows the control block diagram of the proposed method with the disturbance observer. In order to solve the problem in the conventional method, the disturbance observer is utilized to compensate all the disturbances accurately. As the disturbance voltage affects the output current, the disturbance compensate voltage $\hat{v}_{dis}$ is estimated from the output current and the voltage command,

$$\hat{v}_{dis} = \frac{\omega_c}{\omega_c + s}\left(v_{conv}^{*} + \omega_c L i_{Ldet}\right) - \omega_c L i_{Ldet} \tag{3}$$

where, ω_c is the cutoff angular frequency of the disturbance observer, v_{conv}^{*} is the output voltage of the inverter, and

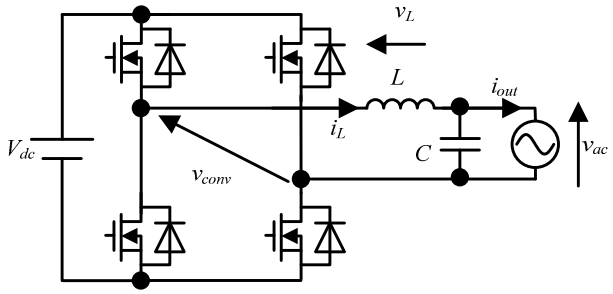


Fig. 1. Single-phase inverter circuit with LC filter. In order to minimize the interconnected inductor, the inductance L is reduced by increasing the switching frequency.

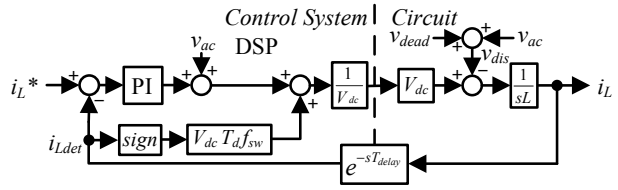


Fig. 2. Control block diagram of conventional dead-time error compensation. In the conventional method, the error voltage from the dead-time v_{dead} is estimated in order to compensate for the output voltage of the inverter

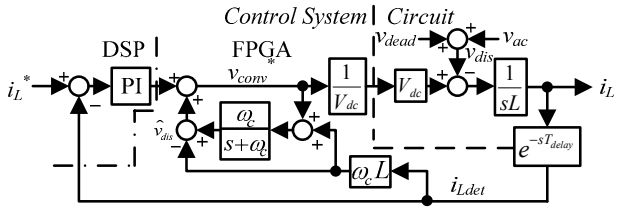


Fig. 3. Control block diagram of dead-time error compensation with disturbance observer. The disturbance observer is used to estimate all the disturbance voltage.

$e^{-sT_{delay}}$ is the delay time of the current detection and the A/D conversion. It should be noted that the delay time of the current detection and the A/D conversion are not used in the disturbance estimation. In this paper, the current controller is implemented by DSP, whereas the disturbance observer is implemented by FPGA. This concept achives the high-performance disturbance observer for high accuracy compensation.

B. Configration of the FPGA

The estimated disturbance voltage by using the disturbance observer in (3) is rewritten as in (4).

$$\hat{v}_{dis} = -\frac{\omega_c s}{\omega_c + s} L i_{Ldet} + \frac{\omega_c}{\omega_c + s} v_{conv}^{*} \tag{4}$$

In (4), the first term on the right side describes that the inverter output current i_{Ldet} is multiplied with the inductance L of the interconnected inductor and then passed through a high pass filter (HPF). The second term on the right side shows that the voltage command v_{conv}^{*} is passed through a low pass filter (LPF). In the right side of (4), let the first term and the second

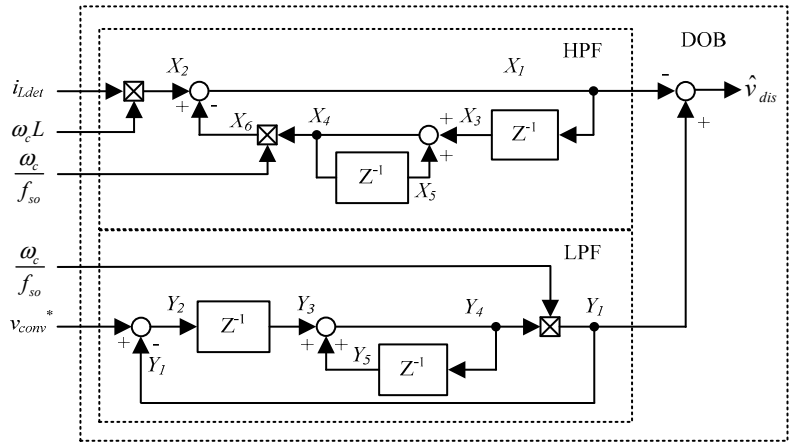


Fig. 4. Module block diagram of disturbance observer in FPGA. The disturbance observer is composed of the high pass filter and the low pass filter in FPGA. By implementing the disturbance observer in FPGA, the disturbance observer can operate faster to compensate for the disturbance. This enables the interconnected inductance is reduced without worsening THD of the output current.

term be X_1, and Y_1, respectively, (5) and (6) are obtained as follows;

$$X_1 = \omega_c L i_{Ldet} - \frac{\omega_c}{s} X_1 \tag{5}$$

$$Y_1 = \frac{\omega_c}{s}\left(v_{conv}{}^* - Y_1\right) \tag{6}$$

Applied the bilinear transformation into (5) and (6), (7) and (8) are obtained as follows;

$$X_1 = \omega_c L i_{Ldet} - \frac{\frac{\omega_c}{f_{so}} z^{-1}}{1 - z^{-1}} X_1 \tag{7}$$

$$Y_1 = \frac{\frac{\omega_c}{f_{so}} z^{-1}}{1 - z^{-1}}\left(v_{conv}{}^* - Y_1\right) \tag{8}$$

where, f_{so} is the sampling frequency of the disturbance observer. The disturbance observer is implemented by using (7) and (8).

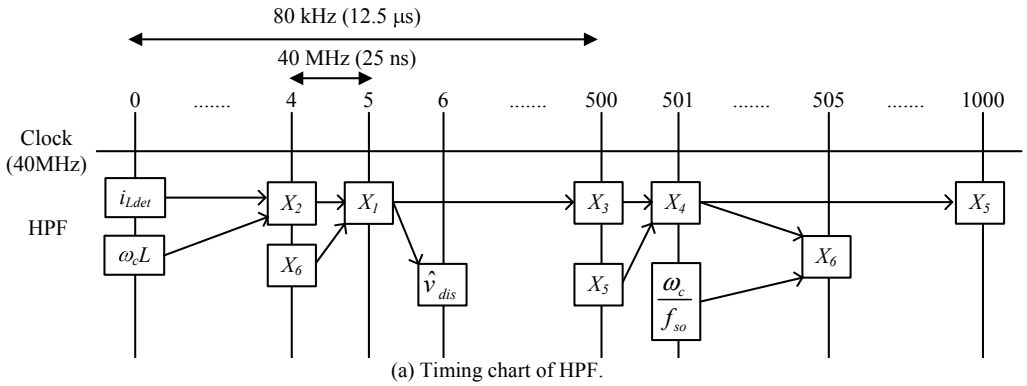
Fig. 4 shows the module block diagram of the disturbance observer that is implemented in FPGA. The disturbance observer is composed of the HPF and the LPF. The voltage between both the ends of interconnected inductor is estimated by inputting the detected current of the interconnected inductor i_{Ldet} to the HPF. The voltage command $v_{conv}{}^*$ is input to the LPF. The disturbance estimation voltage $\hat{v}_{dis}$ is calculated by subtracting the output of the HPF to output of the LPF.

The HPF is composed by a multiplier, an adder and a subtractor. X_2 is derived by multiplying the detected current of the interconnected inductor i_{Ldet} and the gain $\omega_c L$. The output of the HPF is derived by subtracting X_6 to X_2. X_3 is one-sampling period-delayed value of X_1. X_5 is one-sampling period-delayed value from the output of the adder X_4. The adding X_5 to X_3 realizes the integration. X_6 is obtained by multiplying the integrated value X_4 to the gain ω_c/f_{so}. X_6 shows the value of that X_1 is integrated in one sampling time of the disturbance observer $1/f_{so}$. On the other hand, the LPF is also composed by a multiplier, an adder and a subtractor. Y_2 is derived by subtracting the output of LPF Y_1 to the input of LPF $v_{conv}{}^*$. Y_3 is one-sampling period-delayed value of Y_2. Y_4 is obtained by adding Y_5 to Y_3. Y_5 is one-sampling period-delayed value of Y_4. The output of the LPF Y_1 is obtained by multiplying Y_4 to the gain ω_c/f_{so}. According to the above results, the disturbance estimation voltage $\hat{v}_{dis}$ is derived by subtracting the output of the HPF X_1 to the output of the LPF Y_1.

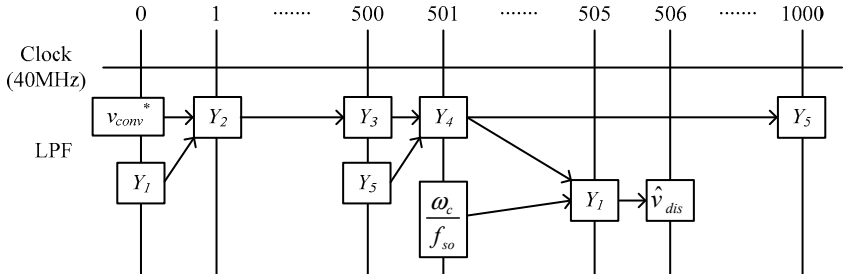
Fig. 5 shows the timing chart of the HPF and the LPF in FPGA controller. In the HPF, the multiplying result of X_2 is outputted with the delay of about 100 ns from the detected current of the interconnected inductor i_{Ldet}. The subtracting result X_1 is outputted after one clock. Note that, one clock equals 25 ns. X_3 is one-sampling period-delayed value of X_1. The adding result X_4 is outputted after one clock, whereas the multiplying result X_6 is outputted with the delay of about 100 ns from X_4. On the other hand, in the LPF, the subtracting result Y_2 is outputted after one clock. Y_3 is outputted with delay of one-sampling from Y_2. The adding result Y_4 is output after one clock. Y_5 is outputted with delay of one-sampling from Y_4. The multiplying result Y_1 is outputted with delay of about 100 ns from Y_4. Finally, the subtracting result $\hat{v}_{dis}$ is outputted after one clock. According to the above timing, the disturbance observer is operated in FPGA.

III. Simulation Result

Table 1 shows the simulation conditions. In this simulation, both the switching frequency f_{sw} and the sampling frequency of the disturbance observer f_{so} are 100 kHz, whereas the sampling frequency of the current controller f_{samp} and the cutoff frequency of the disturbance observer fc are 20 kHz.



(a) Timing chart of HPF.



(b) Timing chart of LPF.

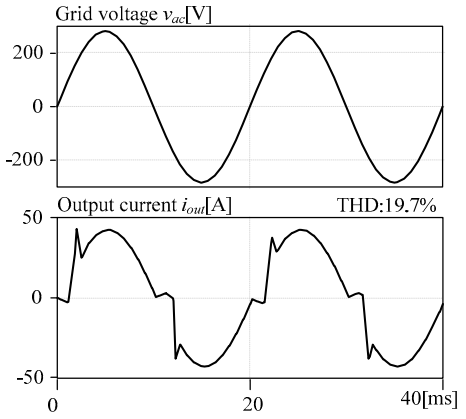
Fig. 5. Timing chart of FPGA controller. According to the above timing, the high-speed disturbance observer is achieved by FPGA.

TABLE. I SIMULATION CONDITION.

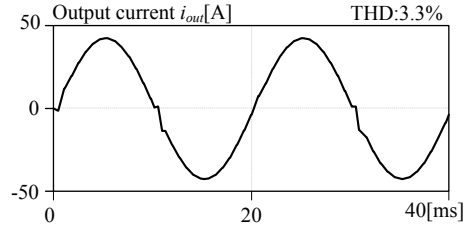
Output power	P_{out}	6 kW	Switching fre.	f_{sw}	100 kHz
DC link vol.	V_{dc}	380 V	Ang. fre. of ACR	ω_n	6000 rad/s
Grid voltage	v_{ac}	200 V_{rms}	Samp. fre. of ACR	f_{samp}	20 kHz
Dead-time	T_d	1.0 μs	Samp. fre. of DOB	f_{so}	100 kHz
Inter. Induc. (%Z)	L	106 μH (0.5%)	Cutoff fre. of DOB	f_c	20 kHz
			CT Delay time	T_{delay}	3 μs

Fig. 6 shows the simulation result of the output current when the conventional and proposed disturbance compensation method are applied. From Fig. 6, it is confirmed that THD of the output current with the conventional and proposed disturbance compensation method are 19.7% and 3.3%, respectively. Thus, it is confirmed that THD of the output current is improved by 83.2% by the proposed disturbance compensation method.

Fig. 7 shows the relationship between THD of the inverter output current and the output power. When the detection delay T_{delay} is 3 μs, THD of the output current with the conventional disturbance compensation method becomes worse. On the other hand, in the proposed disturbance compensation method, because the disturbance observer can estimate all the disturbances from the feedback output current, the disturbance due to the detection delay is suppressed. As a result, THD of the output current is maintained at low value even when the detection delay is introduced to the circuit. In particular, at light load of 0.2 p.u., THD of the output current is improved from 47% to 12% by the proposed disturbance compensation method. These results confirm that the proposed disturbance compensation method using the disturbance observer compensates the dead-time error voltage, even when there is the detection delay. These simulation results verify the validity of the proposed disturbance compensation.



(a) Conventional method.



(b) Proposed method.

Fig. 6. Output current waveform with conventional and proposed disturbance compensation method. In the simulation result, THD of the output current is improved by 83.2% by the proposed disturbance compensation method.

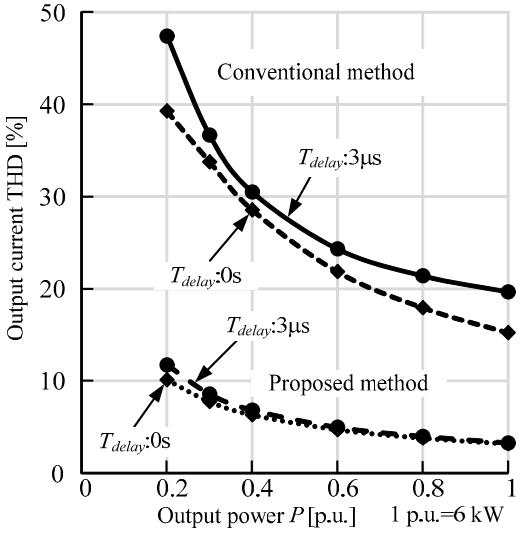


Fig. 7. Inverter output current THD versus Output power characteristics. At the load range from 0.2 p.u. to 1.0 p.u., THD of the output current is improved by the proposed disturbance compensation method.

IV. Experimental Result

A. Evaluation of inverter output current THD

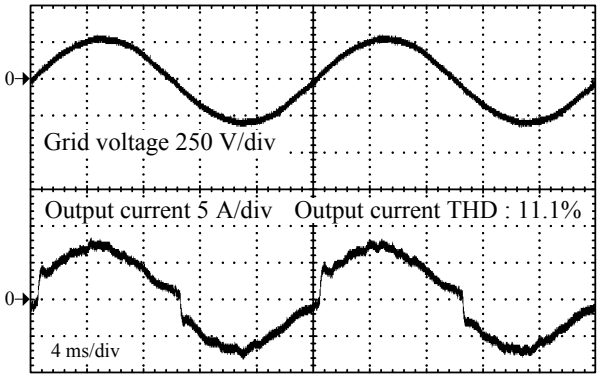
Table 2 shows the experimental conditions. Similarly, in the experiment, THD of the output current is compared when the conventional and proposed disturbance compensation method is applied.

Fig. 8 depicts the experimental result of the output current when the conventional and proposed disturbance compensation method are applied. At rated load, THD of the inverter output current is improved from 11.1% to 2.9% by applying the proposed disturbance compensation method at the disturbance-observer cutoff frequency of 2 kHz. A high distortion occurs at the zero crossing of the inverter output current in the conventional disturbance compensation method. This distortion occurs due to the detection delay of the output current polarity. On the other hand, even when there is the detection delay, the proposed disturbance compensation method using the disturbance observer can compensate the disturbance voltage. As a result, the distortion due to the dead-time error is reduced significantly. In addition, when the cutoff frequency of the disturbance observer is higher, the effect of the proposed disturbance compensation is larger. Because, by increasing the cutoff frequency of the disturbance, the control bandwidth of the disturbance observer is increased which enable to compensate for the disturbance faster. Therefore, the current control system achieved the high disturbance suppression performance using the disturbance observer with the high cutoff frequency, which can be implemented simply by the FPGA.

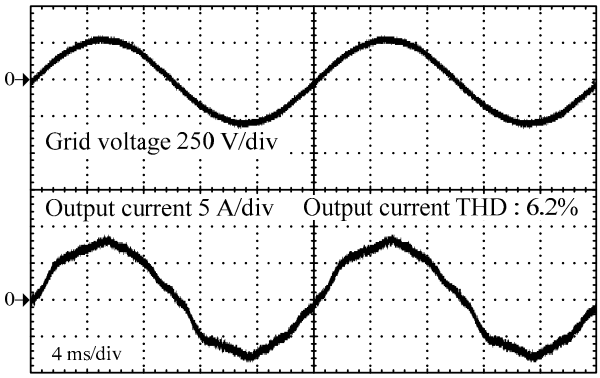
Fig. 9 shows the experimental result of the output current when the conventional and proposed disturbance compensation method are applied at light load. THD of the inverter output current is improved from 44.0% to 14.0% by applying the proposed disturbance compensation method. A high distortion in the waveform of the conventional method occurs. This

TABLE II Experimental condition.

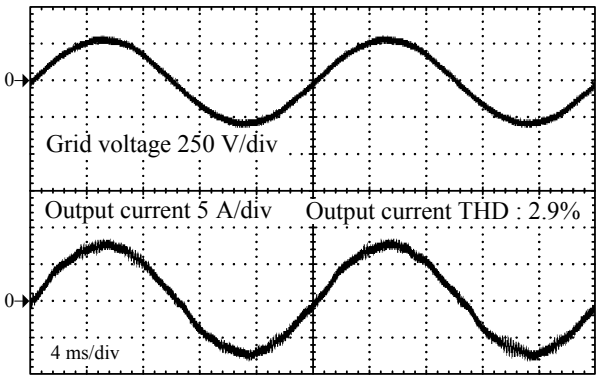
Output power	P_{out}	1 kW	Switching fre.	f_{sw}	80 kHz
DC link vol.	V_{dc}	380 V	Ang. fre. of ACR	ω_n	4000 rad/s
Grid voltage	v_{ac}	200 V_{rms}	Samp. fre. of ACR	f_{samp}	20 kHz
Dead-time	T_d	1.0 μs	Samp. fre. of DOB	f_{so}	80 kHz
Inter. Induc. (%Z)	L	636 μH (0.5%)	Cutoff fre. of DOB	f_c	2 kHz
			CT Delay time	T_{delay}	< 3 μs



(a) Conventional disturbance compensation method.

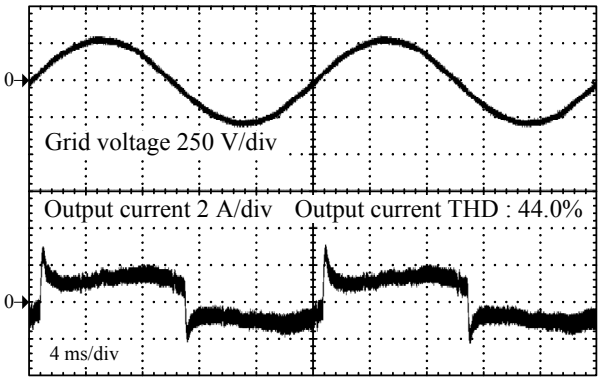


(b) Proposed disturbance compensation method at the disturbance-observer cutoff frequency of 1 kHz.

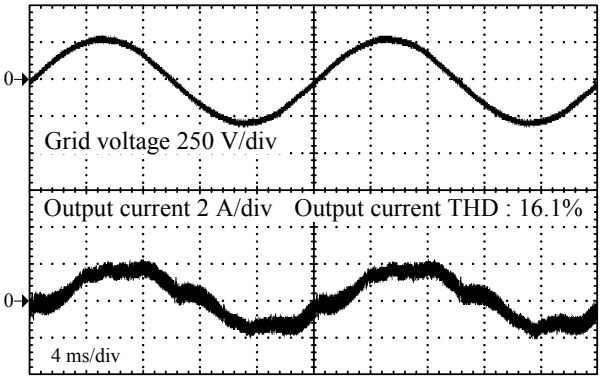


(c) Proposed disturbance compensation method at the disturbance-observer cutoff frequency of 2 kHz.

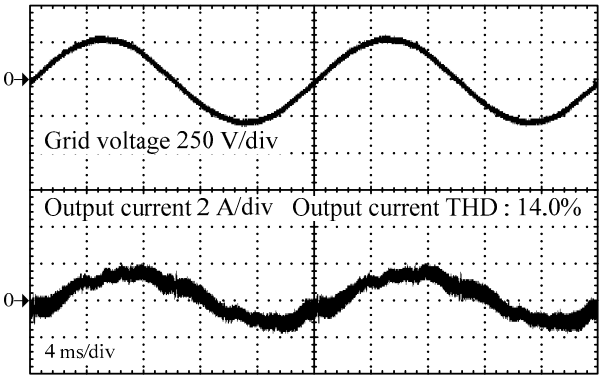
Fig. 8. Output current waveform in conventional and proposed disturbance compensation method at rated load of 1 kW. THD of the output current is improved by74.0% by using the proposed method.



(a) Conventional disturbance compensation method.



(b) Proposed disturbance compensation method at the disturbance-observer cutoff frequency of 1 kHz.



(c) Proposed disturbance compensation method at the disturbance-observer cutoff frequency of 2 kHz.

Fig. 9. Output current waveform in conventional and proposed method at light load of 100 W. THD of the output current is improved by 68.2% by using the proposed method.

distortion occurs because the effective value of the fundamental wave is small whereas the disturbance value such as the dead-time voltage error remains almost constant. Therefore, the compensation value of the conventional method is greatly influenced by the fundamental wave at the light load. On the other hand, the proposed disturbance compensation method using the disturbance observer decrease greatly the distortion of the inverter output current at the light load. Because, the proposed method estimated the disturbance voltage by the inverter output current.

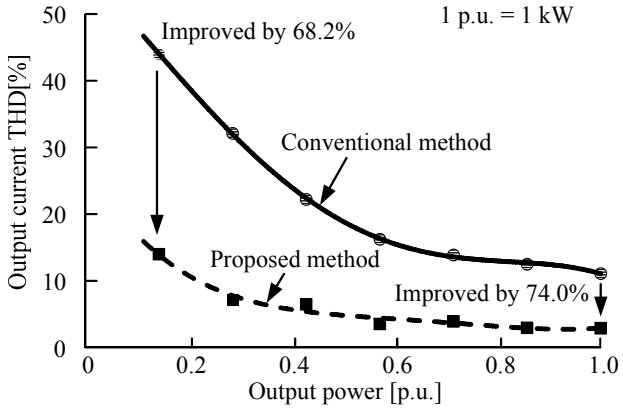


Fig. 10. Experimental characteristic of inverter output current THD versus output power. At the load range from 0.1 p.u. to 1.0 p.u., THD of the output current is improved over 68.2% by using the proposed disturbance observer.

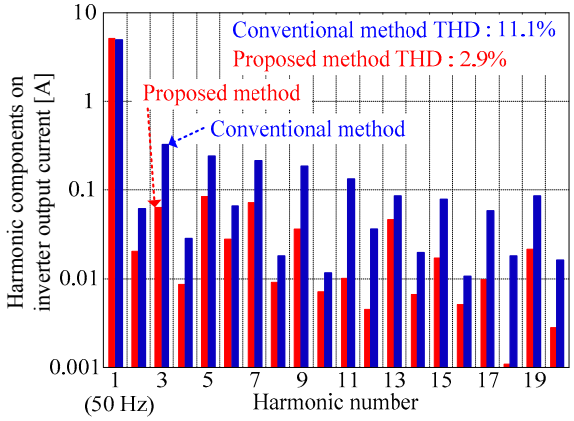
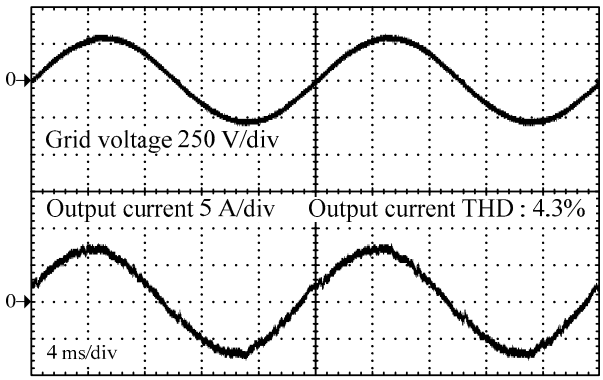


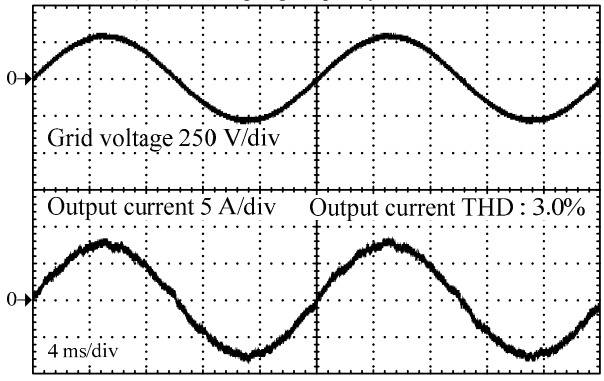
Fig. 11. Harmonic analysis. The high-frequency components of the inverter output current are reduced by using the disturbance observer.

Fig. 10 shows the relationship between THD of the inverter output current and the output power. From Fig. 10, it is confirmed that the proposed disturbance compensation method reduces THD of the output current effectively compared with that of the conventional disturbance compensation method in the load range from 0.1 p.u. to 1.0 p.u.. In particular, by applying the proposed disturbance compensation method, THD of the output current is reduced by 68.2% and 74.0% at load of 0.1 p.u. and 1 p.u., respectively. These results verify the validity and effectiveness of the proposed disturbance compensation method.

Fig. 11 shows the Fast Fourier Transform (FFT) analysis of the output current at rated load. In the FFT analysis, the frequency components from the fundamental wave of 50 Hz to 20th orders of the fundamental wave are shown. In Fig. 11, the high frequency components of the inverter output current is reduced by using the disturbance observer. Thus, the inverter-output-current distortion by the dead-time error voltage is reduced greatly. As a conclusion, even with the small inductance, the low THD of the output current can still be achieved by using the proposed disturbance observer which is implemented by FPGA.

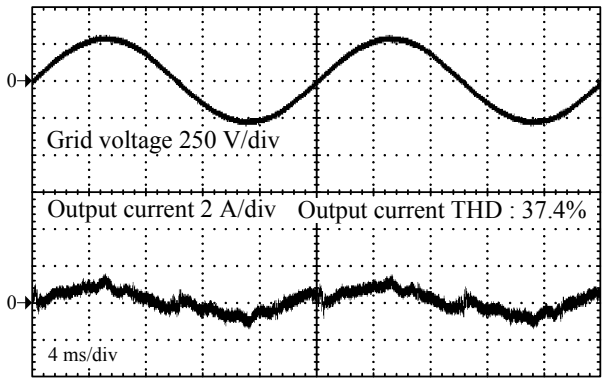


(a) DOB sampling frequency of 20 kHz.

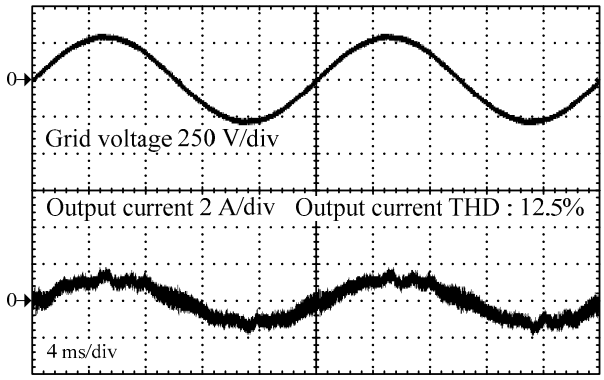


(b) DOB sampling frequency of 40 kHz.

Fig. 12. Output current waveform in proposed method by increasing sampling frequency at rated load. When the sampling frequency of the disturbance observer is changed from 20 kHz to 40 kHz, THD of the inverter output current is improved by 30.2%.



(a) DOB sampling frequency of 20 kHz.



(b) DOB sampling frequency of 40 kHz.

Fig. 13. Output current waveform in proposed method by increased sampling frequency at light load. When the sampling frequency of the disturbance observer is changed from 20 kHz to 40 kHz, THD of the inverter output current is improved by 66.6%.

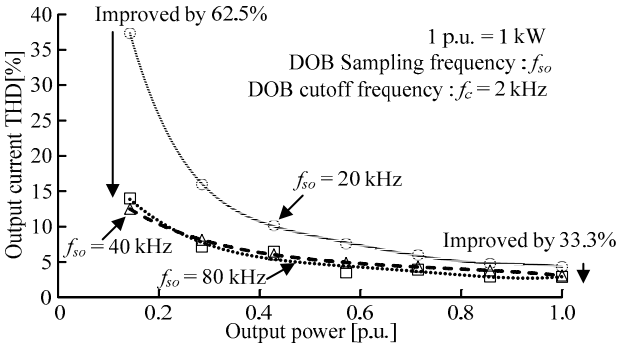


Fig. 14. Experimental characteristic of inverter output current THD versus output power with different sampling frequency. When the sampling frequency of the disturbance observer is increased from 20 kHz to 80 kHz, THD of the output current is reduced by 33.3% and 62.5% at load of 0.1 p.u. and 1 p.u., respectively.

B. Evaluation of disturbance-observer sampling frequency

Fig. 12 shows the inverter output current waveform with different disturbance-observer sampling frequencies at rated load. Note that the cutoff frequency of the disturbance observer is 2 kHz. In Fig. 12 (a), when the sampling frequency of the disturbance observer is 20 kHz, THD of the inverter output current is 4.3%. In Fig. 12 (b), when the sampling frequency of the disturbance observer is 40 kHz, THD of the inverter output current is 3.0%. Thus, when the sampling frequency of the disturbance observer is changed from 20 kHz to 40 kHz, THD of the inverter output current is improved by 30.2%. The higher the disturbance-observer sampling frequency becomes, the more THD of the inverter output current is improved. This is because the disturbance observer is possible to compensate the disturbance at high speed. As a conclusion, the high sampling frequency of the disturbance observer is possible to increase the disturbance suppression performance of the current control system.

Fig. 13 shows the inverter output current waveform with different disturbance-observer sampling frequencies at light load of 0.1 p.u.. In addition, the cutoff frequency of the disturbance observer is 2 kHz. In Fig. 13 (a), when the sampling frequency of the disturbance observer is 20 kHz, THD of the inverter output current is 37.4%. In Fig. 13 (b), when the sampling frequency of the disturbance observer is 40 kHz, THD of the inverter output current is 12.5%. Thus, when the sampling frequency of the disturbance observer is changed from 20 kHz to 40 kHz, THD of the inverter output current is improved by 66.6%. Therefore, it is concluded that even at light load, THD of the inverter output current is still improved when the sampling frequency of the disturbance observer is increased.

Fig. 14 shows the relationship between THD of the inverter output current and the output power, when the sampling frequency of the disturbance observer is 80 kHz, 40 kHz and 20 kHz, respectively. From Fig. 14, it is confirmed that THD of

the inverter output current is reduced in the load range from 0.1 p.u. to 1.0 p.u. at most when the sampling frequency of the disturbance observer is 80 kHz. As an expected result, with the high disturbance-observer sampling frequency, THD of the inverter output current is improved. When the sampling frequency of the disturbance observer is increased from 20 kHz to 80 kHz, THD of the inverter output current is improved from 4.3% to 2.9% at rated load. THD of the output current is reduced by 33.3% and 62.5% at load of 0.1 p.u. and 1 p.u..

From Fig. 8 to Fig. 14, it is confirmed that THD of the inverter output current with reducing inductance of the interconnected inductor is improved by applying the disturbance observer. In addition, when the disturbance observer with high sampling frequency and high cutoff frequency is applied, THD of the inverter output current is improved greatly. Therefore, in order to reduce the inductance of the interconnected inductor, the concept where the high-performance disturbance observer is implemented by FPGA is proved to be effective.

V. CONCLUSION

In order to achieve the minimization of the interconnected inductor, this paper proposed the dead-time voltage error compensation with the high-performance disturbance observer implemented by FPGA. Even when the inductance is minimized to %Z of 0.5%, the high-performance disturbance observer suppressed effectively all the disturbance voltage such as the dead-time error voltage, and the drop voltage on the switching device. In the experimental verification with a 1-kW miniature prototype, the proposed method reduced THD of the inverter output current from 11.1% to 2.9% at the rated load. In addition, it was confirmed that increasing sampling frequency and cutoff frequency of the disturbance observer can further improve THD of the inverter output current.

Future works will be confirmed the operation of the proposed disturbance compensation at 6-kW load. In addition, the operation of Fault-Ride-Through (FRT) is also verified using the disturbance observer.

REFERENCES

[1] Nimrod Vázquez, Marco Rosas, Claudia Hernández, Eslí Vázquez, and Francisco Perez-Pinal, “A New Common-Mode Tranceformereless Photovoltaic Inverter” IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 62, NO. 10, 2015 pp. 6381-6391.

[2] Sachin Jain and Vivek Agarwal, “A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking” IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 22, NO. 5, 2007, pp 1928-1940.

[3] R. Peña-Alzola and M. Liserre,”LCL-Filter Design for Robust Active Damping in Grid-Connected Converters,” IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS, VOL. 10, NO. 4, 2014, pp. 2192-2203.

[4] R. Beres, X. Wang, F. Blaabjerg, M. Liserre, C. Bak, “A Review of Passive Power Filters for Three-Phase Grid Connected Voltage-Source Converters” IEEE Journal Emerging and Selected Topics in Power Electronics, 2015.

[5] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. New York: Springer-Verlag, 2001.

[6] S. G. Jeong and M. H. Park, “The Analysis and Compensation of Dead-time Effects in PWM Inverters” IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 38, NO. 2, 1991, pp. 108-114.

[7] K. Lee, T. M. Jahns, T. A. Lipo, V. Blasko and R. D. Lorenz, . “Observer-Based Control Methods for Combined Source-Voltage Harmonics and Unbalance Disturbances in PWM Voltage-Source Converters” IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 45, NO. 6, 2009, pp. 2010-2021.

[8] N. Hoffmann, M. Hempel, M. C. Harke and F. W. Fuchs, “Observer-based Grid Voltage Disturbance Rejection for Grid Connected Voltage Source PWM Converters with Line Side LCL filters” IEEE Energy Conversion Congress and Exposition (ECCE), 2012, pp. 69-76.

[9] T. Hoshino, J. Itoh, and T. Kaneko, “Dead-time Voltage Error Correction with Parallel Disturbance Observers for High Performance V/f Control” IEEE Industry Applications Conference, 2007. 42nd IAS Annual Meeting, pp. 2038-2044.

[10] Carl J. Kempf and Seiichi Kobayashi “Disturbance Observer and Feedforward Design for a High-Speed Direct-Drive Positioning Table” IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY, VOL. 7, NO. 5, 1999, pp 513-526

[11] Ena Ishii, Hiroaki Nishi and Kouhei Ohnishi, “Improvement of Performances in Bilateral Teleoperation by Using FPGA” IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 54, NO. 4, 2007, pp 1876-1884