Evaluation of Current Source Gate Drive Circuit Applied for High Frequency Converter

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***Abstract*— This paper investigates a switching operation when a current source gate drive circuit with energy cycling is used. The current source gate drive circuit consists of a voltage source, an input inductor and switching devices as an H-bridge inverter. The power consumption of the current source gate drive circuit is reduced to compared with that of a conventional voltage source gate drive circuit because the energy of the capacitor between a gate and a source is not consumed in a gate resistance which is not required for the current source gate drive circuit. The switching operation of the proposed current source gate drive circuit in the high frequency inverter is evaluated in experiment. In addition, the power consumption is measured when the switching frequency is changed from 100 kHz to 1 MHz. As a result, it is confirmed that the power consumption of the current source gate drive circuit with energy cycling is reduced by 26% compared with that of the voltage source gate drive circuit at 1 MHz. In addition, the differential configuration of the current source gate drive circuit is considered in order to actualize the regenerating energy. Consequently, the regenerating energy of the inductor and the capacitance between a gate and a source is confirmed on the proposed current source gate drive circuit in simulation.**

Keywords—voltage sourcve; current source; high frequency switching; gate drive circuit

I. INTRODUCTION

SiC-MOSFETs have especially advantages which are characteristics of the high frequency switching and the low loss in compared with conventional Si-MOSFETs[1-5]. However, the capacitance C_{gs} between a gate and source of SiC-MOSFET is larger than that of Si-MOSFETs[6]. Additionally, the capacitance C_{gs} is increased when the low on resistance R_{on} or the large rated current of Si and SiC-MOSFET is selected. Furthermore, the power consumption of the voltage source gate drive circuit is increased at the high switching frequency because the discharge and charge power of the capacitance C_{gs} is nearly equal to the power consumption in a gate resistance. As a result, the high frequency switching cannot be applied to the conventional voltage source gate drive circuit.

Therefore, gate drive circuits for the fast and low loss charging of the capacitance C_{gs} of the MOSFET between the gate and the source has been actively studied [7-9]. For example, the switching operation of the MOSFET is achieved using the resonance which the inductor is connected to the gate in series [7]. For this reason, the loss is reduced because the charging energy of the capacitance C_{gs} and the inductor are regenerated. As a result, the power consumption of the gate drive circuit is decreased. However, the rise and fall time of the gate voltage is limited by resonance frequency because the capacitance C_{gs} is charged by LC resonance.

On the other hand, the high frequency switching is realized using an inductor in the push-pull gate drive circuit[8]. Generally, the push-pull gate drive circuit uses a positive and a negative voltage source in order to charge the gate capacitance C_{gs}. However, the voltage source availability of the energy is low because that these voltage source are alternately used. In this method, the energy is charged for the inductor using auxiliary MOSFETs for the gate driving which is not contributed to the discharge and charge of the C_{gs} in a push-pull gate drive circuit. Then, the switching is achieved in order to suppress the surge voltage of the inductor on the gate voltage when the current to the inductor is blocked at the switching. However, the circuit configuration becomes complex because many additional components are required in this method. Moreover, the high frequency switching is achieved by connecting an auxiliary switch on the main circuit side[9]. The fall time of the MOSFET is normally decided by the load resistance of the main circuit and the output capacitance. Thus, it is difficult to increase the speed of the fall time by the gate drive circuit. The auxiliary switch is connected on the main circuit side in order to enable the high frequency switching because the discharge and charge of the output capacitance in the main MOSFET can be fast. However, the reconstruction of the main circuit configuration is necessary.

In this paper, the operation of the current source gate drive circuit with energy cycling is experimentally confirmed in order to solve the problems mentioned above. In addition, the current source gate drive circuit with energy regeneration is confirmed by simulation in order to decrease the power consumption. The high frequency switching is possible using the current source gate drive circuit with energy cycling to compare with the voltage source gate drive circuit because the limitation of gate current caused by the gate resistance is not necessary[10]. First, the operating principle of the conventional gate drive circuit and the current source gate drive circuit with energy cycling is explained. Secondly, the design method of the current source gate drive circuit with energy cycling is shown. Thirdly, the

operations of the current source gate drive circuit with energy cycling is confirmed by experiments in upper switching arm on the high frequency inverter at each switching frequency and some gate capacitance value. Additionally, the power consumption is compared between the conventional gate drive circuit and the current source gate drive circuit with energy cycling. Finally, the different configuration of the current source gate drive circuit is proposed in order to realize the regenerating energy of the capacitance C_{gs}. It is confirmed the regenerating operation on the current source gate drive circuit with regeneration in simulation. In addition, the power consumption is compared among three gate drive circuits.

II. TYPE OF THE GATE DRIVE CIRCUIT

A. Conventional gate drive circuit

Fig. 1 shows the circuit configuration of the voltage source gate drive circuit, Fig2 shows the switching patterns of the conventional gate drive circuit. The conventional gate drive circuit is actualized the positive voltage and the negative voltage of the gate voltage using the H-bridge circuit similar to Fig. 1. The switching speed of the main MOSFET is adjusted by the gate resistance R_g in the conventional gate drive circuit because this circuit configuration is equivalent to a discharge and a charge of a gate resistance R_g and a capacitance C_{gs}. However, all energy of charging to a capacitance C_{gs} become a loss. A loss of conventional gate drive circuit is calculated by Eq. (1).

$$P = \frac{1}{2} C_{gs} V_{gs}^{\ 2} \times 2 f_{sw} \quad \text{.....(1)}$$

where V_{gs} is the total peak to peak value of the gate voltage, f_{sw} is the switching frequency. In this equation, the switching frequency is two times because the discharge and charge of the gate capacitance is two period in the switching frequency.

Additionally, the current capacity of the auxiliary MOSFET for gate drive circuit is increased because the gate current is increased when the gate resistance R_g is small for achieving high *dv*/*dt* of the gate voltage. Hence, the switching speed is limited when the capacitance C_{gs} is large of the main MOSFET.

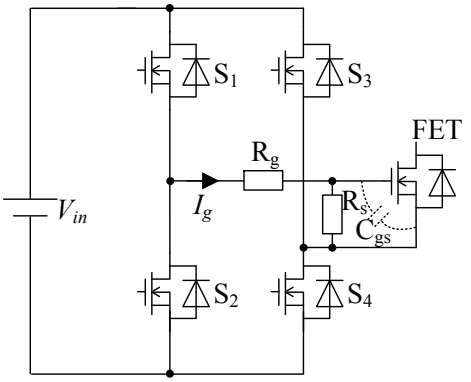

Fig. 1. Conventional gate drive circuit.

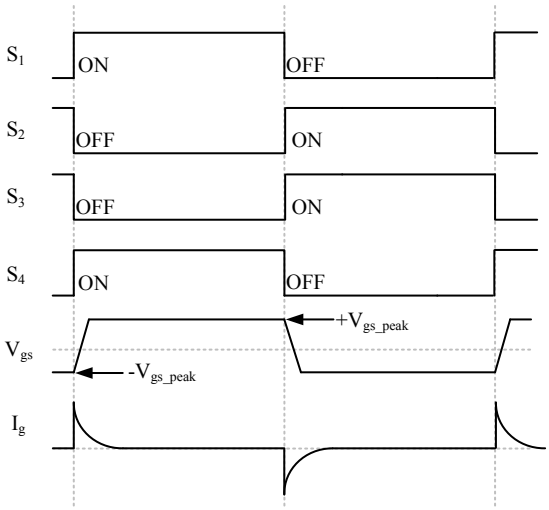

Fig. 2. Switching patterns of the conventional gate drive circuit.

B. Current source gate drive circuit with energy cycling type

Fig. 3 shows the current source gate drive circuit with energy cycling. This gate drive circuit configures the voltage source and the small input inductor L at the current source[6]. It is used for a transient LC resonance to charge and discharge the capacitance Cgs.

Fig. 4 shows the operation mode of the current source gate drive circuit. Normally, the energy of the capacitance C_{gs} is consumed by the gate resistance in the gate drive circuit. Consequently, the power consumption of the gate drive circuit becomes larger as the higher frequency. On the other hand, a transient LC resonance is used on the current source gate drive circuit. As a result, the power consumption becomes smaller than that of conventional voltage source gate drive circuit.

Fig. 5 shows the switching pattern of the current source gate drive circuit. The detail of the switching pattern is explained by using Fig. 3.

1) MODE I [$0 \le t \le T_i$] : S_1 and S_2 are turned on. The energy is charged to the input inductor L.

2) MODE II [$T_i \le t \le T_{ii}$] : S_4 is turned on. This period is the overlapping time for ensuring the inductor current path between MODE I and MODE III.

3) MODE III [$T_{ii} \le t \le T_{iii}$] : S_2 is turned off. The energy of the input inductor L is added to the DC power source. Then, the

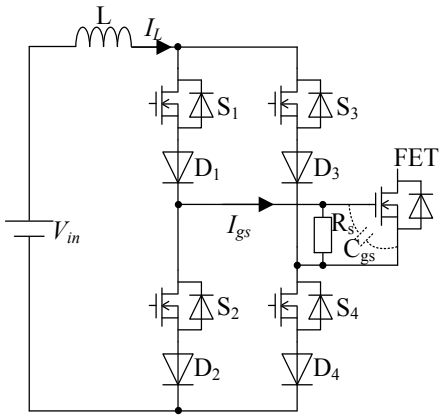

Fig. 3. Current source gate drive circuit.

capacitance C_{gs} is charged a positive voltage. In this operation mode, the input inductor current I_L becomes a sinusoidal waveform. When the gate voltage reaches the maximum value by a transient LC resonance, the gate voltage is kept a constant because the discharging of the capacitor C_{gs} is blocked by diodes.

III. Design Method of Gate Drive Circuit

Fig. 6 shows the flowchart for design of the current source gate drive circuit with energy cycling.

1) Deciding the voltage slope dV_{gs}/dt

First of the gate drive circuit designing, the MOSFET of main circuit is selected. In consequently, the switching specification is decided from the MOSFET. Parameters of other components is designed based on the voltage slope.

2) Designing the input inductor L

This gate drive circuit uses a transient LC resonance for gate driving at rise and fall timing. Therefore, the switching speed is adjusted up to the resonance frequency.

3) Calculation the gate voltage v_{gs}

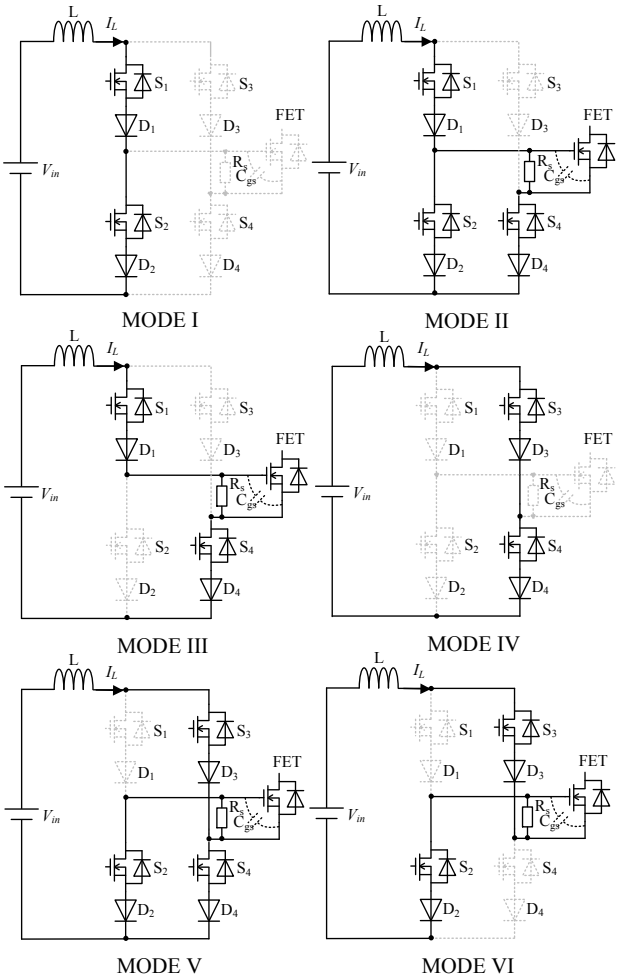

Fig. 4. Switching patterns of the current source gate drive circuit.

The rated gate voltage of the MOSFET is decided when the MOSFET of main circuit is selected. It is necessary to redesign the input inductor L if the calculation result is over the rated gate voltage of the MOSFET.

4) Calculation the input current i_{in}

The calculation of the input current i_{in} is necessary to select the MOSFET for the gate driving. If it is difficult to select the MOSFET for gate driving from commercialized product, it is also necessary to redesign the input inductor L.

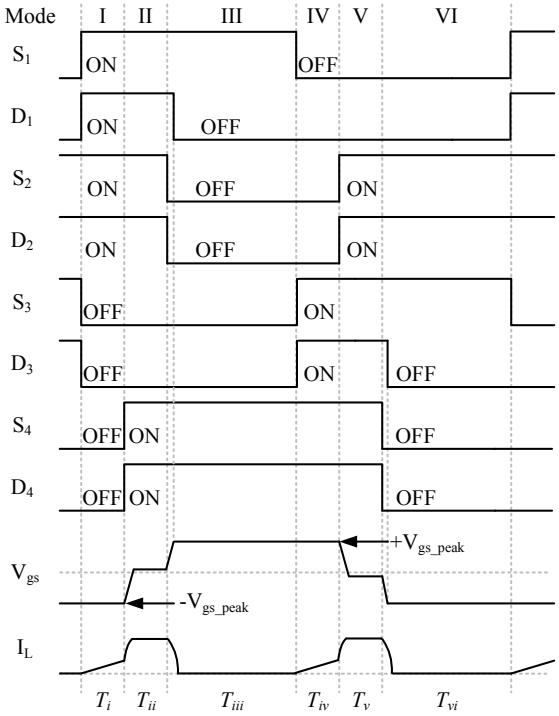

Fig. 5. Switching patterns and operation modes of the current source gate drive circuit.

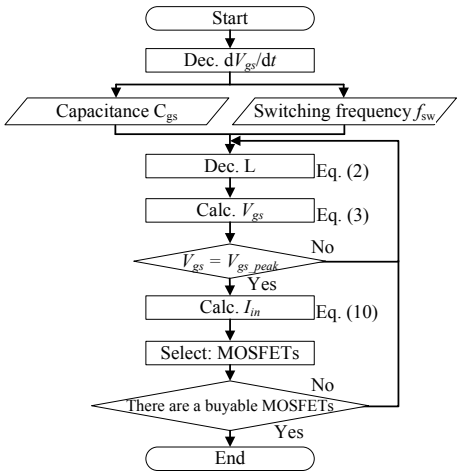

Fig. 6. Flowchart for design of the current source gate drive circuit.

These parameters is designed by this method without the overlapping time because it is negligible compared with the switching period.

A. Decided of the input inductor L

The input inductor L of the gate drive circuit is decided by the LC resonant frequency between input inductor L and the capacitance C_{gs}. The input inductor value is calculated by (2).

$$L = \frac{1}{4\pi^2 \alpha f_{sw} C_{gs}} \quad \text{.....(2)}$$

where f_{sw} is the switching frequency of the gate drive circuit. α is arbitrary constant. Besides, α is adjusted fast enough than that of the switching frequency f_{sw}.

B. Design of the gate voltage v_{gs}

Fig. 7 shows the equivalent circuit of the current source gate drive circuit. The gate voltage v_{gs} is given by (3) from the RLC equivalent circuit in Fig. 7.

$$v_{gs}(t) = \frac{1}{C_{gs}} \frac{e^{-\frac{R_{DS}}{L}t}}{(\frac{R_{DS}}{L})^2 + \omega^2} \left[\left\{ -(k_1 - i(0)k_2)\frac{R_{DS}}{L} + \omega i(0) \right\} \sin \omega t - \left\{ \omega(k_1 - i(0)k_2) + i(0)\frac{R_{DS}}{L} \right\} \cos \omega t \right] + \frac{k_3}{C_{gs}} \quad \text{.....(3)}$$

where L is the input inductor, R_{DS} is the on resistance of MOSFET for gate driving.

In addition, the vibrational angular frequency ω, initial current of input inductor $i(0)$ and coefficient k_1 to k_3 are expressed by (4)-(8).

$$\omega = \sqrt{\frac{1}{LC_{gs}} - \frac{(2R_{DS})^2}{4L^2}} \quad \text{.....(4)}$$

$$i(0) = \frac{(V_{in} - 2V_F)}{2R_{DS}}(1 - e^{-\frac{2R_{DS}}{L}T_i}) \quad \text{.....(5)}$$

$$k_1 = \frac{V_{in} - 2V_F - v_{gs}(0)}{\omega L} \quad \text{.....(6)}$$

$$k_2 = \frac{R_{DS}}{\omega L} \quad \text{.....(7)}$$

$$k_3 = v_{gs}(0)C_{gs} + \frac{\omega(k_1 - i(0)k_2) + i(0)\frac{R_{DS}}{L}}{\left(\frac{R_{DS}}{L}\right)^2 + \omega^2} \quad \text{.....(8)}$$

where T_i is the charging period of input inductor L on MODE I or MODE IV in Fig. 5.

Fig. 8 shows the gate voltage vibration expressed by (3). The gate voltage of current source gate drive circuit is vibrated similar to sinusoidal waveform due to a LC resonance. Moreover, the gate voltage attenuates with time because the current gate drive circuit has resistance components of the MOSFET for gate driving. However, the gate voltage is clamped to the peak voltage value when the gate voltage is increased at initial motion. It is because the diode is connected in series. Therefore, the input inductor L is designed for that the peak value of gate voltage becomes desired value. The time of arriving to the gate voltage peak value t_{Vgs_peak} is given by (9).

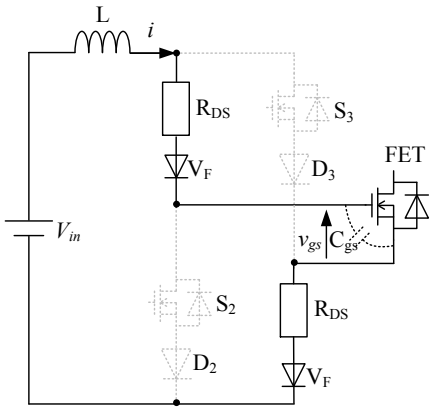

Fig. 7. Equivalent circuit of current source gate drive circuit.

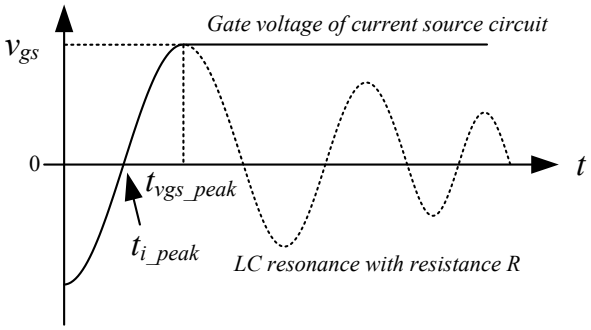

Fig. 8. Gate voltage of current source gate drive circuit.

$$t_{v_{gs\_peak}} = \frac{1}{\omega} Tan^{-1}\left\{ -\frac{i(0)}{k_1 - i(0)k_2} \right\} + \frac{\pi}{\omega} \quad \text{.....(9)}$$

C. Select of the MOSFET for gate drive circuit

The input inductor current is calculated after the input inductor value is decided. The specification of the MOSFET for driving is determined from the calculation result of the input inductor current. The input inductor current value is expressed by (9) from transient response of equivalent circuit in Fig. 5.

$$i_{in}(t) = \frac{V_{in} - 2V_F - V_{gs}(0)}{\omega L} e^{-\frac{R_{DS}}{L}t} \sin \omega t + i(0) e^{-\frac{R_{DS}}{L}t} \left(i(0) \cos \omega t - \frac{R_{DS}}{\omega L} \sin \omega t \right) \quad \text{..(10)}$$

where T_i is the charging period of input inductor similar to (5).

The charging period of input inductor T_i is adjusted shorter than the switching period T_{sw} of the MOSFET for main circuit. Thus, the charging period T_i is set to 25 ns because 5% of the half cycle of the maximum switching frequency 1 MHz is considered in this paper. The MOSFET for gate driving which have rated pulse drain current in order to satisfy the maximum input inductor current is calculated by (8). The time of arriving to the maximum pulse drain current t_{i_peak} is given by (11).

$$t_{i\_peak} = \frac{1}{\omega} Tan^{-1}\left\{ \frac{\omega\left(k_1 - i(0)k_2\right) - \frac{R_{DS}}{L} i(0)}{\frac{R_{DS}}{L}\left(k_1 - i(0)k_2\right) + \omega i(0)} \right\} \quad \ldots (11)$$

IV. Experimental results

Fig. 9 shows the circuit diagram of the high frequency inverter using the current source gate drive circuit with energy cycling type, Table. 1 shows the detail of the experimental condition in Fig. 9. The current source gate drive circuit is connected one by one to each main MOSFET of the high frequency inverter. Furthermore, the current source gate drive circuit in Fig. 3 is used.

A. Switching operation at high frequency

Fig. 10 shows the experimental results of the switching operation on the high frequency inverter at the switching frequency of 100 kHz. It is confirmed that the MOSFET of the upper arm is switching in Fig. 10. However, the gate voltage of the waveforms is vibrated when the current source gate drive circuit is used. This reason is resonance between the capacitance C_{gs} and the parasitic inductance of the wiring from the main MOSFET to the gate drive circuit after the charging of the capacitance C_{gs} is finished. Although, it is not a problem because the voltage of the vibration in the gate voltage is the outside range which is higher and lower than the threshold voltage of the main MOSFET.

Fig. 11 shows the measurement waveform of the high frequency inverter at the switching frequency of 1 MHz. The switching operation of the upper arm MOSFET is also confirmed in Fig. 11. However, the gate voltage have a ringing at rise timing. This reason is similar to the switching frequency of 100 kHz. From results of Fig. 10 and Fig. 11, the high frequency switching of the upper arm MOSFET is realized using the current source gated drive circuit.

Fig. 12 shows the magnifying of the gate voltage waveform when the switching frequency are 100 kHz and 1 MHz. It is

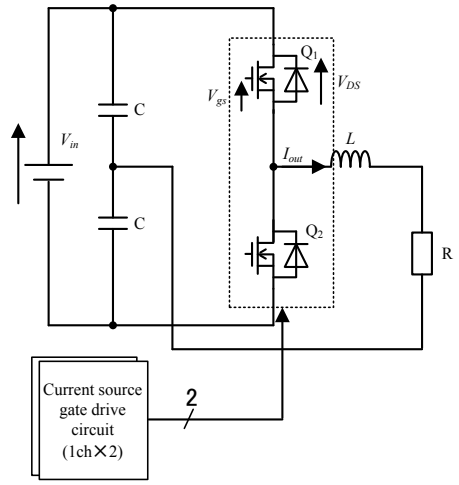

Fig. 9. Experimental circuit diagram.

Table. 1. Experimental condition.

Main circuit	Input voltage V_{in}	48 V
	Input capacitance C	5 μF
	Lode reactor L	5 μH
	Lode resistance R	5 Ω
	Gate voltage V_{gs}	±12 V
Switching device for gate drive circuit	MOSFET:IRLML2060TRPbF(IR)	
	On resistance R_{DS}	0.48 Ω
Diode for gate drive circuit	RB161M-20TR(Rohm)	
	Forward Voltage V_F	0.32 V
Switching device for main circuit	MOSFET:IRF640NPbF(IR)	
	FET Gate capacitance C_{gs}	1670 pF

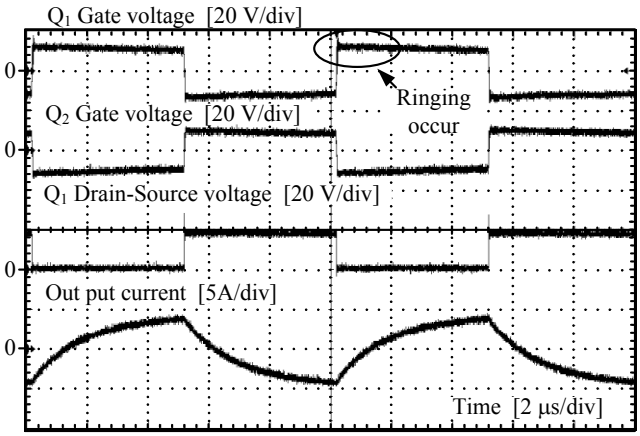

Fig. 10. Measurement waveform of the high frequency inverter using the current source gate drive circuit at 100kHz.

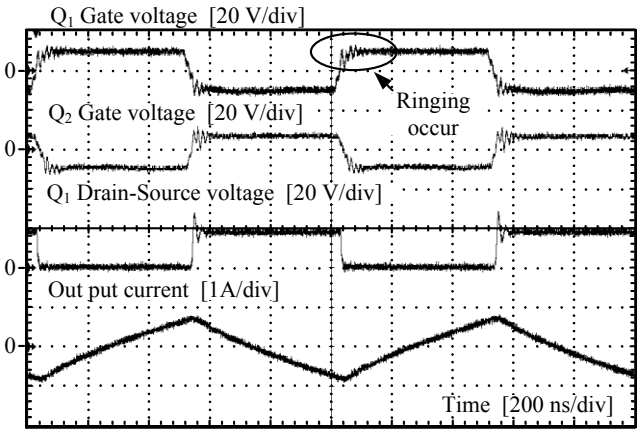

Fig. 11. Measurement waveform of the high frequency inverter using the current source gate drive circuit at 1 MHz.

confirmed the rise time is 37 ns when the switching frequency is 100 kHz. On the other hand, the rise time is 33 ns at the switching frequency of 1 MHz. The results of 100 kHz and 1 MHz are 0.4% and 3.7% when these rise time is considered in the one period of the switching frequency. However, the rise time of the measurement results are included 25 ns of the overlapping time. Therefore, the rise time of the gate voltage can be fast if the overlapping time is shorter than this condition.

B. Comparing of power consumption

Fig. 13 shows the experimental results of the power consumption in the current source gate drive circuit. In addition, the calculation results of the power consumption in the conventional gate drive circuit is shown in order to compare the current source gate drive circuit in Fig. 13. These power consumptions of two gate drive circuits are compared when the switching frequency is changed from 100 kHz to 1 MHz. The maximum input current and the maximum input inductor current are constant value of 4 A in the two gate drive circuits at designing.

The switching frequency is 100 kHz in Fig. 13, the power consumption of the current source gate drive circuit is 0.078 W, the power consumption of the conventional voltage source gate drive circuit is 0.096 W. It is considered the power consumption can be reduced by 18.8% using the current source gate drive circuit. Moreover, when the switching frequency is 1 MHz in Fig. 13, the power consumption of the current source gate drive circuit is 0.71 W, the power consumption of the conventional voltage source gate drive circuit is 0.96 W. As a result, it is confirmed the power consumption of the gate drive circuit is reduced by 26.3 % when the current source gate drive circuit is used. Therefore, the gate drive circuit of the current source gate drive circuit can reduce the power consumption when the switching frequency is high. It is due to the energy of the capacitance C_{gs} is cycled in the gate drive circuit when the reverse polarity voltage is input at the MODE III and MODE VI of the current source gate drive circuit. In consequently, low loss gate drive circuit is achieved by the current source gate drive circuit at the high frequency.

C. Problem of the kickback effect

The kickback effect occur on the gate voltage of the main MOSFET when the capacitance C_{gs} is low value because the current is flow in the gate drive circuit from the path of the capacitance between the drain and the gate C_{ds}. This problem is solved by connecting the capacitance to the capacitance C_{gs} in parallel using several methods. The gate voltage fluctuation suppressed due to flow in the current from the capacitance C_{ds}. However, the power consumption of the gate drive circuit because the capacitance C_{gs} is increased. Therefore the current source gate drive circuit is designed based on the each gate capacitance C_{gs}. In addition, the operation of the switching is measured.

Fig. 14 shows the switching operation when the capacitance C_{gs} is 3000 pF. The ringing of the gate voltage is reduced compared with Fig. 11. It is because the resonance frequency between the capacitance C_{gs} and the parasitic inductance of the wiring from the main MOSFET to the gate drive circuit become

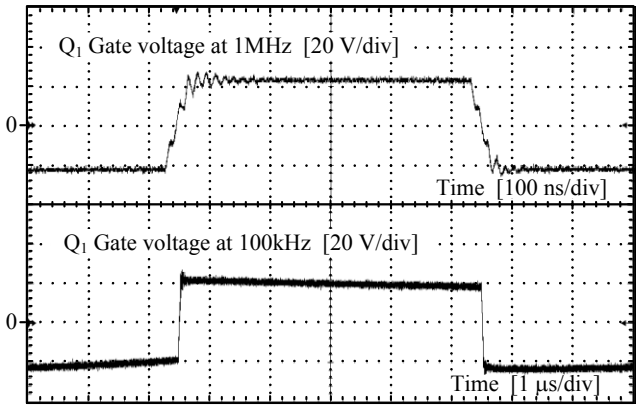

Fig. 12. Magnifying the waveform of the gate voltage at 100kHz and 1MHz

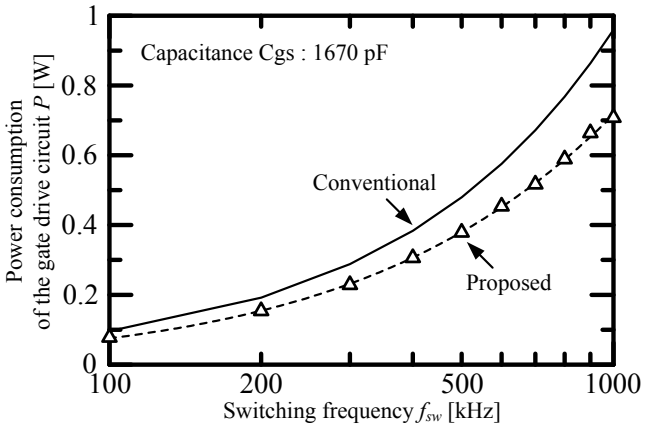

Fig. 13. Comparison of power consumption between two gate drive circuits.

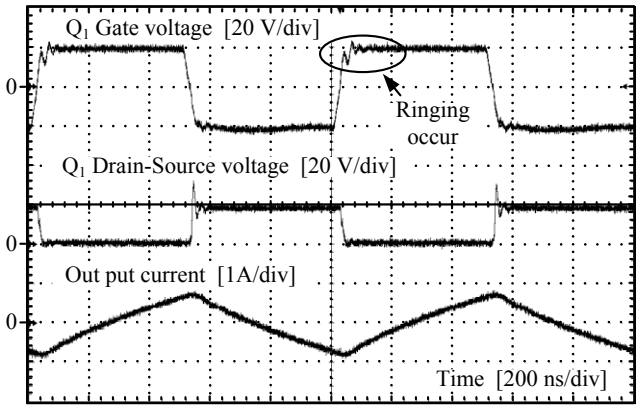

Fig. 14. Measurement waveform of the high frequency inverter using the current source gate drive circuit at 3000pF.

low. Additionally, the kickback effect is suppressed because the capacitance C_{gs} is increased.

Fig. 15 shows the measurement waveform of the switching operation when the capacitance C_{gs} is 5000 pF. As a result, the ringing of the gate voltage is suppressed compared with Fig. 11

and Fig. 14. Besides, the high frequency switching of the main MOSFET is achieved because the rise time of the gate voltage is similar to Fig. 11 and Fig. 14. In consequence, the high frequency switching of the main MOSFET is achieved regardless of the capacitance C_{gs} value.

V. Regenerated Current Source Gate Drive Circuit

A. Operation mode of proposed gate drive circuit

Fig. 16 shows the proposed current source gate drive circuit. In proposed gate drive circuit, components are similar to the current source gate drive circuit with energy cycling. The power consumption of the current source gate drive circuit with energy cycling is reduced than that of the voltage source gate drive circuit. However, energy of the inductor L and the capacitance C_{gs} cannot regenerate to the DC power source because diodes are used for blocking the short path in the gate drive circuit. The power consumption is more reduced if the regenerating of the inductor L and the capacitance C_{gs} energy is actualized. Therefore, the proposed gate drive circuit uses only MOSFETs in order to regenerate energies of the inductor L and the capacitance C_{gs}.

Fig. 17 shows the operation mode of the proposed gate drive circuit. The proposed gate drive circuit has six modes.

1)MODE I : S_1,S_7 and S_8 are turned on. The energy of the inductor L is charged. The rise time of the gate voltage becomes fast when this mode period is long time.

2)MODE II : S_7 and S_8 are turned off, S_4 conducts. The capacitance C_{gs} is charged to a positive voltage. On the other hand, the charging energy of the capacitance C_{gs} in the previous mode is moved to the inductor L.

3)MODE III : All MOSFETs are turned off expect S_6. The energy of the inductor L is regenerated to the DC power source. In addition, the gate voltage is kept during this mode.

The operations of MODE IV-VI are similar to MODE I-III although the voltage polarity of the capacitance C_{gs} is opposite.

B. Simulation of the proposed gate drive circuit

Fig. 18 shows the simulation results of the proposed gate drive circuit at 1 MHz. It is confirmed the gate voltage is actualized -12 V and +12 V. Besides, the input average current is zero because the supplying energy of the DC power source is retrieved from the inductor L and the capacitance C_{gs}. As a result, the regeneration of the gate drive circuit is realized in simulation. However, the inductor current is not reduced because this simulation uses ideal components in MODE II and MODE V.

VI. Conclusion

In this paper, the validity of the current source gate drive circuit for high frequency switching converters is discussed. In consequence, it is confirmed the high frequency switching of the upper arm MOSFET is realized. In addition, the power consumption can be reduced by 26% at the switching frequency of 1 MHz compared with the voltage source gate drive circuit in the experimental results. Moreover, the high frequency switching of the main MOSFET is realized regardless of the

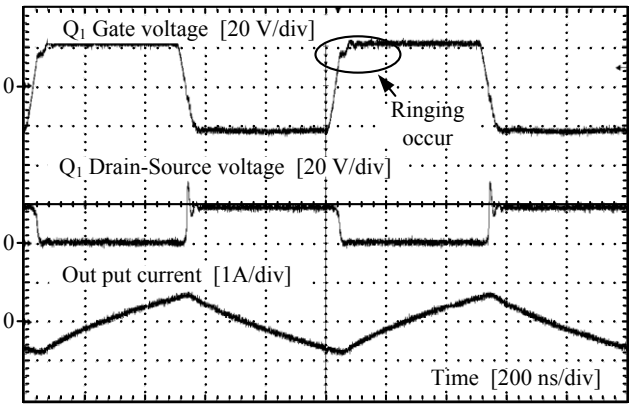

Fig. 15. Measurement waveform of the high frequency inverter using the current source gate drive circuit at 5000 pF.

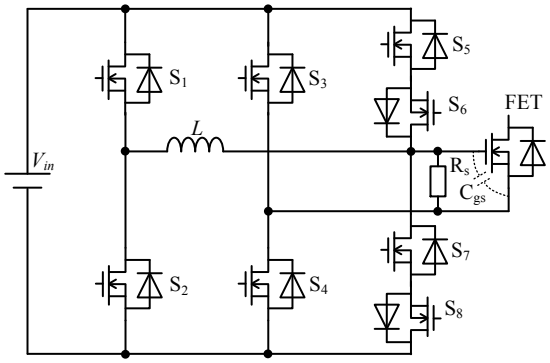

Fig. 16. Circuit diagram of proposed current source gate drive circuit.

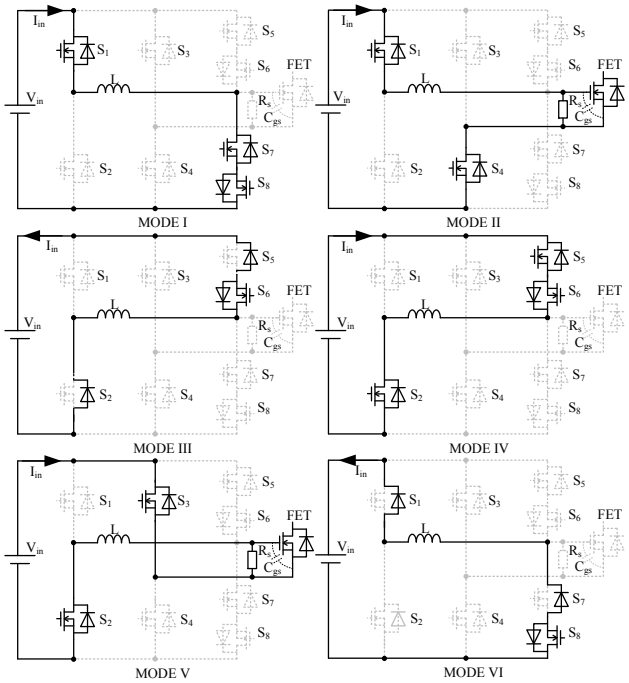

Fig. 17. Operation modes of the proposed gate drive circuit.

capacitance C_{gs} value. Besides, the differential configuration of the current source gate drive circuit is considered in order to actualize the regenerating energy. Consequently, the regenerating energy of the inductor and the capacitance C_{gs} is confirmed on the current source gate drive circuit with regeneration in simulation. In the future, the operation of the proposed current source gate drive circuit will be confirmed in experiment.

REFERENCES

[1] T. Kim, M. Jang, V.G. Agelidis : "Comparative Thermal Performance Evaluation of SiC MOSFETs and Si MOSFET for 1.2 kW 300 kHz DC-DC Boost Converter as a Solar PV Preregulator", The 2014 International Power Electronics Conference,No.21|4-5, pp3933-3937(2014)

[2] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. A. Hull, S. Allen, S. Bhattacharya : "High Switching Performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for Advanced Power Conversion Applications", IEEE Trans. On Power Electronics, Vol. 31, No. 7, pp. 4742-4754 (2016)

[3] S. Safari, A. Castellazzi, P. Wheeler : "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter", IEEE Trans. On Power Electronics, Vol. 29, No. 5, pp. 2584-2596 (2014)

[4] A. Vázquez, A. Rodríguez, M. Fernández, M. M. Hernando, E. Maset, J. Sebastián : "On the Use of Front-End Cascode Rectifiers Based on Normally On SiC JFET and Si MOSFET", IEEE Trans. On Power Electronics, Vol. 29, No. 5, pp. 2418-2427 (2014)

[5] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, A. Agarwal : "Characterization, Modeling, and Application of 10-kV SiC MOSFET", IEEE Transactions on Electron Devices, Vol. 55, No. 8, pp. 1798-1806 (2008)

[6] J. Jordan, V. Esteve, E. Sanchis-Kilders, E.J. Dede, E. Maset, J.B. Ejea, A. Ferreres : "A Comparative Performance Study of a 1200 V Si and SiC MOSFET Intrinsic Diode on an Induction Heating Inverter", IEEE Trans. On Power Electronics, Vol. 29, No. 5, pp. 2550-2562 (2014)

[7] H. Fujita : "A Resonant Gate-Drive Circuit Capable of High-Frequency and High-Efficiency Operation", IEEE Trans. On Power Electronics, Vol. 25, No. 4, pp. 962-969 (2010)

[8] T. Noguchi, S. Yajima, H. Komatsu : "Development of Gate Drive Circuit for Next-Generation Ultra High – Speed Switching Dvices", IEEJ Trans. On Industry Applications, Vol. 129, No. 1, pp. 46-52(2009)

[9] T. Noguchi, M. Mizuno : "High-Speed Switching Operation of MOSFETs Using Auxiliary Circuit Shorting Load", International Conf. Renewable Energy Research and Applications, pp. 1-6(2012)

[10] A. Sagehashi, K. Kusaka, K. Orikawa, J. Itoh : "Current source gate drive circuits with low power consumption for high frequency power converters", Power Electronics and ECCE Asia, Vol. , No. WeH1-1, pp. 1017-1024 (2015)

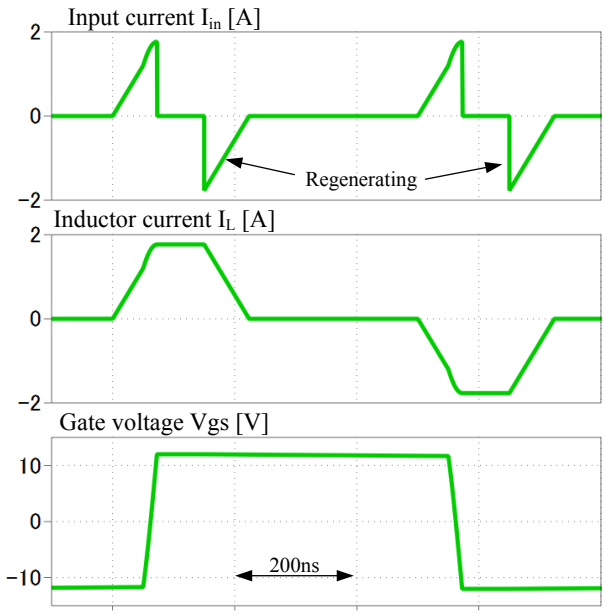

Fig. 18. Simulation results of the proposed gate drive circuit.