Comparison of Circuit Topologies for Active Power Decoupling toward High Power Density

Jun-ichi Itoh, Tomokazu Sakuraba, Keisuke Kusaka, Hiroki Watanabe and Keita Furukawa
Department of Electrical Engineering
Nagaoka University of Technology, NUT
Niigata, Japan
itoh@vos.nagaokaut.ac.jp, t_sakuraba@stn.nagaokaut.ac.jp

***Abstract*— This paper discusses how to achieve high power density with high efficiency for single-phase AC connected inverter with active or passive power decoupling circuit. An inverter connected to a single-phase grid requires a power decoupling device to compensate power pulsation with twice the grid frequency. As the alternative to an electrolytic capacitor connected to DC-link, active buffer circuits with bi-directional chopper and a flying capacitor converter (FCC) with power decoupling capability have been evaluated in terms of long lifetime. In this paper, Pareto optimization is used to compare the character of the power decoupling circuits in terms of an efficiency and a power density. The volume of capacitors in the FCC with ceramic capacitors can be reduced by 54.6% compared to bulky electrolytic capacitors. As a result, when the 400-V SiC-MOSFETs are used for the FCC at 25 kHz, a maximum power density of 5.3 kW/dm^3, which is 1.3 times higher than the power density of the passive topology, can be obtained. Furthermore, the total power loss is reduced by 10.5% in comparison with that of the conventional converter.**

Keywords— single-phase inverter, power ripple compensation, power density design

I. INTRODUCTION

In recent years, single-phase grid connected converters have been studied actively as the power conversion systems (PCSs) for photovoltaics systems or battery energy storage systems and so on. Instantaneous power of the single-phase grid oscillates at twice the grid frequency whereas the output power is constant. As a result, a power ripple with twice the grid frequency occurs at the connection point between the chopper and the inverter. In order to absorb this power ripple, bulky electrolytic capacitors are used in conventional circuits. However, the electrolytic capacitor limits the lifetime and size reduction of the PCS.

As an alternative power decoupling method, an active power decoupling which consists of small capacitors, inductors and switching devices has been proposed [1-3]. As a result, the PCS with long lifetime is expected by using film capacitors or ceramic capacitors as the buffer capacitor. However, an additional inductor and switching devices for the buffer circuit are required to control the buffer capacitor voltage. By increasing the switching frequency of the active buffer circuit, the inductance can be reduced, however the size of the heatsink becomes larger due to increase of the switching loss. As a result, a relationship between the inductor volume and the heatsink volume indicates the trade-off characteristics. Thus, the buffer circuit should be designed and operated at an adequate switching frequency to maximize the power density. In [1] and [3], the ceramic capacitors are applied for the power decoupling circuit in order to achieve a high power density. In [2], the power loss mechanism is analyzed in order to improve the system efficiency of the active buffer circuit. However, past literatures have not clearly mentioned the conditions to achieve a higher efficiency and a power density than the electrolytic capacitor.

This paper clarify the conditions to achieve the higher power density and the higher efficiency by comparing among the electrolytic capacitor and the active power decoupling topologies. First, the design flow for the passive topology using the electrolytic capacitor and the active buffer topology [4-5] using the ceramic capacitor is introduced. Second, from the design flowchart and the specifications of the commercially available products, the power density and the efficiency of the active power decoupling circuit are evaluated by Pareto optimization. Finally, the comparisons of a total loss and a total volume at the maximum power density point are discussed in order to achieve a high efficiency and a high power density.

II. CIRCUIT CONFIGURATION AND DESIGN METHOD

A. Passive Power Decoupling Circuit

Fig. 1 shows the circuit configuration of the passive power decoupling method using an electrolytic capacitor. Table 1 shows the circuit specifications. This paper evaluates the volume of the buffer circuit based on the ripple current in the DC-link. In order to evaluate the ripple current, a power supply with an internal impedance R_{in} is considered to emulate the output of the boost chopper connected to PV.

In the passive topology, the bulky electrolytic capacitor is connected to absorb twice grid frequency. The ripple current restricts the lifetime of the electrolytic capacitor. Therefore, the electrolytic capacitor, which has the allowable ripple current higher than the calculated ripple current, is selected in this paper. The current which flows into the electrolytic capacitor includes not only the power ripple component but also the switching frequency component from the inverter. The

capacitor ripple current is the function of the output power factor and the modulation index, which is a nonlinear value [6]. Then, the effective value of the capacitor ripple current is expressed by

$$I_{rms\_cap} = K_{cap}(\phi, m) I_m \quad (1),$$

where, I_m is the maximum value of the output current, ϕ is the output power factor, m is the modulation index and $K_{cap}(\phi, m)$ is the coefficient regarding ripple current in the DC-link which is obtained by simulation.

Fig. 2 shows the value of $K_{cap}(\phi, m)$ which is obtained by the ration between the output current and the ripple current with circuit simulation as follows. In general, the output power factor of the grid-connected inverter is approximately unity. The modulation index, which expresses the ratio of the dc-link voltage V_{dc} and the maximum output voltage V_m, is 0.74 in this case. Therefore, from Fig.2, $K_{cap}(1, 0.74)$ is 0.56. With the frequency multipliers, the allowable ripple current is calculated by

$$I'_{rms\_cap} = \sqrt{\left(\frac{I_{100\,\mathrm{Hz}}}{K_{100\,\mathrm{Hz}}}\right)^2 + \left(\frac{1}{K_{sw}}\right)^2 \sum_{n=1}^{\infty} I_{nsw}^2} \quad (2),$$

where, $I_{100\mathrm{Hz}}$ is the effective current whose frequencies are twice the grid frequency, I_{nsw} is the effective current at the switching frequency, $K_{100\mathrm{Hz}}$ and K_{sw} are the frequency multipliers at 100 Hz and the switching frequency, respectively.

An electrolytic capacitor, which has the allowable ripple current higher than the result of (2), should be required.

B. Boost Type Active Buffer Circuit

Fig. 3 shows the circuit configuration of the boost type active buffer circuit. The active circuit consists of a boost chopper and a small capacitor C_{buf} to absorb the power ripple in DC-link. The active buffer circuit achieves long lifetime because the film capacitors or the ceramic capacitors are used as the buffer capacitor. The principle for the power decoupling between the DC and the AC sides is explained as follows.

Fig. 4 shows the relationship among the input power p_{in}, the output power p_{out} and the compensation power p_{buf} in the active buffer. The output instantaneous power is shown in (3) when the output current is the sinusoidal wave with unity power factor.

$$p_{out} = \frac{V_m I_m}{2}(1 - \cos 2\omega_{out} t) \quad (3),$$

where, V_m is the peak voltage of the single-phase grid and ω_{out} is the angular frequency of a grid. From (3), the twice grid frequency power ripple occurs in the DC-link. In order to absorb the power ripple, the instantaneous power p_{buf} in the active buffer is controlled according to

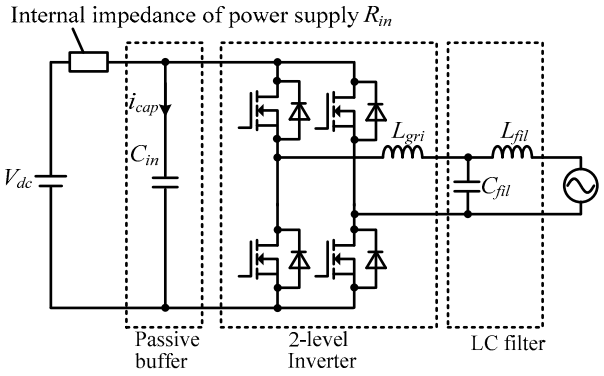


Fig. 1. Passive power decoupling circuit.

Table 1. System specification.

Parameter	Symbol	Value
Rated power	P_{out}	6 kW
Output voltage	V_{out}	200 V
Output frequency	f_{out}	50 Hz
Power factor	$\cos\phi$	1.0
Input voltage	V_{in}	150 V
DC link voltage	V_{dc}	380 V
Input impedance	R_{in}	3.3 Ω
Modulation index	m	0.74
Ambient temperature	T_a	40 °C
Junction temperature	T_j	140 °C
CSPI		3 °C/dm^3

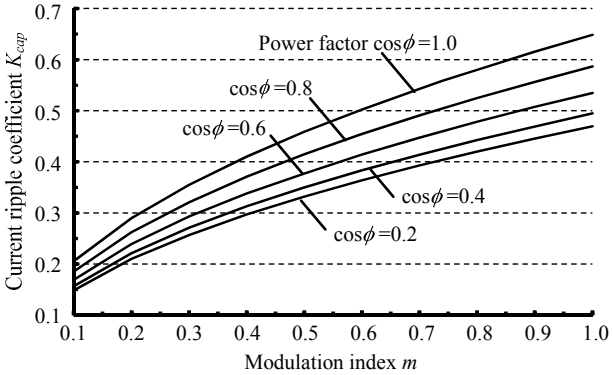


Fig. 2. Current ripple coefficient for the calculation of the ripple current flowing into the electrolytic capacitor. The ripple current is function of the output power factor cosϕ and the modulation index m.

$$p_{buf} = \frac{1}{2} V_m I_m \cos 2\omega_{out} t \quad (4),$$

Fig. 5 shows the design flowchart in order to optimized design the boost type active buffer. First, the capacitance of the buffer capacitor is calculated based on an average voltage and a voltage oscillation range of the buffer capacitor. Then, the capacitor volume Vol_{Cbuf} is determined from the commercially available products. The switching device is decided based on the maximum voltage of the buffer capacitor. In this paper, the switching device, which has a rating voltage of 1200 V, is used. Second, the boost inductor is designed based on the switching frequency f_{sw} and the inductor ripple current. The

volume of the boost inductor is estimated according to Area Product concept [7]. Third, the heatsink volume is calculated from the thermal resistance which depends on the conduction loss P_{loss_cond} and the switching loss P_{loss_sw} of the switching devices. Finally, the Pareto optimization is obtained through varying the switching frequency in order to reveal the maximum power density point.

The capacitance is decided from the relationship between the storage energy and the capacitor voltage. From the storage power in (4), the instantaneous power p_{buf} in the active buffer is represented by

$$P_c = \frac{1}{2}\omega_{out} C_{buf}\left\{\left(V_{ave}+\Delta\frac{V_c}{2}\right)^2-\left(V_{ave}-\Delta\frac{V_c}{2}\right)^2\right\} \quad (5),$$

where V_{ave} is the average voltage and ΔV_c is the voltage oscillation range of the buffer capacitor.

In the passive topology circuit with the bulky electrolytic capacitor, the power storage is achieved by the large capacitance. On the other hand, in the active buffer, the storage power is achieved through the large ΔV_c [8]. This is the principle to reduce the capacitance with active power decoupling method. Then, the capacitance to compensate the power ripple is calculated by

$$C_{buf} = \frac{P_c}{\omega_{out} V_{ave} \Delta V_c} \quad (6),$$

The buffer capacitor requires the large V_{ave} and ΔV_c for reducing the capacitance. However, when the buffer capacitor voltage is increased, the switching device with the high rating voltage is required. In this paper, the switching device, which has the rating voltage of 1200 V, is selected as the peak capacitor voltage of 800 V.

The boost inductor is designed based on an allowable ripple current Δi_L. The inductance becomes the maximum value when the difference between the dc-link voltage and the buffer capacitor voltage reaches the maximum. Thus, the inductance of the boost inductor is provided by

$$L_{buf} = \frac{V_{dc}}{\Delta i_L f_{sw}} \frac{\left(V_{ave}+\frac{\Delta V_c}{2}\right)-V_{dc}}{V_{ave}+\frac{\Delta V_c}{2}} \quad (7),$$

The inductor volume depends on many parameters of the components. There are several ways to select the core for the inductor. In this paper, the boost inductor is designed by Area Product concept using the window area and the cross-sectional area [7]. Therefore, the volume of the boost inductor Vol_{Lbuf} is calculated by

$$Vol_{Lbuf} = K_v\left(\frac{L_{buf} I_{\max}^2}{K_u B_{\max} J}\right)^{\frac{3}{4}} \quad (8),$$

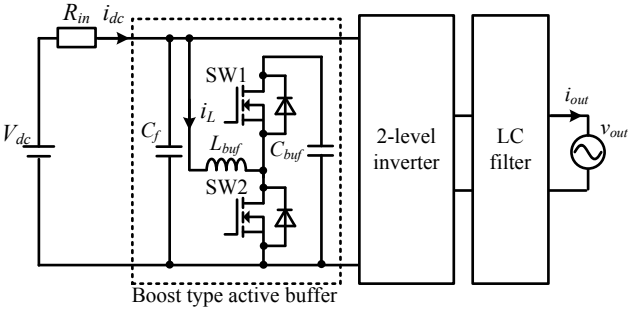


Fig. 3. Boost type active buffer circuit.

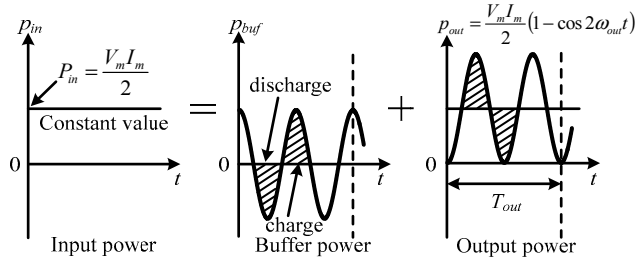


Fig. 4. Single-phase power ripple compensation.

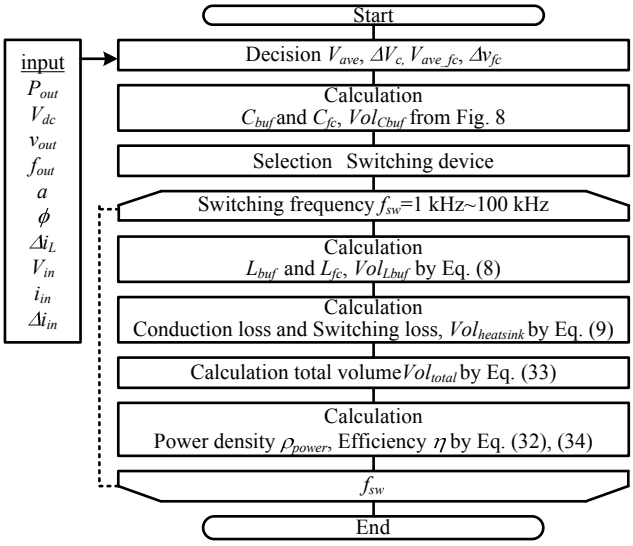


Fig. 5. Designing flow for active buffer circuit.

where, K_v is the volume coefficient depending on the shape of cores, I_{max} is the maximum current flowing to the inductor, K_u is the fill factor of the window, B_{max} is the maximum flux density of the core, and J is the current density of the wire.

The switching devices require a cooling system such as heatsinks and fans. In general, the cooling system is designed based on the thermal resistance. CSPI (cooling system performance index) is introduced to estimate the volume of cooling system [9]. CSPI means the cooling performance per unit volume of the cooling system. The cooling system is miniaturized when CSPI become higher. The volume of the cooling system $Vol_{heatsink}$ is provided by

$$Vol_{heatsink} = \frac{1}{R_{th(f-a)} CSPI} \quad (9),$$

where, $R_{th(f-a)}$ is the thermal resistance of the cooling system

which is given by

$$R_{th(f-a)} = \frac{T_j - T_a}{P_{loss}} - \left(R_{th(j-c)} + R_{th(c-f)}\right) \quad (10),$$

where, T_j is the junction temperature of the switching device, T_a is the ambient temperature, $R_{th}(j\text{-}c)$ is the junction-to-case thermal resistance and $R_{th}(c\text{-}f)$ is the case-to-fin thermal resistance. The total loss P_{loss}, which is composed of the conduction loss P_{loss_cond} and the switching loss P_{loss_sw} from the switching devices, is calculated by

$$P_{loss} = P_{loss\_cond\_buffer} + P_{loss\_sw\_buffer} \quad (11),$$

where, P_{loss_cond} and P_{loss_sw} are given by

$$P_{loss\_cond\_buffer} = \frac{1}{T_{out}} \int_0^{T_{out}} i_L^2 r_{on\_buffer} dt \quad (12),$$

$$P_{loss\_sw\_buffer} = \frac{1}{E_{dcd} I_{md}} \left(e_{on} + e_{off}\right) f_{sw} \frac{1}{T_{out}} \int_0^{T_{out}} v_c i_L dt \quad (13),$$

respectively, where, T_{out} is the period of the grid, r_{on} is the on-resistance of the switching device, f_{sw} is the switching frequency of the active buffer, e_{on} and e_{off} are the turn-on and turn-off energy per switching referred from a datasheet, respectively, E_{dcd} and I_{md} are the voltage and the current under the measurement condition of the switching loss described in the datasheet. The buffer capacitor voltage v_c and the boost inductor current i_L are expressed by

$$v_c = V_{ave} - \frac{\Delta V_c}{2} \sin\left(2\omega_{out} t\right) \quad (14),$$

$$i_L = \frac{V_{ave}}{V_{dc}} C_{buf} \frac{dv_c}{dt} \quad (15),$$

respectively. From (13), the increase in the switching frequency leads to the increase in the switching loss. The cooling performance can be improved by fans to minimize the heatsinks. However, the system lifetime is limited by these fans. Thus, in this paper, the cooling system is designed on the assumption that the natural cooling is applied.

The small filter capacitor C_f is necessary in order to absorb the ripple current at the switching frequency. The impedance of the filter capacitor should be sufficiently small against the internal impedance R_{in}. Thus, C_f is designed by

$$C_f = \frac{1}{2 \times 2\pi f_{sw\_inv}} \frac{10}{R_{in}} \quad (16),$$

where f_{sw_inv} is the switching frequency of the inverter.

C. Buck Type Active Buffer Circuit

Fig. 6 shows the circuit configuration of the buck type active buffer circuit. In this circuit, the capacitor voltage is lower than the DC-link voltage. The buck type active buffer can still be designed through the flowchart in Fig. 5.

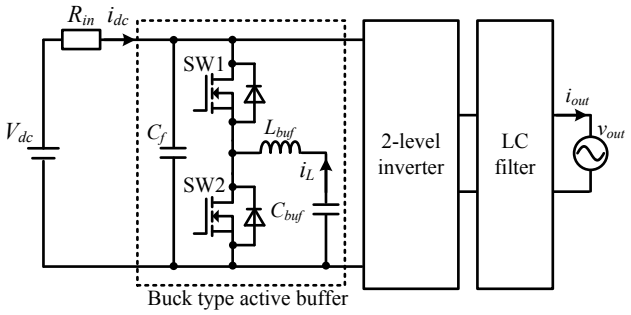


Fig. 6. Buck type active buffer circuit.

The buffer capacitor is designed by (6). However, the DC link voltage limits the peak voltage of the buffer capacitor. As a result, the buffer capacitance has to be larger than the one of the boost type active buffer.

The inductance of the smoothing inductor reaches the maximum value when the capacitor voltage is a half of the input voltage. Thus, the inductance is designed by

$$L_{buf} = \frac{V_{dc}}{4 \Delta i_L f_{sw}} \quad (17),$$

where, i_L is the current which flows to the smoothing inductor which is provided by

$$i_L = C_{buf} \frac{dv_c}{dt} = -\frac{P_{out}}{V_{ave}} \cos\left(2\omega_{out} t\right) \quad (18),$$

The volume of the smoothing inductor is estimated by Area Product of (8). The loss generated by the switching devices is calculated by substituting (18) to (11), (12) and (13).

D. Flying Capacitor Converter

Fig. 7 shows the circuit configuration of a flying capacitor converter (FCC) with a capability of the power decoupling [11]. This circuit consists of a flying capacitor C_{fc}, a boost inductor L_{fc} and four switches. The power ripple is absorbed by the flying capacitor whose voltage oscillates at twice the grid frequency. This circuit has no additional inductor for a buffer voltage control. The duty ratio is decided from the sum of the duties of a current control for the FCC, a power decoupling control and a noninterference control. Therefore, the duties for S1 and S2 are obtained by

$$d_1 = \frac{V_{in}}{V_{dc}} \left\{1 + \cos\left(2\omega_{out} t\right)\right\} \quad (19),$$

$$d_2 = \frac{V_{in}}{V_{dc}} \left\{1 + \left(1 - \frac{V_{dc}}{V_{fc\_ave}}\right) \cos\left(2\omega_{out} t\right)\right\} \quad (20),$$

respectively. Note that the S3 and S4 are complementary to S2 and S1, respectively. When the boost ratio is larger than 2, an

inductance of the boost inductor in the worst case is calculated by

$$L_{fc} = \frac{\max\left[\left(V_{in} - V_{dc} - v_{fc}\right)d_1, \left(V_{in} - v_{fc}\right)d_2\right]}{f_{sw}\Delta i_{in}} \quad (21),$$

where Δi_{in} is the allowable current ripple and f_{sw} is the switching frequency of the FCC. The volume of the boost inductor is estimated by Area Product of (8). The voltage of the flying capacitor v_{fc} is given by

$$v_{fc} = V_{fc\_ave} - \frac{\Delta v_{fc}}{2}\sin\left(2\omega_{out}t\right) \quad (22),$$

where, V_{ave_fc} is the average voltage and Δv_{fc} is the voltage oscillation range of the flying capacitor. Therefore, the capacitance of the flying capacitor is calculated from (6).

The conduction loss and the switching loss caused by switching devices are calculated by

$$P_{loss\_cond\_FCC} = \frac{1}{T_{out}}\int_0^{T_{out}} i_{in}^2 r_{on\_FCC}\,dt \quad (23),$$

$$P_{loss\_sw\_FCC} = \frac{1}{E_{dcd}I_{md}}\left(e_{on} + e_{off}\right)f_{sw}\frac{1}{T_{out}}\int_0^{T_{out}} v_{Sn} i_{in}\,dt \quad (24),$$

respectively, where r_{on_FCC} is the on-resistance of switching devices. The maximum voltage applied for each switch v_{Sn} is expressed by

$$v_{S1} = v_{S4} = V_{dc} - v_{fc} \quad (25),$$

$$v_{S2} = v_{S3} = v_{fc} \quad (26),$$

respectively. Based on the designing flowchart of Fig. 5, the Pareto front of the FCC is obtained.

III. Boost Chopper Design

Fig. 8 shows the circuit configuration of an overall PCSs which is consisted of a boost chopper, a buffer circuit, a grid interconnected inverter and a LC filter. The FCC comes in the boost chopper and the buffer circuit. In order to compare between the volumes of the FCC and the conventional topology, the volume design of the boost chopper is necessary.

The inductance of a boost inductor is determined by

$$L_{cho} = \frac{V_{in}}{\Delta i_{in} f_{sw}}\frac{V_{dc} - V_{in}}{V_{dc}} \quad (27),$$

where, Δi_{in} is the input current ripple, which is 30% of the rated input current in this paper. The total loss of the switching devices is expressed by

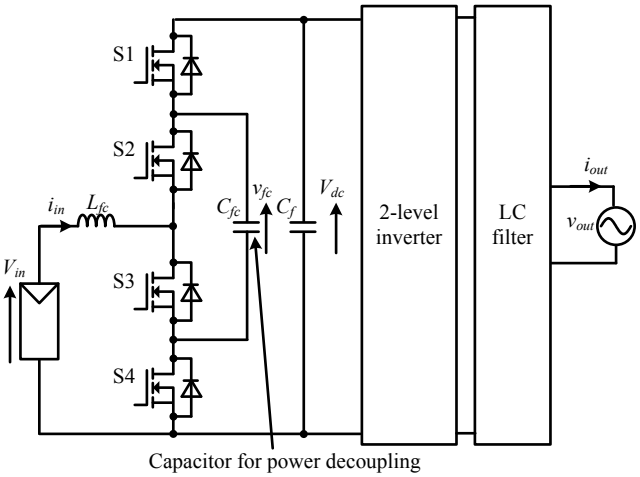


Fig. 7. Flying capacitor converter applied for the power decoupling.

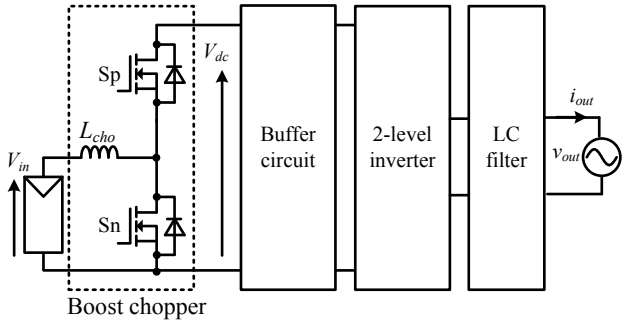


Fig. 8. Circuit configuration of an overall PCSs.

$$P_{loss\_chopper} = P_{loss\_cond\_chopper} + P_{loss\_swi\_chopper} \quad (28),$$

where, the conduction loss $P_{loss\_cond\_chopper}$ is calculated by

$$P_{loss\_cond\_chopper} = r_{on\_chopper}\left(I_{in}^2 + \frac{\Delta i_{in}^2}{3}\right) \quad (29),$$

and $P_{loss\_swi\_chopper}$ is the total switching loss by Sp and Sn whose the switching losses are obtained by

$$P_{loss\_sw\_sp} = \frac{1}{E_{dcd}I_{md}} f_{sw} V_{dc}\left[e_{on}\left(i_{in} + \Delta i_{in}\right) + e_{off}\left(i_{in} - \Delta i_{in}\right)\right] \quad (30),$$

$$P_{loss\_sw\_sn} = \frac{1}{E_{dcd}I_{md}} f_{sw} V_{dc}\left[e_{on}\left(i_{in} - \Delta i_{in}\right) + e_{off}\left(i_{in} + \Delta i_{in}\right)\right] \quad (31),$$

respectively.

IV. Efficiency and Power Density Evaluation

A. Comparison Pareto front of buffer circuit

In the passive topology circuit, the electrolytic capacitor connected to the DC-link is selected based on (2). The allowable ripple current becomes 18.7 A on the assumption that $K_{100\text{Hz}}$=1.0 and K_{sw}=1.4. Thus, the electrolytic capacitor, which has the allowable ripple current larger than 18.7 A, is selected. When the rating voltage of the electrolytic capacitor is fixed, the volume of the electrolytic capacitor becomes smaller by connecting the capacitors with small allowable ripple

current in parallel [10]. In this paper, 28 electrolytic capacitors, which have the allowable ripple current of 1 A per one capacitor, are connected in parallel with a ripple current margin of 50%. As a result, the total capacitance is 5040 μF.

Fig. 9 shows a relationship between the capacitance and the total volume when the ceramic capacitors are connected in parallel. In the active buffer, the ceramic capacitor is used as the buffer capacitor in term of the high energy density. The DC bias characteristic, which is the decrease in the capacitance of the ceramic capacitor by DC bias, has been considered in Fig. 9. Comparing to the electrolytic capacitor, the ceramic capacitor has the higher ratio between the allowable ripple current and the capacitance. Therefore, when the requirement of the capacitance for the power decoupling is satisfied, the allowable ripple current is sufficient for the ceramic capacitor. Specifically, when the average voltage V_{ave} and the voltage amplitude ΔV_c are 600 V and 400 V respectively, the capacitance C_{buf} is 79.6 μF. The volumes of capacitors of GRM series and KC series (Murata Manufacturing Co., Ltd.) are 0.23 dm^3 and 0.44 dm^3 respectively in the total capacitance of 79.6 μF. However, the required numbers of the ceramic capacitor are 1136 and 13440 respectively, which are not realistic. On the other hand, when a ceramic capacitor of the EVS series (Murata Manufacturing Co., Ltd.) is applied, the total volume and the required number are 0.11 dm^3 and 45 in 79.6 μF. Therefore, the EVS series capacitor (Murata Manufacturing Co., Ltd.) is used in this paper.

Table 2 shows the selected components. Fig. 10 shows the Pareto front of the power density ρ_{power} and the efficiency η with the switching frequency f_{sw} as a variable. The power density is calculated by (19) from the total volume of (20). The efficiency η is provided by (21).

$$\rho_{power} = \frac{P_{out}}{Vol_{total}} \tag{32},$$

$$Vol_{total} = Vol_{Lbuf} + Vol_{Cbuf} + Vol_{sw} + Vol_{heatsink} \tag{33},$$

$$\eta = \frac{P_{out}}{P_{out} + \left(P_{loss} + P_{loss\_Cbuf} + P_{loss\_Cf}\right)} \tag{34},$$

where, Vol_{Cbuf} and Vol_{sw} are the volumes of the buffer capacitor and the package of the switching device. The power density reaches the maximum value, when SiC-MOSFET is used in the boost type active buffer at 30 kHz. Specifically, the maximum power density of 17.0 kW/dm^3 are achieved with the efficiency of 99.5%. On the other hand, the power density of 18.8 kW/dm^3 and the efficiency of 99.8% are achieved in the passive topology. The power density of the passive topology is 1.4 times higher than the maximum power density of the active buffer.

B. Volume Comparison between Boost Type and Buck Type Active Buffer

Fig. 11 shows the relationship between the rated power and the total volume of the boost and the buck type active buffer. In

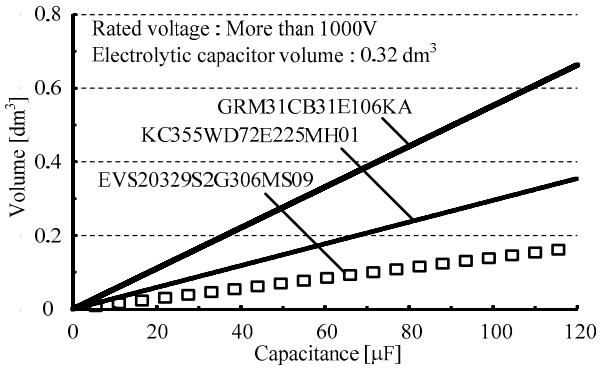


Fig. 9. Relationship between capacitor volume and capacitance.

Table 2. Selected components.

Circuit	Part	Marking	Maximum ration
Passive buffer	C_{in}	Nippon Chemi-Con EKMZ451VSN181MP30S	450 V, 1.0 Arms 180 μF
Boost type active buffer	C_{buf}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF
	SW1 SW2	ROHM SiC-MOSFET, SCH2080KE	1200 V 40 A
		Fuji Electric IGBT, FGW30N120HD	1200 V 30 A
		Fuji Electric Si-MOSFET, FMH30N60S1	600 V(2 series connection) 30 A
Step down type active buffer	C_{buf}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF
	SW1 SW2	ROHM SCT2120AF	650 V 29 A
Boost chopper	Sp Sn	ROHM SiC-MOSFET, SCT120AF	650 V 29 A
Flying capacitor converter	S1 S2 S3 S4	ROHM SiC-MOSFET, SCT120AF	650 V 29 A
		ROHM SiC-MOSFET, SCTMU001F	400 V 20 A
	C_{fc}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF
	C_f	Murata Manufacturing KC355WD72E225MH01	450 V 1 μF

Fig. 11, the frequency value expresses the maximum power density point in each rated power. In the region of less than 3 kW, the volume of the buck type active buffer is smaller than that of the boost type active buffer, especially 24% smaller at 2 kW.

Fig. 12(a) shows the volume ratio of components at the maximum power density point when the output power is 2 kW. In the boost type active buffer, the capacitance of the buffer capacitor can be reduced by higher capacitor voltage, however, the series connection numbers increases to satisfy the rating voltage. As a result, the volume of the buffer capacitor is 167% of that of the buck type active buffer.

Fig. 12(b) shows the volume ratio of components at the maximum power density point in 6 kW. In the buck type active buffer, the cooling system volume accounts for 64% of the total and it is 244% against that of the boost type active buffer. Because the buffer capacitor voltage is lower than DC-link voltage, the high effective current of the boost inductor leads to the large conduction loss. The increases of the heatsink volume

is more critical than that of the boost type active buffer. Therefore, in the region of more than 3 kW, the total volume of the buck type active buffer is larger than that of the boost type active buffer.

C. Comparison Pareto front of FCC

Fig. 13(a) presents the operation waveforms which is operated by a 1-kW prototype of the FCC without the power decoupling control. According to Fig. 13(a), the DC-link voltage fluctuates at twice the grid frequency. On the other hand, from Fig. 13(b), a flying capacitor voltage whose amplitude and average are 100 $V_{\text{peak-peak}}$ and 200 V respectively, oscillates at twice the grid frequency. As a results, the DC-link voltage becomes the constant. This experimental waveforms show that the single-phase power ripple can be compensated by the flying capacitor.

Fig. 14 shows the Pareto front of the FCC and the boost chopper with the buffer circuits. The switching devices with a rated voltage of 650 V and 400 V are selected for the FCC in Table 2 and the derating current which is 5 times of the rated input current is considered. The maximum voltages of the flying capacitor are set to 340 V and 250 V for each switching device. According to the Fig. 14, the power density approaches the maximum value, when SiC-MOSFET with a rated voltage of 400 V is used in the FCC at 25 kHz. A maximum power density of 5.3 kW/dm^3 is achieved with efficiency of 98.9%. On the other hand, the power density of 4.2 kW/dm^3 and the efficiency of 98.8% are achieves in the passive topology. Therefore, the maximum power density of the FCC is 1.3 times higher than the power density of the passive topology.

D. Volume Comparison

Fig. 15 shows the volume ratio of components at the maximum power density point. The component volumes are normalized with the total volume of the passive topology as 100%. In the FCC with 400-V SiC-MOSFET, the volume of the flying capacitor is reduced by 54.6% of that of the electrolytic capacitor. As a result, the overall volume is 78.8% in comparison with the one of the passive topology. When the flying capacitor voltage is set to 250 V and the switching device with the rated voltage of 400 V is applied to the FCC, the flying capacitor is twice the volume of the one with the rated voltage of 650 V. However, the volumes of the boost inductor and the cooling system are reduced to 58.3% and 46.2%, respectively. As a result, the total volume of FCC with the switching devices of the 400-V rated voltage is 57.5% of that of FCC with a rated voltage of 650 V.

E. Loss Comparison

Fig. 16 shows the power loss ratio at the maximum power density point. The loss caused by the boost inductor is ignored. The loss is normalized with the total loss of the passive topology. When the switching device with a rated voltage of 650 V is used for the FCC, the total power loss is 120%. On the other hand, the conduction loss of the switching devices of 400-V rated voltage is reduced to 56.3% in comparison with that of the 650-V rated voltage device. As a result, the total power loss of the FCC using the switching device with the

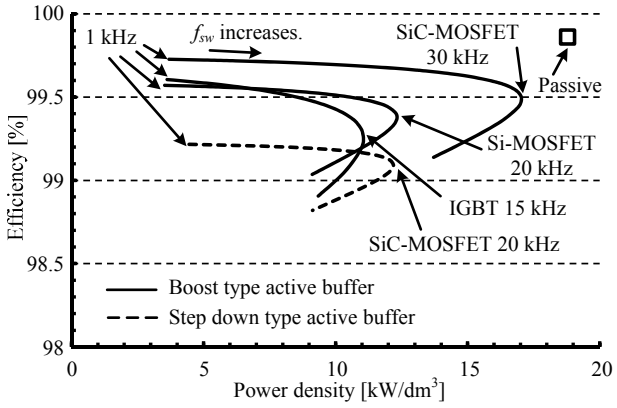


Fig. 10. Pareto front of the passive and the active buffer circuits.

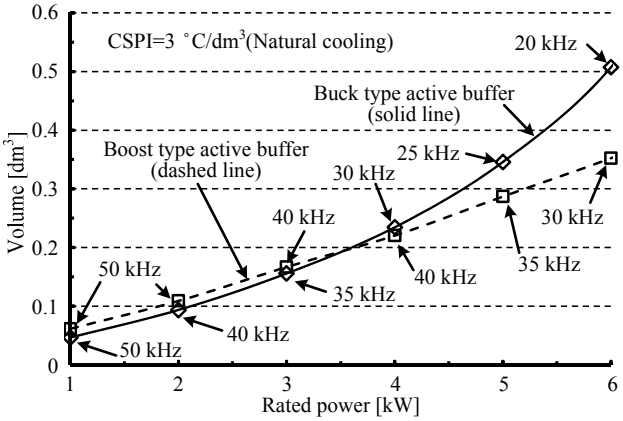
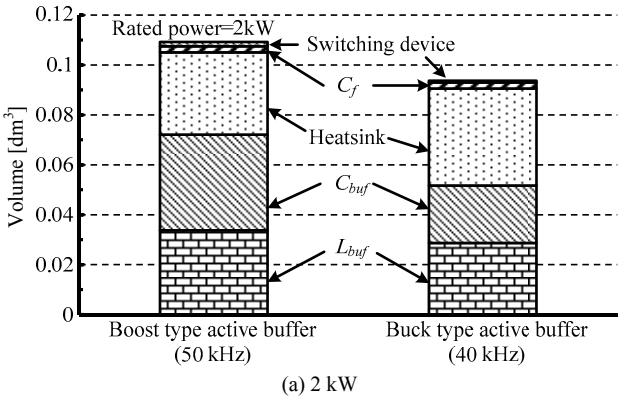
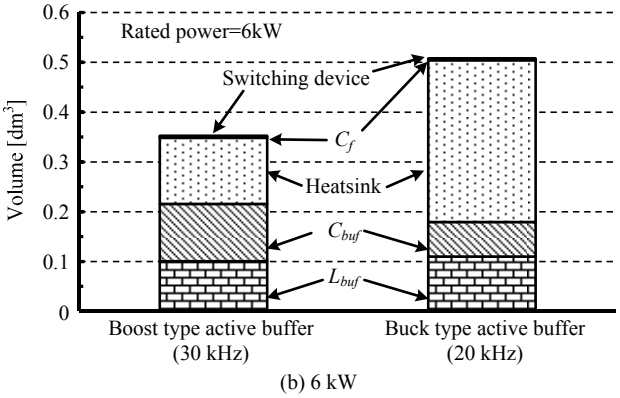


Fig. 11. Relationship between the rated power and the volume of the boost and buck type active buffer at the maximum power density points.



(a) 2 kW



(b) 6 kW

Fig. 12. Volume comparison of the active buffer circuits.

rated voltage of 400 V is 89.5% compared to that of the conventional topology.

V. Conclusion

This paper discussed a comparison of circuit topologies for an active power decoupling of single-phase inverter in terms of efficiency and power density. In particular, the volume of capacitors is reduced by 54.6% in a FCC with ceramic capacitors compared to bulky electrolytic capacitors. As a result, when a SiC-MOSFET of the 400-V rated voltage is applied for the FCC at 25 kHz, the maximum power density is 5.3 kW/dm^3 which is 1.3 times higher than the power density of the electrolytic capacitor. Furthermore, the total power loss is reduced to 89.5% in comparison with that of the conventional converter. Therefore, the flying capacitor converter can achieve the highest power density and the highest efficiency in the discussed topologies in this paper.

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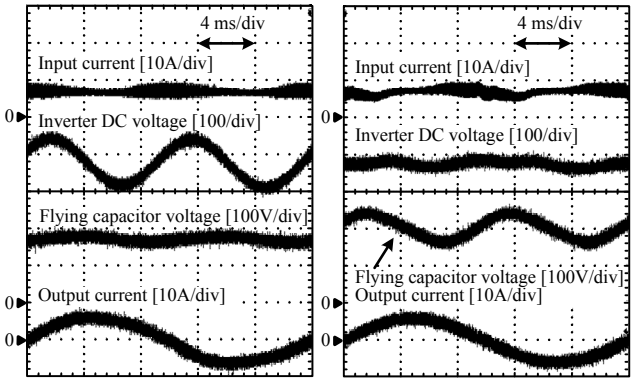

Fig. 13. Operation waveforms of the flying capacitor converter.

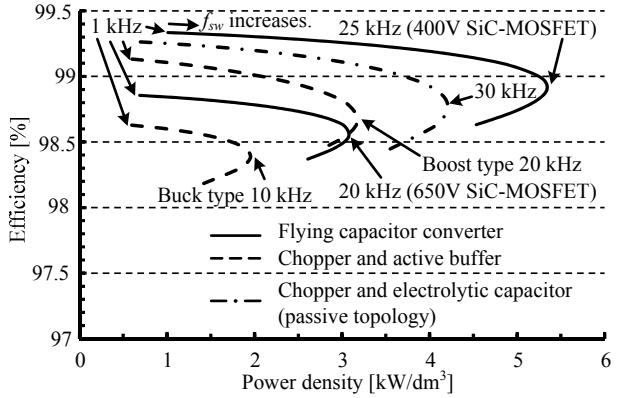

Fig. 14. Pareto front of the FCC and the boost chopper with the buffer circuits.

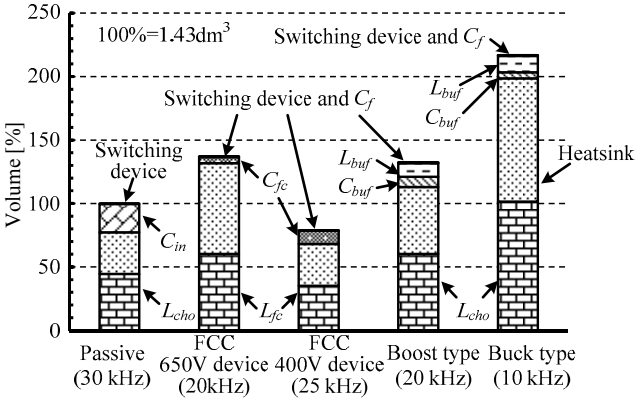

Fig. 15. Volume comparison in the maximum power density points.

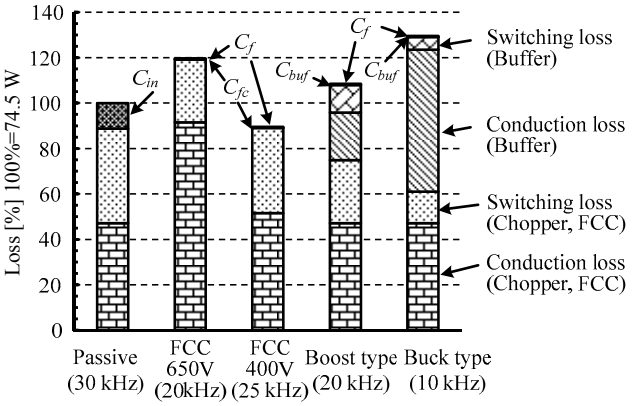

Fig. 16. Loss comparison in the maximum power density points.