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Paper

Fundamental Operation of Modular Marx Topology for High Boost Ratio DC-DC Converter

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The paper proposes a high boost ratio of modular Marx topology DC-DC boost converter (MTBC). In the proposed converter, the parallel-connection is applied at the input side in order to reduce the conduction loss and the copper loss. Meanwhile the multi-stage connection is applied at the output side in order to reduce the voltage rating of switching components at the output side. Therefore, with the proposed circuit configuration, high efficiency of the high boost ratio DC-DC converter is achieved. Besides, 3-stage MTBC with boost ratio of 8.33 between the input voltage to the output voltage is designed and constructed. Moreover, the achieved maximum efficiency of the designed 3-stage MTBC is 94.5%. Meanwhile, from the loss analysis, it shows that the iron loss and the conduction loss are dominant.

Keywords: high boost ratio DC-DC converter, Marx topology converter, input inductor design, stage capacitor design.

1. Introduction

DC-DC converter with high boost ratio is required for low DC voltage energy sources such as for electric vehicle (EV) system, fuel-cells system and photovoltaic (PV) systems. These systems usually need low-voltage and high-current power converters in order to supply DC power to a DC bus or a load.

In a conventional DC-DC boost converter, a high boost ratio can be achieved by connecting those converters in cascade connection [1]. However, this topology cannot achieve high efficiency due to a number of required cascade connected DC-DC converters. Especially, high conduction losses occur at input side due to large input current. Besides, generally DC-DC converters using high frequency transformers are also used in order to obtain a high boost ratio [1-5]. However, those converters usually suffer from the bulkiness and large losses due to the bulky transformer. In addition, leakage current causes false operation of the DC-DC converter due to the parasitic capacitance and high voltage difference between the transformer windings. On the other hand, a high boost ratio is achieved with switched capacitor DC-DC converters [6-8]. However, the output voltage stress on the output capacitor is very high due to high output voltage and it requires many capacitors connected in series. Meanwhile, with diode clamped converters, the low on-resistance of switching devices is difficult to be achieved due to high voltage stress at the output side [9-11]. Especially if a high boost ratio is considered, those circuit configuration is not practical.

Besides, a Marx generator topology is one of the attractive topology that able to achieve a high boost ratio in DC-DC converter. Basically the purpose of Marx generator is to generate a high-voltage pulse from a low-voltage DC source [12, 13]. However, the conventional Marx generator has high conduction losses and copper losses due to large input current. As a result, the efficiency of the conventional Marx generator is low. Therefore the main application of the Marx generator is limited for low power applications. On the other hand, the Marx topology DC-DC converters with resonant condition operation are proposed in order to achieve the ZCS condition [14-16]. However, due to the resonant condition, the input inductor current should be in discontinuous current mode (DCM) and consequently the input inductor is bulky. Furthermore the conduction loss is also increased.

This paper proposes a new high boost ratio of a Marx topology DC-DC converter. In the proposed circuit, the parallel-connection of conventional 2-level boost DC-DC converters are applied at the input side in order to reduce the conduction loss and the copper loss. In addition, the multi-stage connections are applied at the output side in order to reduce the voltage rating of stage capacitors and switches. Meanwhile, voltage stress of the lower switches side in the input side is same to that of components at the output side. Therefore, lower voltage semiconductors which have low on-resistance can be used for the switches in the proposed circuit. Meanwhile, high voltage rating diodes at the input side are required. However, high voltage rating of SiC diodes which have low forward voltage and low reverse recovery time can be used nowadays. As a result, a high-efficiency boost converter can be achieved.

This paper is organized as follows. First, the principle of the n-stage Marx topology DC-DC converter is described. Then, the input inductors and stage capacitors designs on each stage are established. The relationship between the voltage stress on stage

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capacitors and the number of stages is evaluated. Finally, power loss of the proposed converter is theoretically analyzed. Then, distribution of the power loss is clarified by comparing calculated results and measurement results based on 3-stage Marx topology DC-DC boost converter.

2. Converter Principle and Circuit Configuration

Fig. 1 shows a circuit configuration of the n-stage Marx topology boost converter (MTBC). Basically, each stage of the MTBC consists of a conventional 2-level boost DC-DC converter, a capacitor and two additional switches. The converter is designed based on a principle of the Marx pulse generator whereby a high-output voltage is generated from a low-voltage DC source [12]. This principle is realized by charging several capacitors in parallel and then suddenly connecting those capacitors in series. Therefore, by arranging these combinations of capacitors in the proposed converter, a high output voltage is generated. It is noted that 10 to 20 stages might be required in order to reduce input currents stress, switching devices voltage rating and stage capacitor voltages stress in the actual application.

In order to analyze the MTBC operation and its characteristic, a 3-stage MTBC is introduced as a specific example in this section. In principle, the relationship between the input voltage V_{in} and the output voltage V_{out} is expressed as follows:

$$V_{out} = \beta V_{in} \quad \text{..... (1)}$$

where β is the boost ratio. Meanwhile the duty ratio D in terms of boost ratio β can be expressed as follows:

$$D = \frac{1}{1+\frac{n}{\beta}} \quad \text{..... (2)}$$

where D is the duty ratio for the switches S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_{3a} and S_{3b} and n is the number of stage. Thus the output voltage V_{out} in terms of the duty ratio D, the number of stage n and the input voltage V_{in} can be rewrite as follows:

$$V_{out} = \left(\frac{D}{1-D}\right) n V_{in} \quad \text{..... (3)}$$

Figs. 2 and 3 show the switching pattern and operation mode of the 3-stage MTBC, respectively. The switching pattern with dead-time T_d and additional time-delayed T_a is considered for reducing of surge voltage of the switch. The 3-stage MTBC needs four operation modes.

Table 1 shows the conditions of the stage capacitors. The stage capacitors C_1, C_2 and C_3 are charging when those capacitors are connected in parallel as shown in Fig. 3. Then, those stage capacitors are connected in series during discharging condition as shown in Fig. 3. Thus, the output voltage is boost-up by the advantage of a series connection of the stage capacitors. Therefore, a high boost ratio is achieved.

The voltage stresses on the switching devices S_{1a}, S_{1b}, S_{1c}, S_{2a}, S_{2b}, S_{2c}, S_{3a}, S_{3b} and S_{3c} are determined by each of the maximum stage capacitor voltages V_{C1}, V_{C2} and V_{C3}. Each stage capacitor voltage is lower than the output voltage. Therefore, lower voltage stress semiconductors which have low on-resistance can be used. Meanwhile, the voltage stresses on the diodes D_1, D_2 and D_3 are equal to the V_{C1}, $2V_{C2}$, and $3V_{C3}$, respectively. Thus the top diode voltage stress is equal to total stage capacitor voltage stresses.

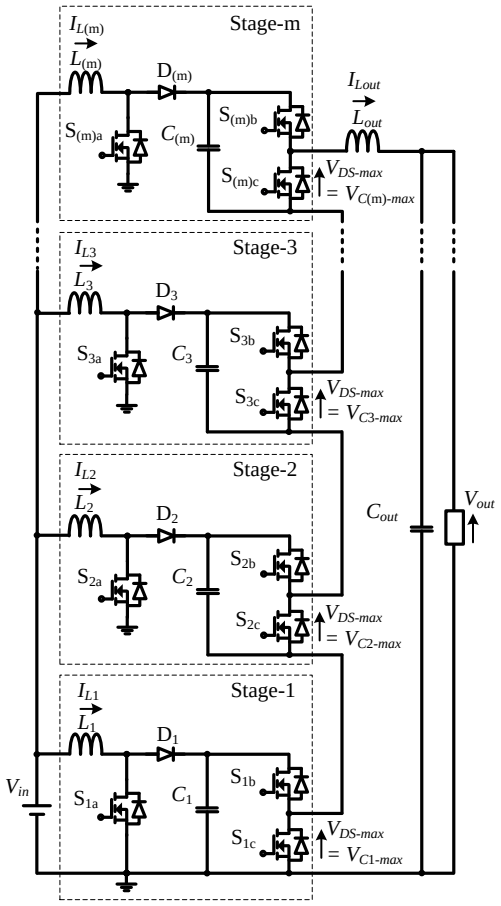


Fig. 1. n-stage MTBC circuit configuration.

However, high voltage SiC diodes which have low forward voltage and low reverse recovery time can be used nowadays.

3. Passive components design and selection

In this section, the inductor current of each stage in the MTBC is designed to be operated in continuous current mode (CCM) in order to minimize the peak input current. Thus the minimum inductor current of each stage should be greater than zero in order to ensure a CCM condition is achieved. Then the minimum inductance of the input inductor of each stage $L_{in(m)}$ for CCM operation is expressed as follows:

$$L_{in(m)} > \frac{n(V_{in})^2 D}{2 P_{out} f_{sw}} \quad \text{..... (4)}$$

where m is the n-th of stage, n is the number stage, P_{out} is the output power and f_{sw} is the switching frequency. Meanwhile the inductor current ripple on each stage $\Delta I_{Lin(m)}$ can be expressed as follows:

$$\Delta I_{Lin(m)} = \frac{V_{in} D}{f_{sw} L_{in(m)}} \quad \text{..... (5)}$$

The capacitance of the stage capacitor is expressed as follows:

$$C_{(m)} = \frac{I_{L(m)-ave}(1-D)}{\Delta V_{C(m)} f_{sw}} = \frac{P_{in}(1-D)}{n V_{in} \Delta V_{C(m)} f_{sw}} \quad \text{..... (6)}$$

where $C_{(m)}$ is the capacitance of the stage capacitor and $\Delta V_{C(m)}$ is the stage capacitor voltage ripple.

Principally, the maximum stage capacitor voltage $V_{C(m)\text{-}max}$ and the average inductor current on each stage $I_{L(m)\_ave}$ are expressed as follow:

$$V_{C(m)-\max} = V_{DS-\max} = V_{in} + \frac{V_{out}}{n} \quad \text{..... (7)}$$

$$I_{L(m)-ave} = \frac{P_{in}}{nV_{in}} \quad \text{..... (8)}$$

where $V_{DS\text{-}max}$ is the maximum drain-source voltage of a MOSFET, P_{in} is the input power.

According to the circuit arrangement as shown in Fig. 3, the maximum stage capacitor voltage is equal to the maximum of drain-source voltage of MOSFETs as shown by (7). Furthermore, the maximum stage capacitor voltage and average stage current are inversely proportional to the number of stage as shown by (7) and (8). Thus the maximum stage capacitor voltage and average stage current will be reduced according to the increasing the number of stage *n*.

4. Loss Analysis Based on Theoretical Equation

In this section, the effective and average currents for the MOSFETs and diode are derived mathematically for loss analysis calculation. Then, the conduction power losses of the MOSFET and diode in the 3-stage MTBC are analyzed theoretically.

4.1 Conduction loss for MOSFETs S_{1a}, S_{2a} and S_{3a}

Principally, the effective currents of $i_{S1a(eff)}$, $i_{S2a(eff)}$ and $i_{S3a(eff)}$ are same because the input side of the MTBC are synchronized. The effective current is expressed as follows:

$$i_{S1a(eff)} = i_{S2a(eff)} = i_{S3a(eff)} \quad \text{..... (9)}$$

$$i_{S1a(eff)} = \left(\frac{\left(I_{Lin\_\max}{}^2 - 2I_{Lin\_\min} I_{Lin\_\max} + I_{Lin\_\min}{}^2 \right) D}{3} + \left(I_{Lin\_\max} - I_{Lin\_\min} \right) I_{Lin\_\min} D + I_{Lin\_\min}{}^2 D \right)^{1/2} \quad \text{..... (10)}$$

where I_{Lin_max} and I_{Lin_min} are the maximum and minimum input inductor currents, respectively at each stage and the currents equal to the maximum and minimum currents of the MOSFET S_{1a} I_{S1a_max} and I_{S1a_min}, respectively. The maximum and minimum currents I_{S1a_max} and I_{S1a_min} are expressed as follow:

$$I_{S1a\_\max} = I_{Lin\_\max} = \frac{I_{in}}{n} + \frac{V_{in} D}{f_{sw} L_{out}} \quad \text{.....(11)}$$

$$I_{S1a\_\min} = I_{Lin\_\min} = \frac{I_{in}}{n} - \frac{V_{in} D}{f_{sw} L_{out}} \quad \text{..... (12)}$$

where I_{in} is the average input current. Thus the summation of conduction losses for S_{1a}, S_{2a} and S_{3a} are expressed as follows:

$$P_{cond\_(Sma)} = i_{Sma(eff)}{}^2 R_{on} \times n \quad \text{..... (13)}$$

4.2 Conduction loss for MOSFETs S_{1b}, S_{2b} and S_{3b}

The effective currents of $i_{S1b(eff)}$, $i_{S2b(eff)}$ and $i_{S3b(eff)}$ are same. It equals to the output inductor current I_{Lout} when these switches are on-state. The effective current of these switches is expressed as follow:

$$i_{S1b(eff)} = i_{S2b(eff)} = i_{S3b(eff)} \quad \text{..... (14)}$$

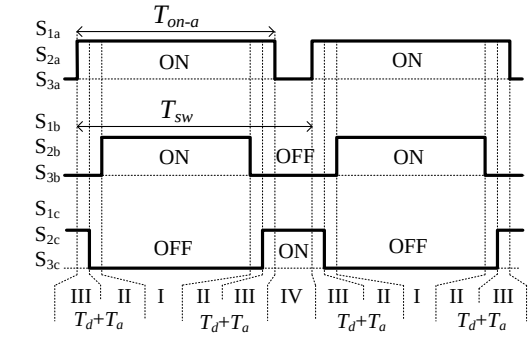
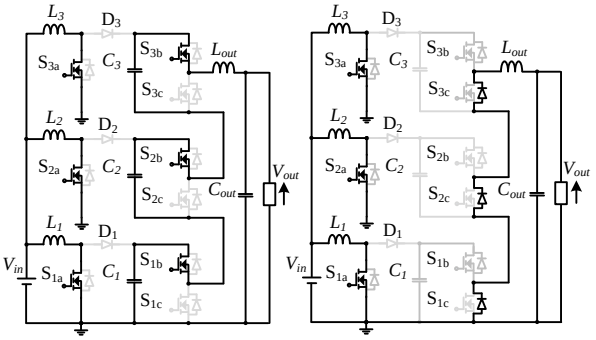
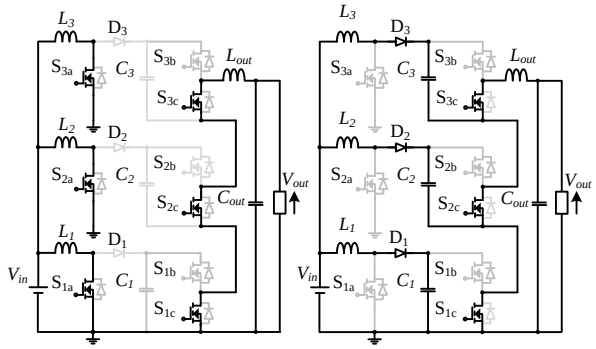


Fig. 2. Switching pattern.



Mode I
S_{1a}, S_{2a} and S_{3a} – ON
S_{1b}, S_{2b} and S_{3b} – ON

Mode II
Dead-time T_d condition
S_{1a}, S_{2a} and S_{3a} – ON



Mode III
Additional time-delay T_a condition
S_{1a}, S_{2a} and S_{3a} – ON
S_{1c}, S_{2c} and S_{3c} – ON

Mode IV
S_{1c}, S_{2c} and S_{3c} – ON

Fig. 3. Operation mode of the 3-stage MTBC.

Table 1. Stage capacitor operation on 3-stage MTBC.

Mode	S_{1a} S_{2a} S_{3a}	S_{1b} S_{2b} S_{3b}	S_{1c} S_{2c} S_{3c}	C_1, C_2 & C_3
(I)	ON	ON	OFF	Discharging in series
(II)	ON	OFF	OFF	unchanged
(III)	ON	OFF	ON	unchanged
(IV)	OFF	OFF	ON	Charging in parallel

$$i_{S1b(eff)} = \left(\frac{\left(I_{Lout\_max} - I_{Lout\_min}\right)^2 D}{3} + \frac{2I_{Lout\_min}\left(I_{Lout\_max} - I_{Lout\_min}\right)D}{2} + I_{Lout\_min}{}^2 D \right)^{1/2} \quad \text{..... (15)}$$

where I_{Lout_max} and I_{Lout_min} are the maximum and maximum output inductor currents, respectively and the currents are equal to the maximum and minimum currents of the MOSFET S_{1b} I_{S1b_max} and I_{S1b_min}, respectively. The maximum and minimum currents I_{S1b_max} and I_{S1b_min} are expressed as follow

$$I_{S1b\_max} = I_{Lout\_max} = I_{out} + \frac{nDV_{in}}{2f_{sw}L_{out}} \quad \text{..... (16)}$$

$$I_{S1b\_min} = I_{Lout\_max} = I_{out} - \frac{nDV_{in}}{2f_{sw}L_{out}} \quad \text{..... (17)}$$

where I_{out} is the average output current. Thus the summation of conduction losses for S_{1b}, S_{2b} and S_{3b} are expressed as follow:

$$P_{cond\_(Smb)} = i_{Smb(eff)}{}^2 R_{on} \times n \quad \text{..... (18)}$$

4.3 Conduction loss for MOSFET S_{1c}, S_{2c} and S_{3c}

Principally, the MOSFETs S_{1c}, S_{2c} and S_{3c} are operated during charging condition of the stage capacitors. Furthermore, the currents $i_{S1c(eff)}$, $i_{S2c(eff)}$ and $i_{S3c(eff)}$ are not same one another due to circuit configuration at the output side as shown in Mode IV of Fig. 3.

The effective current for $i_{S1c(eff)}$ is expressed as follows:

$$i_{S1c(eff)} = \left(\begin{array}{l} \dfrac{\left(I_{S1c\_max}{}^2 - 2I_{S1c\_max}I_{S1c\_min} + I_{S1c\_min}{}^2\right)\left(1-D^3\right)}{3(D-1)^2} \\ + \left(\dfrac{\left(I_{S1c\_max} - I_{S1c\_min}\right)I_{S1c\_min}}{D-1} - \dfrac{\left(I_{S1c\_max}{}^2 - 2I_{S1c\_max}I_{S1c\_min} + I_{S1c\_min}{}^2\right)}{(D-1)^2} \right)\left(1-D^2\right) \\ + \left(I_{S1c\_min}{}^2 - \dfrac{2I_{S1c\_min}\left(I_{S1c\_max} - I_{S1c\_min}\right)}{D-1} + \dfrac{\left(I_{S1c\_max}{}^2 - 2I_{S1c\_max}I_{S1c\_min} + I_{S1c\_min}{}^2\right)}{(D-1)^2} \right)(1-D) \end{array} \right)^{1/2} \quad \text{. (19)}$$

where I_{S1c_max} and I_{S1c_min} are the maximum and minimum current of the MOSFET $S_{1c,}$ respectively. The maximum and minimum currents I_{S1c_max} and I_{S1c_min} are expressed as follow:

$$I_{S1c\_max} = \frac{2I_{in}}{n} - I_{out} + \frac{V_{in}D}{f_{sw}L_{in}} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (20)}$$

$$I_{S1c\_min} = \frac{2I_{in}}{n} - I_{out} - \frac{V_{in}D}{f_{sw}L_{in}} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (21)}$$

Thus the conduction loss for S_{1c} is expressed as follows:

$$P_{cond\_(S1c)} = i_{S1c(eff)}{}^2 R_{on} \quad \text{..... (22)}$$

Then, the effective current for $i_{S2c(eff)}$ is expressed as follows:

$$I_{S2c(eff)} = \left(\begin{array}{l} \dfrac{\left(I_{S2c\_max}{}^2 - 2I_{S2c\_max}I_{S2c\_min} + I_{S2c\_min}{}^2\right)\left(1-D^3\right)}{3(D-1)^2} \\ + \left(\dfrac{\left(I_{S2c\_max} - I_{S2c\_min}\right)I_{S2c\_min}}{D-1} - \dfrac{\left(I_{S2c\_max}{}^2 - 2I_{S2c\_max}I_{S2c\_min} + I_{S2c\_min}{}^2\right)}{(D-1)^2} \right)\left(1-D^2\right) \\ + \left(I_{S2c\_min}{}^2 - \dfrac{2I_{S2c\_min}\left(I_{S2c\_max} - I_{S2c\_min}\right)}{D-1} + \dfrac{\left(I_{S2c\_max}{}^2 - 2I_{S2c\_max}I_{S2c\_min} + I_{S2c\_min}{}^2\right)}{(D-1)^2} \right)(1-D) \end{array} \right)^{1/2} \quad (23)$$

where I_{S2c_max} and I_{S2c_min} are the maximum and minimum currents of the MOSFET $S_{2c,}$ respectively. The maximum and minimum currents I_{S2c_max} and I_{S2c_min} are expressed as follow:

$$I_{S2c\_max} = \frac{I_{in}}{n} - I_{out} + \frac{V_{in}D}{2f_{sw}L_{in}} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (24)}$$

$$I_{S2c\_min} = \frac{I_{in}}{n} - I_{out} - \frac{V_{in}D}{2f_{sw}L_{in}} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (25)}$$

Thus the conduction loss for S_{2c} is expressed as follows:

$$P_{cond\_(S2c)} = i_{S2c(eff)}{}^2 R_{on} \quad \text{..... (26)}$$

Meanwhile, the effective current for $i_{S3c(eff)}$ is expressed as follows:

$$i_{S3c(eff)} = \left(\begin{array}{l} \dfrac{\left(I_{S3c\_max}{}^2 - 2I_{S3c\_max}I_{S3c\_min} + I_{S3c\_min}{}^2\right)\left(1-D^3\right)}{3(D-1)^2} \\ + \left(\dfrac{\left(I_{S3c\_max} - I_{S3c\_min}\right)I_{S3c\_min}}{D-1} - \dfrac{\left(I_{S3c\_max}{}^2 - 2I_{S3c\_max}I_{S3c\_min} + I_{S3c\_min}{}^2\right)}{(D-1)^2} \right)\left(1-D^2\right) \\ + \left(I_{S3c\_min}{}^2 - \dfrac{2I_{S3c\_min}\left(I_{S3c\_max} - I_{S3c\_min}\right)}{D-1} + \dfrac{\left(I_{S3c\_max}{}^2 - 2I_{S3c\_max}I_{S3c\_min} + I_{S3c\_min}{}^2\right)}{(D-1)^2} \right)(1-D) \end{array} \right)^{1/2} \quad (27)$$

where I_{S3c_max} and I_{S3c_min} are the maximum and minimum currents of the MOSFET $S_{3c,}$ respectively. The maximum and minimum currents I_{S3c_max} and I_{S3c_min} are expressed as follow:

$$I_{S3c\_max} = I_{Lout} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (28)}$$

$$I_{S3c\_min} = I_{Lout} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (29)}$$

where I_{Lout} is the average output inductor current. Therefore the conduction loss for S_{3c} is expressed as follows:

$$P_{cond\_(S3c)} = i_{S3c(eff)}{}^2 R_{on} \quad \text{..... (30)}$$

4.4 Conduction loss for diodes D_1, D_2 and D_3 The average diode currents $i_{D1(ave)}$, $i_{D2(ave)}$ and $i_{D3(ave)}$ are same. The average diode current is expressed as follow:

$$i_{D1(ave)} = i_{D2(ave)} = i_{D3(ave)} \quad \text{..... (31)}$$

$$i_{D1(ave)} = \begin{pmatrix} \frac{\left(I_{Lin\_max} - I_{Lin\_min}\right)\left(1-D^2\right)}{2(D-1)} \\ -\frac{\left(I_{Lin\_max} - I_{Lin\_min}\right)(1-D)}{(D-1)} + (1-D)I_{Lin\_min} \end{pmatrix} \quad \text{..... (32)}$$

The maximum and minimum diode currents I_{D1_max} and I_{D2_min} are expressed as follow:

$$I_{D1\_max} = I_{Lin\_max} = \frac{I_{in}}{n} + \frac{V_{in}D}{f_{sw}L_{out}} \quad \text{..... (33)}$$

$$I_{D2\_min} = I_{Lin\_min} = \frac{I_{in}}{n} - \frac{V_{in}D}{f_{sw}L_{out}} \quad \text{..... (34)}$$

Therefore the summation of conduction losses for D_1, D_2 and D_3 are expressed as follows:

$$P_{cond\_(Dm)} = i_{Dm(ave)}V_F \times n \quad \text{..... (35)}$$

4.5 Copper and iron losses In the constructed 3-stage MTBC, the copper loss is contributed by the three input inductors and one output inductor. The copper resistances of each inductor are measured for copper loss estimation. The expression for the copper loss is expressed as follows:

$$P_{copper} = \sum_{m=1}^{n}\left(i_{Lm(eff)}{}^2 R_{copper\_m}\right) + i_{Lout(eff)}{}^2 R_{copper\_out} \quad \text{..... (36)}$$

where $i_{Lm(eff)}$ is the effective stage input inductor currents, $i_{Lout(eff)}$ is the effective output inductor current, R_{copper_m} is the inductor winding resistance of the stage input inductor and R_{copper_out} is the inductor winding resistance of the output inductor.

Meanwhile, iron loss is not analyzed by the theoretical equation in this paper. Instead, based on the power loss measurement and theoretical calculation of other power losses, the different between both power losses is considered as the iron loss.

4.6 Switching loss for MOSFETs and diodes All switching device voltages have same minimum and maximum voltages of the stage capacitor. The minimum and maximum voltages can be expressed as follow:

$$V_{C(m)\_max} = \frac{nV_{in} + V_{out}}{n} + \frac{1}{2}\frac{(1-D)P_{out}}{nf_{sw}C_{(m)}V_{in}} \quad \text{..... (37)}$$

$$V_{C(m)\_min} = \frac{nV_{in} + V_{out}}{n} - \frac{1}{2}\frac{(1-D)P_{out}}{nf_{sw}C_{(m)}V_{in}} \quad \text{..... (38)}$$

The generalization of each switching loss for S_{1a}, S_{2a} and S_{3a} is expressed as follows:

$$P_{SW\_Sma} = \left(\frac{V_{C(m)\_min}I_{Sma\_max}}{6} f_{sw}t_r\right)_{on} + \left(\frac{V_{C(m)\_max}I_{Sma\_min}}{6} f_{sw}t_f\right)_{off}$$

..... (39)

On the other hand, the switching losses for S_{mb} and S_{mc} are defined by the same equation of (39).

4.7 Total conduction and switching losses for all switches and diodes The total conduction and switching losses for all switches and diodes in 3-stage MTBC is expressed as follows:

$$\begin{aligned} P_{cond+SW\_(total)} &= P_{cond\_(total)} + P_{SW\_(total)} \\ &= P_{cond\_(S1a+S2a+S3a)} + P_{cond\_(S1b+S2b+S3b)} + P_{cond\_(S1c)} \\ &+ P_{cond\_(S2c)} + P_{cond\_(S3c)} + P_{cond\_(D1+D2+D3)} \\ &+ P_{SW\_(S1a+S2a+S3a)} + P_{SW\_(S1b+S2b+S3b)} + P_{SW\_(S1c)} \\ &+ P_{SW\_(S2c)} + P_{SW\_(S3c)} \end{aligned} \quad \text{..... (40)}$$

5. Experimental results

Table 2 shows the specifications of the experimental prototype circuit. The inductance of the input inductor on each stage is designed by using (5).

Fig. 4 shows the experimental results of the input inductor current ripples on stage-1 (I_{L1}), stage-2 (I_{L2}) and stage-3 (I_{L3}), which are 1.9 A, 1.8 A and 1.8 A respectively at the output power of 1 kW. However the designed input inductor current ripple on each stage is 1.5 A and the design principle is according to (5). The different between experimental results and designed value is due to the voltage drop on the winding resistance of the inductors. The stage average inductor current is divided by three due to three parallel-connections at the input side. Therefore, if many stages are considered, the input current will be divided by the factor of the stage number and consequently the input current stress, the conduction loss and the copper loss will be reduced.

Fig. 5 shows the experimental results of the capacitor voltages on each stage V_{C1}, V_{C2} and V_{C3} of the 3-stage MTBC. The results show that each stage capacitor voltage is 190 V. On the other hand, it is experimentally confirmed that the output voltage is 400 V when the input voltage is 48 V. Meanwhile if the number of stage is increased the voltage stress on stage capacitors and the maximum voltage stress on switching devices will be reduced as well. Thus according to the (9), the voltage stress on stage capacitor voltages and the maximum voltage stress on switching devices are inversely proportional to the number of stage.

Fig. 6 shows the efficiency characteristic of the prototype circuit. The input and output voltages are fixed at 48 V and 400 V, respectively. The maximum efficiency is 94.5% at the output power of 500 W. In addition, the efficiency is decreased when the output power is increased at 1 kW due to the increasing of the conduction loss and the copper loss. On the other hand, during low output power, the power loss is dominated by the iron loss. As a result, the efficiency is low during low output power.

Fig. 7 shows the distribution of the power losses based on theoretical calculation. The power losses are distributed into nine parts, i.e., diode conduction loss, MOSFET conduction loss at input and output sides, MOSFET switching loss at input and output sides, inductor copper loss, ESR loss, no load loss (discharging power losses for drain-source parasitic capacitances of MOSFETs) and others. The total power loss of 100% is based on the measured total power loss by experiment when the output power is 1 kW. From the loss analysis, it shows that the converter loss is dominated by the 'Others' loss whereby it includes the iron loss, wiring loss and so on. It is estimated that the iron loss is dominant in the 'Others' loss.

Table 2. Experiment specification.

Specification	Value
Input voltage V_{in}/Output voltage V_{out}	48/400 V
Output power P_{out}	1000 W
Switching frequency f_{sw}	50 kHz
Input inductor L_1=L_2=L_3	500 µH
Output inductance L_{out}	800 µH
Stage capacitor C_1=C_2=C_3/Output capacitor C_{out}	44/50 µF
Power MOSFET (SiHG25N40D)	400 V/25 A
SiC Schottky Barrier Diode (SCS220KGC)	1200 V/20 A

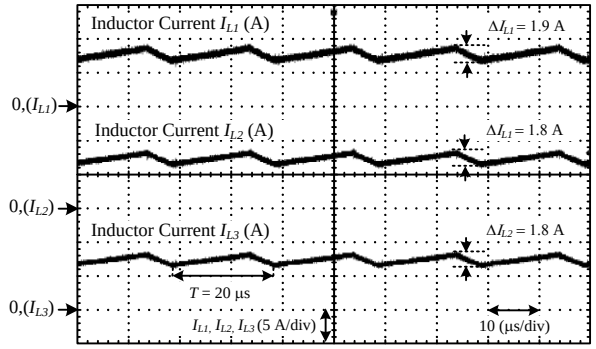


Fig. 4. Experimental waveforms of the stage-1, stage-2 and stage-3 inductor currents.

Based on circuit configuration, the proposed 3-stage MTBC has input and output inductors. Thus, the iron loss is considered dominant especially at the output inductor side due to the high voltage stress at the output. The second major losses are the MOSFET conduction loss and copper loss. From the experimental results, the input current ripple is increased when the output power is increased and this condition leads the iron loss increasing according the increasing the output power. Besides, according to [17], the iron loss is influenced by the voltage stress on the inductor and the applied switching frequency. Thus principally, the iron loss is reduced when the voltage stress and the applied switching frequency are reduced. These options will be further analyzed in a future research work for iron loss reduction.

6. Conclusion

This paper proposes a high boost ratio modular Marx topology DC-DC boost converter whereby the parallel-connection of several capacitors at the input side and then the multistage connection of capacitors at the output side are applied. In the present paper, the authors have discussed (i) the fundamental circuit operation confirmation of the 3-stage MTBC, (ii) the design principle of the input inductors and stage capacitors, and (iii) the mathematical expression for loss calculation and analysis.

The principals of designing the inductance of the input inductor and the capacitance of the stage capacitors according to the number of stage were explained. As a result, the inductance of the input inductor and stage capacitor voltages stress on each stage is reduced by the increasing the number of stage. The input inductor current ripple on each stage is designed and it confirmed by the experimental results. Moreover, mathematical expressions of the conduction and switching losses are derived and were confirmed by the simulation results. The maximum efficiency of the prototype converter was 94.5% at the output power of 500 W. From the loss analysis, it is confirmed that the efficiency is increased by optimizing inductor design.

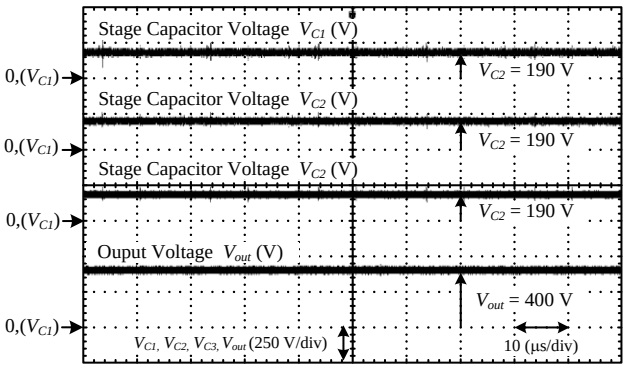


Fig. 5. Experimental waveforms of the stage-1, stage-2 and stage-3 capacitor voltages, and the output voltage.

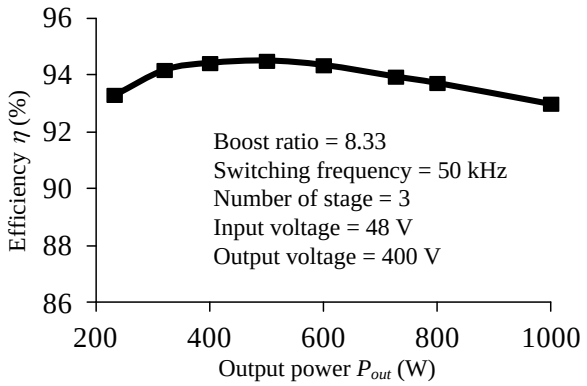


Fig. 6. Efficiency of the 3-stage MTBC.

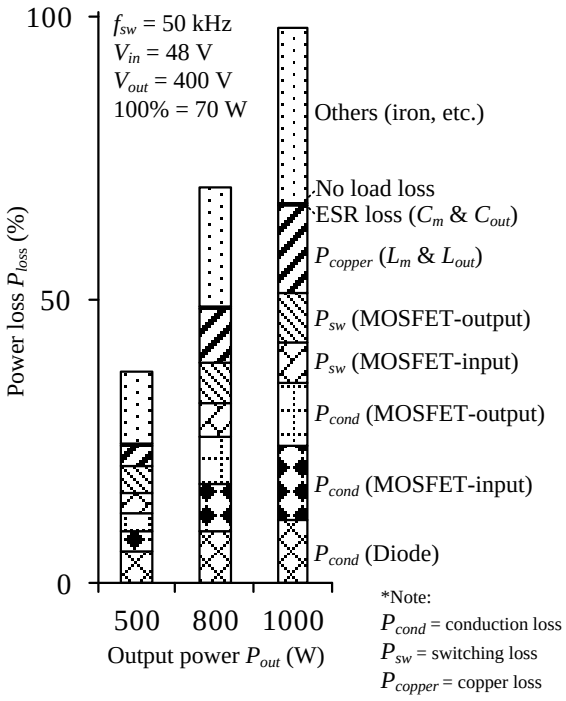


Fig. 7. Loss distribution of the 3-stage MTBC.

In a future, new switching patterns will be introduced for the converter efficiency improvement.

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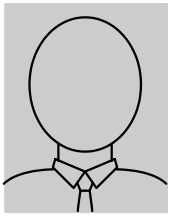

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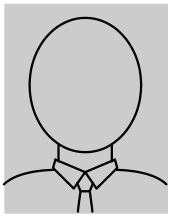

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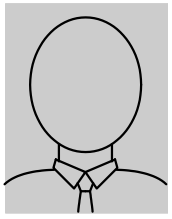

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