Requirements for Circuit Components of Single-Phase Inverter Applied with Power Decoupling Capability toward High Power Density

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Keywords

«High power density systems», «Single phase system», «Power conditioning»

Abstract

This paper discusses how to achieve high power density with high efficiency for a single-phase inverter with an active power decoupling circuit. In conventional PV inverters, bulky electrolytic capacitors are connected to DC-link in order to absorb power pulsation with twice the grid frequency. On the other hand, in the active power decoupling circuit, the small capacitor can be used. However, the additional inductors and switching devices are necessary. Thus, the power density of the active power decoupling circuit is reduced. In this paper, the Pareto optimization of power density and efficiency is used to clarify the maximum power density points of the power decoupling circuits. As a result, the maximum power density of the conventional boost type active buffer, which connects a boost chopper to DC-link, is 90% of that of electrolytic capacitor topology. In addition, this paper proposes a DC-DC converter with the power decoupling capability in order to achieve higher power density than that of the passive topology. The proposed circuit, which requires no additional inductor for the power decoupling circuit, uses discontinuous current mode (DCM) for the power decoupling capability. As a result, the maximum power density is obtained to 1.1 times higher than that of passive topology. However, the total loss of switching devices is 1.5 times higher. Thus, in order to surpass the efficiency of the passive topology by the active power decoupling, the switching device is required to reduce the total loss by 35% compared to the present products.

I. Introduction

In recent years, single-phase grid connected converters has been studied actively as the power conversion systems (PCSs) for the photovoltaics system or battery energy storage system and so on [1-4]. Instantaneous power of the single-phase grid oscillates at twice the grid frequency whereas the output power is constant. As a result, a power ripple with twice the grid frequency occurs at the connection point between the chopper and the inverter. In order to absorb this power ripple, bulky electrolytic capacitors are used in the conventional circuit. However, the electrolytic capacitor limits the lifetime of the PCS [5].

As an alternative power decoupling method, an active power decoupling, which consists of small capacitors, inductors and switching devices, has been proposed [6-8]. As a result, the PCS with long lifetime is expected by using film capacitors or ceramic capacitors as the buffer capacitor. In particular, buck type active buffer circuits, whose the buffer capacitor voltage is lower than DC-link voltage, are actively proposed [9-11]. In these circuit topologies, since the maximum voltage of the buffer capacitor is limited, the reduction of the buffer capacitance has limitations due to the satisfaction of the average stored energy of buffer capacitor $CV^2/2$. Moreover, due to the large effective current of a smoothing inductor, the conduction loss of the switching devices becomes high. As a result, the large cooling system leads to the lower power density system. In order to drastically increase the power density of a single-phase inverter, fans are used to minimize the heatsinks [12]. However, the system lifetime is limited by these fans. Thus, the cooling system is desirable to be designed on the assumption that the natural cooling is applied.

On the other hand, an additional inductor and switching devices for the buffer circuit are required to control the buffer capacitor voltage. By increasing the switching frequency of the buffer circuit, the inductance can be reduced due to the reduction of required store energy of the inductor. However, the

size of the heatsink becomes larger due to the increase of the switching loss. As a result, the relationship between the inductor volume and the heatsink volume results with the trade-off characteristics. Thus, the buffer circuit should be designed and operated at an adequate switching frequency to maximize the power density. However, past literatures which were investigated by authors do not mention clearly the condition to achieve higher efficiency and power density than the electrolytic capacitor topology.

This paper clarifies the conditions to achieve high power density with high efficiency by comparison between the electrolytic capacitor and the active power decoupling topologies. Moreover, a novel circuit topology, which requires no additional inductor for the power decoupling circuit, is proposed. The proposed circuit uses discontinuous current mode (DCM) for the power decoupling capability. This paper is organized as follows; first, the design flow for the passive topology using the electrolytic capacitor and the active buffer topology using the ceramic capacitor is introduced. Second, from the design flowchart and the specifications of the present products, the power density and the efficiency are evaluated by Pareto-front. Third, the requirements for components in the active power decoupling circuit to surpass the passive topology in terms of the efficiency and the power density are clarified. Finally, the power density and the efficiency of the proposed circuit are evaluated by Pareto-front optimization.

II. CIRCUIT CONFIGURATION AND DESIGN METHOD

A. Passive power decoupling circuit

Fig. 1 shows the circuit configuration of a DC to single-phase AC converter with the passive power decoupling method. Table I shows the circuit specifications. This paper evaluates the volume of the buffer circuit based on the ripple current in DC-link.

In the passive topology circuit, the bulky electrolytic capacitor is connected for compensation of the single-phase power ripple. The ripple current restricts the lifetime of the electrolytic capacitor. Therefore, in this paper, the electrolytic capacitor, which has the allowable ripple current higher than the calculated ripple current, is selected. The current which flows into the electrolytic capacitor includes not only the power ripple component but also the switching frequency component from the inverter. The capacitor ripple current is the function of the output power factor angle ϕ and the modulation index m, which is a nonlinear value [13]. Then, the effective value of the capacitor ripple current is expressed by

$$I_{rms\_cap} = K_{cap}(\phi, m) I_m \quad (1),$$

where, I_m is the maximum value of the output current and $K_{cap}(\phi, m)$ is the coefficient which is obtained by simulation.

Fig. 2 shows the simulated result of $K_{cap}(\phi, m)$. $K_{cap}(\phi, m)$ is decided from Fig. 2 as follows. Generally, the output power factor of the grid-connected inverter is approximately unity. The modulation index, which expresses the ratio of the input voltage V_{in} and the maximum output voltage V_m, is 0.74 in this case. Therefore, from Fig. 2, $K_{cap}(1.0, 0.74)$ is 0.56. With the frequency multipliers, the allowable ripple current is calculated by

$$I'_{rms\_cap} = \sqrt{\left(\frac{I_{100\,\mathrm{Hz}}}{K_{100\,\mathrm{Hz}}}\right)^2 + \left(\frac{1}{K_{sw}}\right)^2 \sum_{n=1}^{\infty} I_{nsw}^2} \quad (2),$$

where, $I_{100\mathrm{Hz}}$ is the effective current whose frequencies are twice the grid frequency, I_{nsw} is the effective current at the switching frequency, $K_{100\mathrm{Hz}}$ and K_{sw} are the frequency multipliers at 100 Hz and the switching frequency, respectively. An electrolytic capacitor, which has the allowable ripple current higher than the result of (2), should be required.

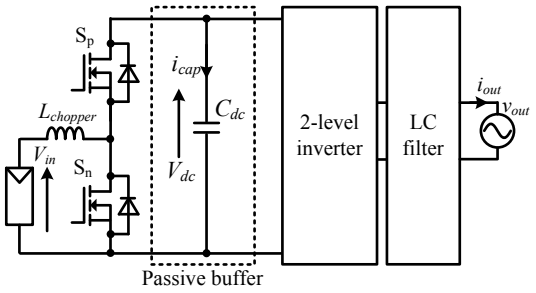


Fig. 1. DC to single-phase AC converter with passive power decoupling circuit.

Table I. System specification.

Parameter	Symbol	Value
Rated power	P_{out}	6 kW
Output voltage	V_{out}	200 V
Output frequency	f_{out}	50 Hz
Power factor	$\cos\phi$	1.0
Input voltage	V_{in}	150 V
DC link voltage	V_{dc}	380 V
Modulation index	m	0.74
Ambient temperature	T_a	40 °C
Junction temperature	T_j	140 °C
CSPI		3 °C/dm^3

B. Boost type active buffer circuit

Fig. 3 shows the relationship among the input power p_{in}, the output power p_{out} and the compensation power p_{buf} in the active buffer. The output instantaneous power is shown in (3) when the output current is the sinusoidal wave with unity power factor.

$$p_{out} = \frac{V_m I_m}{2}(1 - \cos 2\omega_{out} t) \quad (3),$$

where, V_m is the peak voltage of the single-phase grid and ω_{but} is the angular frequency of a grid. From (3), the power ripple, whose frequency is twice the grid frequency, occurs at the DC link. In order to absorb the power ripple, the instantaneous power p_{buf} in the active buffer is controlled according to

$$p_{buf} = \frac{1}{2} V_m I_m \cos 2\omega_{out} t \quad (4).$$

Fig. 4 shows a circuit configuration of an active buffer circuit. In this circuit, because the buffer capacitor voltage is higher than the DC-link voltage, this active power decoupling circuit is classified as the boost type active buffer. The active buffer consists of a boost chopper and a small capacitor C_{buf} which absorbs the power ripple in the DC-link. The active buffer circuit achieves long lifetime because the film capacitors or the ceramic capacitors is used as the buffer capacitor. A small filter capacitor C_f is connected in order to absorb the ripple current at the switching frequency. The principle for the power decoupling between the DC and the AC sides is explained as follows.

Fig. 5 shows the design flowchart in order to design the boost type active buffer. First, the capacitance of the buffer capacitor is calculated based on an average voltage and a voltage oscillation range of the buffer capacitor. Then, the capacitor volume Vol_{Cbuf} is determined from the present products. The switching device is decided based on the maximum voltage of the buffer capacitor. In this paper, the switching device, which has a rating voltage of 1200 V, is used. Second, the boost inductor is designed based on the switching frequency f_{sw} and the inductor ripple current. The volume of the boost inductor is estimated by Area Product concept [14]. Third, the heatsink volume is calculated from the thermal resistance which depends on the conduction loss P_{loss_cond} and the switching loss P_{loss_sw} of the switching devices. Finally, the pareto-front is obtained through varying the switching frequency in order to clarify the maximum power density point.

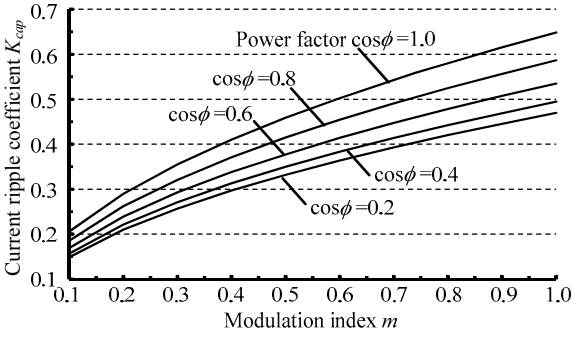


Fig. 2. Current coefficient for the calculation of the ripple current flowing into the electrolytic capacitor.

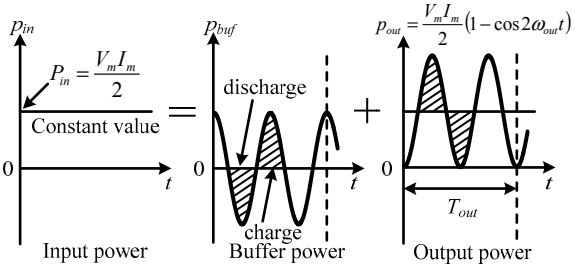


Fig. 3. Single-phase power ripple compensation.

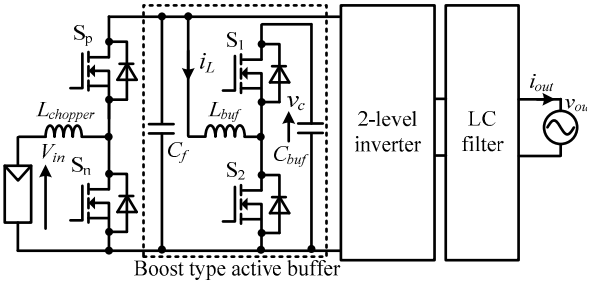


Fig. 4. DC to single-phase AC converter with boost type active buffer circuit.

The selection method of the buffer capacitor is discussed. The capacitance is decided from the relationship between the storage energy P_c and the capacitor voltage. Thus, from the instantaneous power in (4), the capacitance to compensate the power ripple is calculated by

$$C_{buf} = \frac{P_c}{\omega_{out} V_{ave} \Delta V_c} \quad (5),$$

where V_{ave} is the average voltage and ΔV_c is the voltage oscillation range of the buffer capacitor.

In passive topology circuit with the bulky electrolytic capacitor, the storage power is achieved by the large capacitance. On the other hand, in the active buffer, the storage power is achieved through the large ΔV_c. This is the principle to reduce the capacitance with active power decoupling method.

The buffer capacitor requires the large V_{ave} and ΔV_c for reducing the capacitance. However, when the buffer capacitor voltage is increased, the switching device with the high rating voltage is required. In this paper, the switching device which has the rating voltage of 1200 V is selected as the peak capacitor voltage is designed at 800 V.

The boost inductor is designed based on the ripple current Δi_L. The inductance becomes the maximum value when the difference between the input voltage and the buffer capacitor voltage reaches the

maximum. Thus, the inductance of the boost inductor is provided by

$$L_{buf} = \frac{V_{dc}}{\Delta i_L f_{sw}} \frac{\left(V_{ave} + \frac{\Delta V_c}{2}\right) - V_{dc}}{V_{ave} + \frac{\Delta V_c}{2}} \quad (6).$$

The inductor volume depends on many parameters of the components. There are several ways to select the core for the inductor. In this paper, the boost inductor is designed by Area Product concept using the window area and the cross-sectional area [14]. Therefore, the volume of the boost inductor Vol_{Lbuf} is calculated by

$$Vol_{Lbuf} = K_v \left(\frac{L_{buf} I_{\max}^2}{K_u B_{\max} J} \right)^{\frac{3}{4}} \quad (7),$$

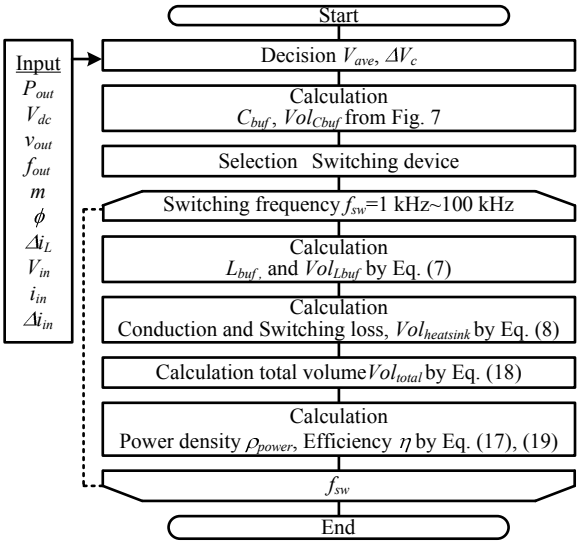


Fig. 5. Designing flow for active buffer circuit.

where, K_v is the volume coefficient depending on the shape of cores, I_{max} is the maximum current flowing to the inductor, K_u is the window utilization factor, B_{max} is the maximum flux density of the core, and J is the current density of the wire.

The switching devices require a cooling system such as heatsinks and fans. In general, the cooling system is designed based on the thermal resistance. CSPI (Cooling System Performance Index) is introduced to estimate the volume of cooling system [15]. CSPI means the cooling performance per unit volume of the cooling system. The cooling system is miniaturized when CSPI become higher. The volume of the cooling system $Vol_{heatsink}$ is provided by

$$Vol_{heatsink} = \frac{1}{R_{th(f-a)} CSPI} \quad (8),$$

where, $R_{th(f\text{-}a)}$ is the thermal resistance of the cooling system which is given by

$$R_{th(f-a)} = \frac{T_j - T_a}{P_{loss}} - \left(R_{th(j-c)} + R_{th(c-f)}\right) \quad (9),$$

where, T_j is the junction temperature of the switching device, and T_a is the ambient temperature. The total loss P_{loss}, which is composed of the conduction loss P_{loss_cond} and the switching loss P_{loss_sw} from the switching devices, is calculated by

$$P_{loss} = P_{loss\_cond} + P_{loss\_sw} \quad (10),$$

where, P_{loss_cond} and P_{loss_sw} are given by

$$P_{loss\_cond} = \frac{1}{T_{out}} \int_0^{T_{out}} i_L^2 r_{on} dt \quad (11),$$

$$P_{loss\_sw} = \frac{e_{on} + e_{off}}{E_{dcd} I_{md}} f_{sw} \frac{1}{T_{out}} \int_0^{T_{out}} v_c i_L dt \quad (12),$$

respectively, where, T_{out} is the period time of the grid, r_{on} is the on resistance of the switching device, f_{sw} is the switching frequency of the active buffer, e_{on} and e_{off} is the turn-on and turn-off energy per switching from datasheet respectively, E_{dcd} and I_{md} are the voltage and the current under the measurement condition of the switching loss from the datasheet. The buffer capacitor voltage v_c and the boost inductor current i_L is expressed by

$$v_c = V_{ave} + \Delta V_c \cos\left(2\omega_{out} t\right) \quad (13),$$

$$i_L = \frac{V_{ave}}{V_{in}} C_{buf} \frac{dv_c}{dt} \quad (14),$$

respectively. From (12), the increase in the switching frequency leads to the increase in the switching loss. The cooling performance can be improved by fans to minimize the heatsinks. However, the system lifetime is limited by these fans. Thus, in this paper, the cooling system is designed on the assumption that the natural cooling is applied.

C. Buck type active buffer circuit

Fig. 6 shows a circuit configuration of an active buffer circuit. Because the buffer capacitor voltage is lower than the DC-link voltage, this circuit is classified as a buck type active buffer. The buck type active buffer can also be designed through the flowchart in Fig. 5.

The buffer capacitor is designed by (5). However, the DC-link voltage limits the peak voltage of the buffer capacitor. As a result, the buffer capacitance is larger than the one of the boost type active buffer.

The inductance of the smoothing inductor reaches the maximum value when the capacitor voltage is a half of the input voltage. Thus, the inductance is designed by

$$L_{buf} = \frac{V_{in}}{4\Delta i_L f_{sw}} \quad (15),$$

where, i_L is the smoothing inductor current which is provided by

$$i_L = C_{buf}\frac{dv_c}{dt} = \frac{P_{out}}{V_{ave}}\sin(2\omega_{out}t) \quad (16).$$

The volume of the smoothing inductor is estimated by Area Product of (7). The loss generated by the switching devices is calculated by substituting (16) to (10), (11) and (12).

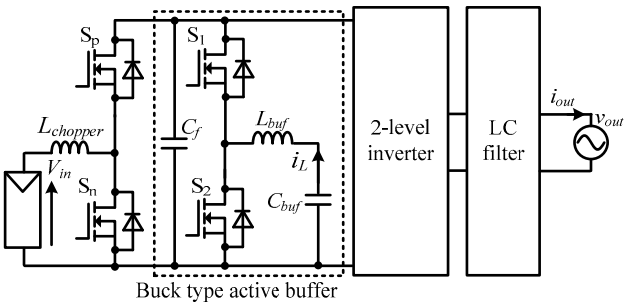


Fig. 6. DC to single-phase AC converter with buck type active buffer circuit.

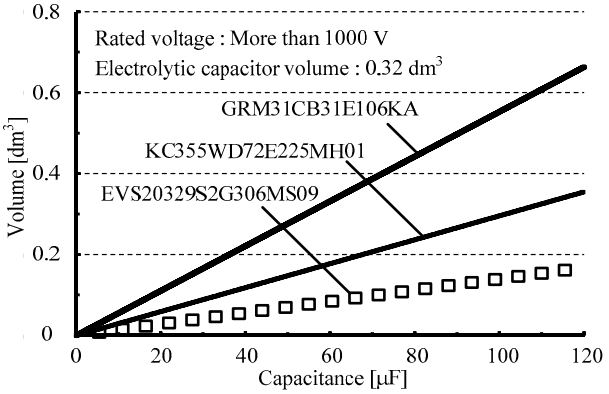


Fig. 7. Relationship between capacitor volume and capacitance.

III. Efficiency and Power Density Evaluation

A. Comparison of Pareto-front for buffer circuit

In the passive topology circuit, the electrolytic capacitor connected to the DC-link is selected based on (2). The allowable ripple current becomes 18.7 A on the assumption that K_{100Hz}=1.0 and K_{sw}=1.4. Thus, the electrolytic capacitor, which has the allowable ripple current larger than 18.7 A, is selected. When the rating voltage of the electrolytic capacitor is fixed, the volume of the electrolytic capacitor becomes smaller by connecting the capacitors with small allowable ripple current in parallel [16]. In this paper, 28 electrolytic capacitors, which have the allowable ripple current of 1 A per one capacitor, are connected in parallel with a ripple current margin of 50%. As a result, the total capacitance is 5040 μF.

Fig. 7 shows a relationship between the capacitance and the total volume when the ceramic capacitors are connected in parallel. In the active buffer, the ceramic capacitor is used as the buffer capacitor in term of the high energy density. The DC bias characteristic, which is the decrease in the capacitance of the ceramic capacitor by DC bias, has been considered in Fig. 7. Comparing to the electrolytic capacitor, the ceramic capacitor has the higher ratio between the allowable ripple current and the capacitance. Therefore, when the requirement of the capacitance for the power decoupling is satisfied, the allowable ripple current is sufficient for the ceramic capacitor. Specifically, when the average voltage V_{ave} and the voltage amplitude ΔV_c are 600 V and 200 V respectively, the capacitance C_{buf} is 79.6 μF. The volumes of capacitors of GRM series and KC series (Murata Manufacturing Co., Ltd.) are 0.23 dm^3 and 0.44 dm^3 respectively in the total capacitance of 79.6 μF. However, the required numbers of the ceramic capacitor are 1136 and 13440 respectively, which are not realistic. On the other hand, when a ceramic capacitor of the EVS series (Murata Manufacturing Co., Ltd.) is applied, the total volume and the required number are 0.11 dm^3 and 45 in 79.6 μF. Therefore, the EVS series capacitor (Murata Manufacturing Co., Ltd.) is used in this paper.

Table II shows the selected components. Fig. 8 shows the pareto-front of the power density ρ_{power} and the efficiency η with the switching frequency f_{sw} as a variable. The power density is calculated by (17) from the total volume of (18). The efficiency η is provided by (19).

$$\rho_{power} = \frac{P_{out}}{Vol_{total}} \quad (17),$$

$$Vol_{total} = Vol_{Lbuf} + Vol_{Cbuf} + Vol_{sw} + Vol_{heatsink} \quad (18),$$

$$\eta = \frac{P_{out}}{P_{out} + \left(P_{loss} + P_{loss\_Cbuf} + P_{loss\_Cf}\right)} \quad (19),$$

where, Vol_{Cbuf} and Vol_{sw} are the volumes of the buffer capacitor and the package of the switching device. The power density reaches the maximum value, when SiC-MOSFET is used in the boost type active buffer at 30 kHz. Specifically, the maximum power density of 17.0 kW/dm^3 are achieved with the efficiency of 99.5%. On the other hand, the power density in the passive topology, which is 18.8 kW/dm^{3}and the efficiency of 99.8%, is 1.4 times higher than that of the active buffer.

B. Volume comparison

Fig. 9 shows the volume ratio of components at the maximum power density point. The component volume is normalized with the volume of the electrolytic capacitors as 100%. The buffer capacitor size is reduced by 64% compared to bulky electrolytic capacitors by the active power decoupling. However, the volumes of the heatsink for the switching device and the boost inductor are 35% and 41% compared to the electrolytic capacitors, respectively. By increasing the switching frequency, the boost inductor size can be reduced. However, the cooling system size increases due to the increase of the switching loss. As a result, the maximum power density of the active buffer is 90% against the one of the passive topology.

C. Loss comparison

Fig. 10 shows the power loss ratio at the maximum power density point. The loss caused by the boost inductor is ignored. The loss is normalized with the loss of the passive topology. In the passive topology, the conduction loss, which is caused by the equivalent series resistance (ESR) of the electrolytic capacitors, is considered. The power loss of the active buffer is 135% in comparison with the one of the passive topology.

Table II. Selected components.

Circuit	Part	Marking	Maximum rating
Passive buffer	C_{in}	Nippon Chemi-Con EKMZ451VSN181MP30S	450 V, 1.0 Arms 180 μF
Boost type active buffer	C_{buf}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF
	C_f	Murata Manufacturing KC355WD72E225MH01	450 V 1 μF
	S_1 S_2	ROHM SiC-MOSFET, SCH2080KE	1200 V 40 A
		Fuji Electric IGBT, FGW30N120HD	1200 V 30 A
		Fuji Electric Si-MOSFET, FMH30N60S1	600 V(2 series connection),30 A
Buck type	S_1 S_2	ROHM SiC-MOSFET, SCT2120AF	650 V 29 A
Boost chopper	S_p S_n	ROHM SiC-MOSFET, SCT120AF	650 V 29 A
Proposed circuit	S_1 -S_4	CREE SiC-MOSFET,C2M0025120D	1200 V 60 A

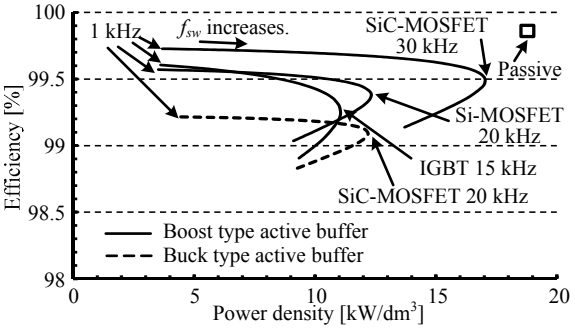


Fig. 8. Pareto-front of passive and active buffer circuit.

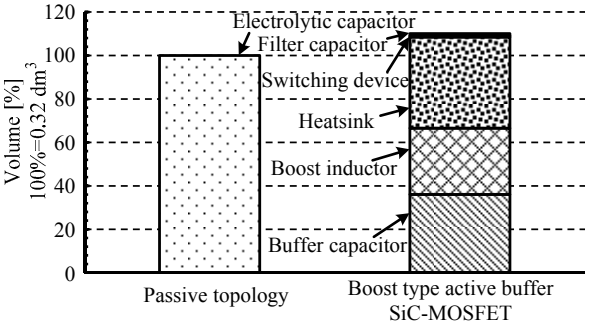


Fig. 9. Volume distribution (f_{sw}=30 kHz).

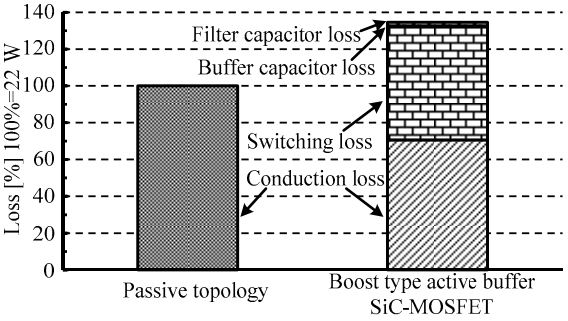


Fig. 10. Loss distribution (f_{sw}=30 kHz).

IV. Requirements for Components

The requirements for the power decoupling components in the active buffer to surpass the passive topology in term of the efficiency and the power density are discussed.

From Fig. 9, the total volume of the active buffer should be reduced to 90% of that of the present products. Thus, the ceramic capacitor, whose the capacitance per unit volume is 1.4 times higher than the present products, is required. Otherwise, the ceramic capacitor, which has the high rated voltage as

same as the film capacitor with the rated voltage of 630 V, can reduce the series numbers of 3 to 2. As a result, the total volume reduces by 33%. On the other hand, the boost inductor size should be reduced by improving the circuit topology. For example, by sharing the boost inductor with a boost chopper or a single-phase inverter, the additional inductor for the power decoupling can be omitted. Finally, a power decoupling topology of the boost type, which can reduce the inductor volumes less than 90%, is required.

From Fig. 10, a switching device, which can reduce the total loss to 74% of the present products, is required. In particular, the on resistance and the switching loss are less than 92 mΩ and 166 μJ, respectively, under the condition of 1200 V rating voltage and 40 A rating current at 140 ˚C. On the other hand, as an example of the improving method for circuit topologies, the switches for the buffer capacitor voltage control are shared with a boost chopper.

V. Proposed Boost-Type Active-Buffer Circuit Operated in DCM

A. Circuit configuration and design

Fig. 11 shows a DC-DC converter which integrates a power decoupling capability. This circuit requires no additional inductor for the power decoupling circuit. When the boost chopper operates in the continuous current mode (CCM), the discharge mode for the buffer capacitor cannot be realized because the direction of the current cannot be changed suddenly in CCM. Thus, this paper came up with the idea that the charge and discharge modes are realized by the discontinuous current mode (DCM). In particular, the zero-current period is utilized for the operation of power decoupling. By using the zero-current period, the DC-link voltage and the buffer voltage are controlled by only one boost inductor.

Fig. 12 shows inductor current waveform in the DCM active power decoupling circuit. The average current of the boost inductor is the sum of the average current for the DC-link voltage control $i_{L\_ave\_dc}$ and the buffer capacitor voltage control $i_{L\_ave\_buf}$.

$$i_{L\_ave} = i_{L\_ave\_dc} + i_{L\_ave\_buf} \tag{20},$$

where, $i_{L\_ave\_dc}$ is given by

$$i_{L\_ave\_dc} = \frac{i_{peak\_dc}}{2}(d_1 + d_2) = \frac{P_{out}}{V_{in}}\{1 - \cos(2\omega_{out}t)\} \tag{21},$$

where, d_1 and d_2 are the on duties of S_1 and S_3. Thus, the input average current without the power decoupling oscillates at twice the grid frequency. In order that the average current becomes constant value, $i_{L\_ave\_buf}$ is given by

$$i_{L\_ave\_buf} = \frac{i_{peak\_buf}}{2}(d_3 + d_4) = \frac{P_{out}}{V_{in}}\cos(2\omega_{out}t) \tag{22},$$

where, d_3 and d_4 are the on duties of S_1 and S_2 for the buffer capacitor voltage control.

On the other hand, the conduction loss is calculated from (11) and duties d_1~d_4. From Fig. 8, the switching loss of a turn-off caused by switching devices are calculated by

$$P_{sw\_off\_dc} = \frac{e_{off}}{E_{dcd} I_{md}} f_{sw} \frac{1}{T_{out}} \int_0^{T_{out}} V_{dc} i_{peak\_dc} dt \tag{23},$$

$$P_{sw\_off\_buf} = \frac{e_{off}}{E_{dcd} I_{md}} f_{sw} \frac{1}{T_{out}} \int_0^{T_{out}} v_c i_{peak\_buf} dt \tag{24},$$

where, i_{peak_dc} and i_{peak_buf} are current peaks of the boost inductor for the DC-link voltage control and the buffer capacitor voltage control, respectively.

When the switch S_1 and S_2 are turned on, the recovery loss in the free-wheeling diode (FWD) does not occur because the FWD is turned off naturally in DCM. However, the turn-on losses are caused by the discharge of the parasitic capacitor, and are calculated by

$$P_{sw\_on\_S1} = \frac{3}{4} C_{ds} V_{in}^2 f_{sw} \tag{25},$$

$$P_{sw\_on\_S2} = \frac{1}{4} C_{ds} (v_c - V_{in})^2 f_{sw} \tag{26},$$

where, C_{ds} is the capacitance between the drain and the source of the switching device.

In order to avoid an interference between the voltage controls, in Fig. 12, the total of the duties is

$$d_1 + d_2 + d_3 + d_4 \le 1 \tag{27}.$$

When (27) is equal to 1, this circuit operates in the critical current mode. In the critical condition, the current ripple of the boost inductor becomes the minimum, which leads to the minimum of the conduction loss. Thus, in this paper, the inductance of the boost inductor is designed based on the critical condition at the rated power, and is calculated by

$$L_{boost} = \frac{V_{in}^2(\alpha_{di}-1)}{4 f_{sw} P_{out} \alpha_{di}\left(1+\sqrt{\frac{\alpha_{bd}}{2}\frac{\alpha_{di}-1}{\alpha_{di}\alpha_{bd}-1}}\right)^2} \quad (28),$$

where, α_{bd} is the boost ratio of the average voltage of the buffer capacitor to the DC-link voltage, and α_{di} is the boost ratio of the DC-link voltage to the input voltage.

Fig. 13 presents the operation waveforms when a prototype of 600 W is operated. The boost inductor current oscillates at twice the grid frequency when the power decoupling is not applied. On the other hand, the buffer capacitor voltage with the power decoupling control is oscillated at twice the grid frequency. As a result, the single-phase power ripple can be compensated by the active power decoupling, which is confirmed by the significant ripple reduction in the boost inductor current.

Fig. 14 shows the enlarged operation waveforms with the power decoupling control. The realization of the charge and the discharge modes for the buffer capacitor by DCM is confirmed.

Fig. 15 shows the harmonics analysis result of the boost inductor current. When the power decoupling is applied, the second order harmonic component is reduced by 78.3% compared to that without power decoupling. Thus, the compensation of the single-phase power fluctuation is confirmed.

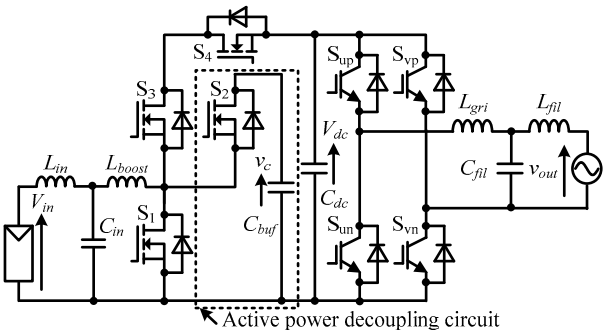
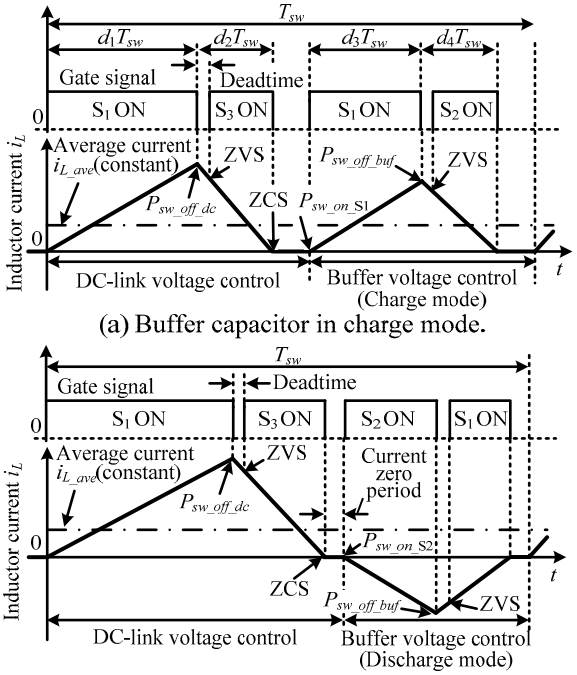


Fig. 11. DCM active-power-decoupling circuit.



(a) Buffer capacitor in charge mode.

(b) Buffer capacitor in discharge mode.

Fig. 12. Boost inductor current waveform in DCM active-power-decoupling circuit.

B. Comparison of Pareto-front of DC-DC converter with power decoupling capability

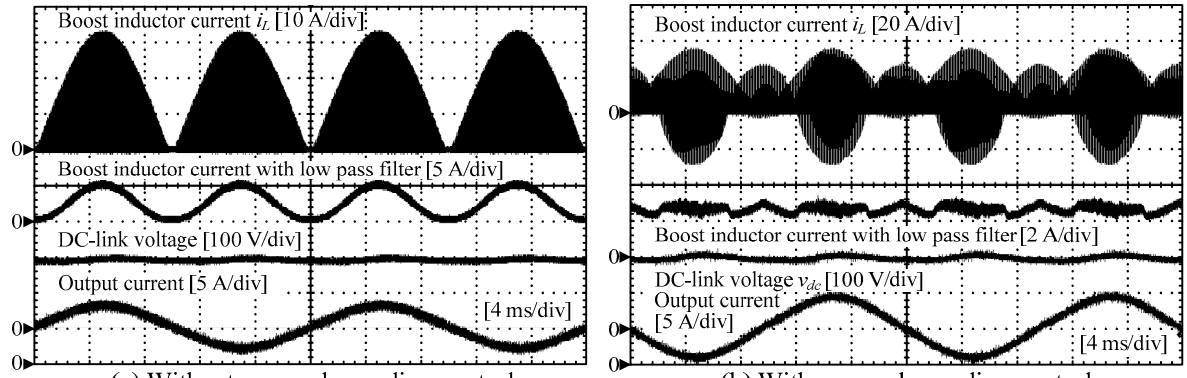
Fig. 16 shows the pareto-front of ρ_{power} and η with f_{sw} as variable. In Fig. 16, the volume of the passive topology, the boost type and the buck type active buffer circuit includes the volume of the boost chopper components. The maximum power density of the boost chopper with the passive buffer is 4.1 kW/dm^3 with the efficiency of 98.9% at the switching frequency of 30 kHz. On the other hand, the power density of the DCM active-power-decoupling circuit reaches the maximum value, when the switching frequency is 25 kHz. Specifically, the maximum power density of 4.6 kW/dm^3 is achieved with the efficiency of 98.3%, and is 1.1 times higher than the power density of the passive topology.

C. Volume and loss analysis of DC-DC converter with power decoupling capability

Fig. 17 shows the volume distribution of components at the maximum power density point. The component volume is normalized with the volume of the passive topology as 100%. The volume of the boost inductor of the DCM active-power-decoupling circuit is 63% of that of the boost chopper. As a result, the total volume of the DCM active power decoupling circuit is 91% against that of the passive topology.

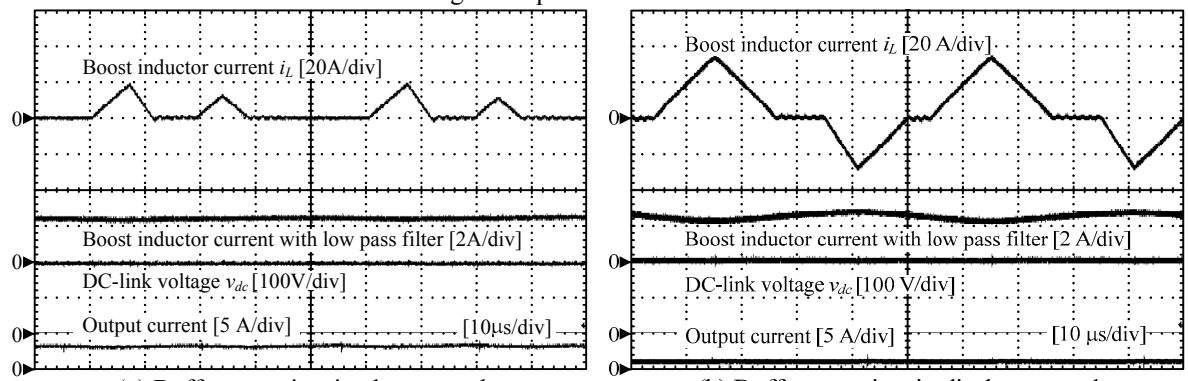
Fig. 18 shows the power loss distribution at the maximum power density point. The total loss of the DCM active-power-decoupling circuit is 154% in comparison with that of the passive topology. Note that the loss caused by the boost inductor is ignored. In order that the efficiency of the DCM active-

power-decoupling circuit surpasses the one of passive topology, a switching device, which can reduce the total loss to 65% of the present products, is required. In particular, the on resistance and the turn-off loss are less than 26 mΩ and 234 μJ, respectively, under the condition of 1200 V rating voltage and 40 A rating current at 140 ˚C of the junction temperature.



(a) Without power decoupling control (b) With power decoupling control

Fig. 13. Operation waveforms.



(a) Buffer capacitor in charge mode. (b) Buffer capacitor in discharge mode.

Fig. 14. Enlarged operation waveforms with power decoupling control.

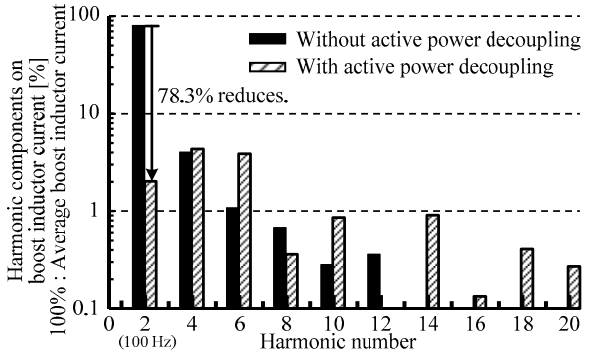


Fig. 15. Harmonics analysis on boost inductor current.

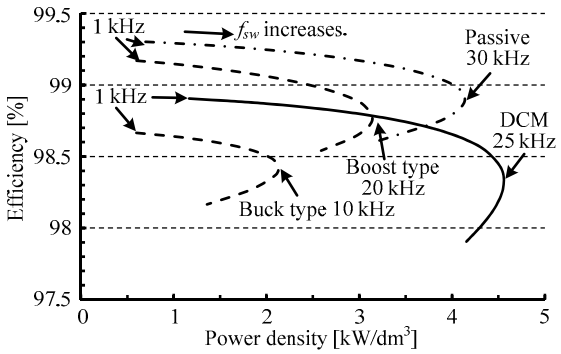


Fig. 16. Pareto-front of DC-DC converter with power decoupling capability.

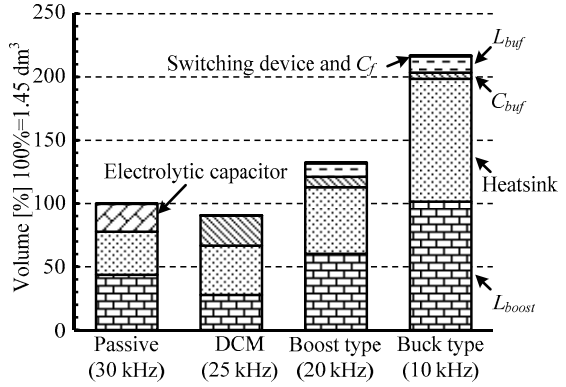


Fig. 17. Volume distribution of DC-DC converter.

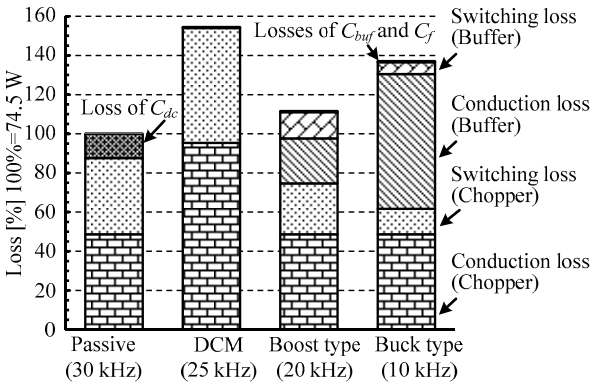


Fig. 18. Loss distribution of DC-DC converter.

V. Conclusion

This paper discussed how to achieve high power density with high efficiency for single-phase inverter with active power decoupling circuit. Based on the Pareto optimization of power density and efficiency, the maximum power density points of the power decoupling circuits are clarified. The problems of the conventional boost type active buffer are following;

- The maximum power density is 90% of that of the passive topology which uses electrolytic capacitors.
- The power loss caused by switching devices is 135% of that of the passive topology.

As a result, the circuit topology of the active power decoupling which can reduce the total component volume less than 90%, especially the boost inductor volume, is required. Thus, this paper proposed a new DC-DC converter which uses discontinuous current mode for the power decoupling capability. The features of the proposed circuit are following;

- The proposed circuit requires no additional inductor for the power decoupling circuit.
- The maximum power density is 1.1 times higher than that of the passive topology.
- The power loss caused by switching devices is 1.5 times higher than that of the passive topology.

As a result, in order to surpass the efficiency of the passive topology by active power decoupling, the switching device is required to reduce the total loss by 35% compared to the present products.

In future work, the power density and the efficiency of the proposed circuit are evaluated by experiments in 6 kW.

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