Reduction of Input Current Harmonics based on Space Vector Modulation for Three-phase VSI with varied Power Factor

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***Abstract*—This paper proposes space vector modulation (SVM) which reduces the current harmonics flowing through the DC-link capacitor of three-phase motor drive systems. In a conventional SVM, the selection of the space vectors results in the long zero vector period, which increases the inverter input current harmonics. On the other hand, in the proposed SVM, the space vectors are selected in order to actively shorten the zero vector period. Furthermore, by applying the proposed SVM only in the regions where the instantaneous value of the input current is positive, the input current harmonics are reduced even when the load power factor becomes low. Through the experiment applying the proposed SVM, it is confirmed that input current harmonics is reduced by up to 33.9% of that of the conventional method. Moreover, it is confirmed that the input current harmonics with the proposed SVM are reduced in all range of the load power factor compared to that of the conventional SVM.**

Keywords—DC link capacitor; input current harmonics; space vector modulation; two-level, VSI

I. INTRODUCTION

Three-phase AC motors are widely utilized in the industrial and household applications [1-5]. In recent years, the researches -aiming for long lifetime of the three-phase inverter in the motor drive system have been actively conducted [6]. The smoothing capacitor connected to the DC-link of the inverter is required to have a large capacitance in order to smooth the DC-link voltage. Generally, an electrolytic capacitor is used as the smoothing capacitor which absorbs the high harmonics of the DC-link current. The electrolyte of the electrolytic capacitor deteriorates by these harmonic components flowing into the electrolytic capacitor. As a result, the lifetime of the electrolytic capacitor decreases due to these high harmonics of the DC-link current, i.e. the input current of the three-phase voltage source inverter (VSI).

In order to extend the lifetime of the smoothing capacitor, the method to use film capacitors as the smoothing capacitor has been proposed [7]. However, the motor drive system becomes bulky because the energy density of the film capacitor is much smaller than that of the electrolytic capacitor. On the other hand, the modulation methods to reduce the input current harmonics of the three-phase VSI have also been proposed [8-9]. The input current harmonics are reduced by minimizing the applied time of the zero vector as much as possible in each switching period. However, the input current harmonics cannot be reduced by these modulation methods when the power factor is low because the current in the DC-link capacitor is drastically increased by applying these modulation methods when the power factor is lower than 0.866 [9]. Thus, these modulation methods cannot be applied to the motor drive system, the power factor variation of which is considerably wide.

This paper proposes a new space vector modulation (SVM) which reduces the input current harmonics of the three-phase VSI over all range of the power factor. The proposed SVM achieves the reduction of the input current harmonics by selecting space vectors with the consideration that the zero vector period is minimized. This paper is organized as follows, first, the reduction of the input current harmonics by minimizing the zero vector period is explained, then, the mechanism of the proposed SVM for the variation of the power factor is proposed. Finally, the effectiveness of the proposed SVM is confirmed by simulation and experiment at the time of driving mode with induction motor.

II. CONVENTIONAL AND PROPOSED SVM

A. Conventional SVM

Fig. 1 shows a three-phase VSI. This inverter consists of three half bridges. Switching state of each half bridge is expressed as following switching functions.

$$s_x = \begin{cases} 1, & (\mathrm{S}_{xp} : \mathrm{ON}, \mathrm{S}_{xn} : \mathrm{OFF}) \\ 0, & (\mathrm{S}_{xp} : \mathrm{OFF}, \mathrm{S}_{xn} : \mathrm{ON}) \end{cases}, \quad (x = u, v, w) \qquad (1)$$

Output currents of inverter at steady state are expressed as

$$\begin{cases} i_u = I_m \cos(\theta - \varphi) \\ i_v = I_m \cos\left(\theta - \varphi - \dfrac{2\pi}{3}\right) \\ i_w = I_m \cos\left(\theta - \varphi + \dfrac{2\pi}{3}\right) \end{cases} \quad (2)$$

where, I_m is the maximum value of output current, θ is phase angle and φ is load power factor angle, respectively.

Fig. 2 shows the definitions of the conventional SVM. Fig. 2(a) and 2(b) are the space vectors of the inverter in $\alpha\beta$ plane and the sector definition of the conventional SVM, respectively. In particular, there are eight fundamental vectors (six active vectors and two zero vectors) and each fundamental vector can be expressed by using switching functions as $\mathbf{V}(s_u\, s_v\, s_w)$. The $\alpha\beta$ plane area where three-phase VSI can output is divided into six sectors (sector 1 ~ 6) in every 60 degrees of the voltage reference vector's phase angle. The voltage reference vector can be expressed with modulation index (m) and phase angle as below.

$$\mathbf{V}^* = m\angle\theta \quad (3)$$

The voltage reference vector sampled in each control period (T_s) is generated by synthesizing three time-averaged fundamental vectors $\mathbf{V_a}$, $\mathbf{V_b}$, $\mathbf{V_c}$ as following equations.

$$\begin{aligned} \mathbf{V}^* &= \frac{t_a}{T_s}\mathbf{V_a} + \frac{t_b}{T_s}\mathbf{V_b} + \frac{t_c}{T_s}\mathbf{V_c} \\ T_s &= t_a + t_b + t_c \end{aligned} \quad (4)$$

where, t_a, t_b, t_c are on duty of each selected fundamental vectors and a, b, c mean the number of selected fundamental vector.

Fig. 3 shows the conventional SVM. Fig. 3(a) and 3(b) are the conventional generation of the voltage reference vector and the input current waveform with the conventional SVM, respectively. In the conventional SVM, the voltage reference vector ($\mathbf{V}^*$) is generated by using two adjacent active vectors, i.e. $\mathbf{V_1}$ and $\mathbf{V_2}$ as shown in Fig. 3(a), and one zero vector ($\mathbf{V_0}$) at each control period when the voltage reference vector is in the sector 1 [10]. In other words, three fundamental vectors which are the closest to the voltage reference vector ($\mathbf{V}^*$) are used in order to generate the voltage reference vector in the conventional SVM. Consequently, the applied time of the zero vector (t_0 or t_7) becomes maximum. During the zero vector period, the input current of the inverter becomes zero, which results in the high step change of the input current waveform. This leads to the increase in the input current harmonics. Therefore, in order to reduce the input current harmonics, the period of the zero vector is required to be minimized.

B. Evaluation for Input Current Harmonics

An Instantaneous value of the inverter input current can be calculated from switching functions and output current as following [11].

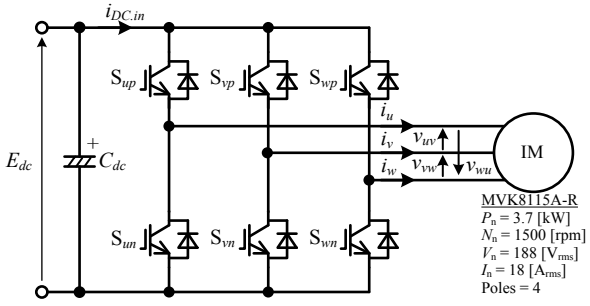
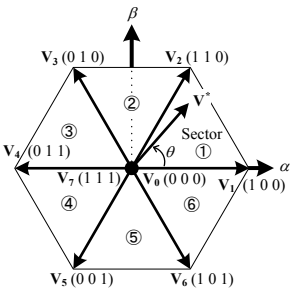


Fig. 1. Three-phase VSI with motor load.

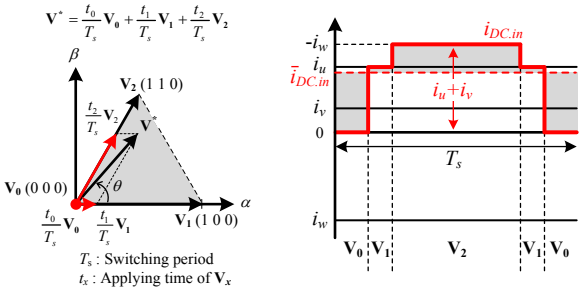


(a) Space vectors in $\alpha\beta$ plane.

Sector	Phase angle
①	$0° < \theta \le 60°$
②	$60° < \theta \le 120°$
③	$120° < \theta \le 180°$
④	$180° < \theta \le 240°$
⑤	$240° < \theta \le 300°$
⑥	$300° < \theta \le 360°$

(b) Sector definition.

Fig. 2. Definitions of conventional SVM.



(a) Generation of voltage reference vector. (b) Waveform of input current.

Fig. 3. Conventional SVM.

$$i_{DC.in} = \sum_{x=u,v,w}(c_x \times i_x) \quad (5)$$

Since the input side of three-phase VSI operates at six-fold fundamental frequency, calculating the rms value of the inverter input current over a sixth of the fundamental period.

$$i_{DC.in.RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}i_{DC.in,k}^2\right)d\theta} \quad (6)$$

where, t_k is the on duty of selected fundamental vector and $i_{DC.in,k}$ is the instantaneous value of the inverter input current when selected fundamental vector is applied.

Then, the average value of the inverter input current over a sixth of the fundamental period can be calculated as following.

$$\begin{aligned}\bar{i}_{DC.in} &= \frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}i_{DC.in,k}\right)d\theta \\ &= \frac{3}{4}m\cdot I_m\cos\varphi\end{aligned} \tag{7}$$

The rms value of the current flowing into the smoothing capacitor can be calculated by using (6) and (7) as following.

$$i_{C.RMS} = \sqrt{i_{DC.in.RMS}^2 - \bar{i}_{DC.in}^2} \tag{8}$$

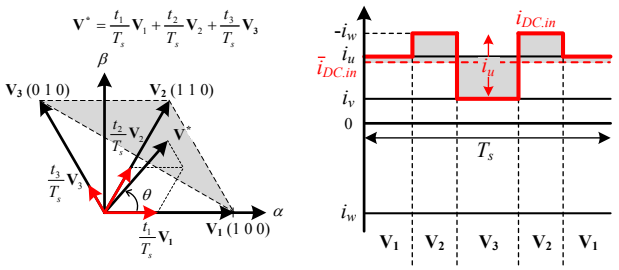
From (6), it is understood that the rms value of the inverter input current changes according to the choice of fundamental vectors. On the other hand, from (7), it is understood that the average value of the inverter input current dose not depend on the choice of fundamental vectors, but the modulation index and the load power factor. In other words, the average value of the inverter input current is constant regardless of the choice of fundamental vectors. Therefore, by selecting fundamental vectors in order to minimize the rms value of the inverter input current, the rms value of the smoothing capacitor current is also minimized. To analyze the optimized vector patterns for a minimum rms value of the inverter input current, the rms value of the inverter input current over a control period, derived from (6), is used for the analysis [12].

$$\begin{aligned}i_{DC.in.RMS}(T_s) &= \sqrt{\frac{1}{T_s}\int_0^{T_s}\left(i_{DC.in}^2\right)dt} \\ &= \sqrt{\sum_{k=a,b,c}\frac{t_k}{T_s}\left(i_{DC.in,k}^2\right)}\end{aligned} \tag{9}$$

Note that the smaller the difference between the instantaneous value and average value of input current (shown by the colored area in Fig. 3(b)) is, the smaller the value of (9) becomes. Additionally, the value of (9) is independent from the switching period. Therefore, the rms value of the inverter input current is independent from the switching frequency.

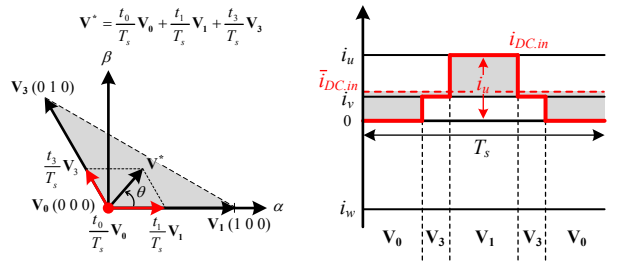
C. Reduction Method for Input Current Harmonics

Fig. 4 shows an optimized vector pattern for the minimum rms value of the inverter input current when i_u and i_v are positive and i_w is negative in the case of the high modulation index. As shown in Fig. 4(a), three consecutive active vectors ($\mathbf{V_1}$, $\mathbf{V_2}$ and $\mathbf{V_3}$) are used to generate the voltage reference vector, which results in the elimination of the zero vector [8]. Note that, the elimination of the zero vector is achieved only when the tip of voltage reference vector belongs to the triangle formed by the tips of three consecutive fundamental vectors ($\mathbf{V_1}$, $\mathbf{V_2}$ and $\mathbf{V_3}$) as shown by the colored area in Fig. 4(a), i.e. in the case of high modulation index. Besides, the area that can be output by using three consecutive fundamental vectors is same as the conventional SVM. Thus, the optimized vector patterns for the minimum rms value of the inverter input current allows to obtain the same output voltage limits as the conventional SVM. Fig. 4(b) shows the waveform of the input current with the optimized vector pattern when i_u and i_v are positive and i_w is negative in the case of the high modulation index. The difference between the instantaneous value and average value of the input current as shown by the colored area in Fig. 4(b) is smaller than that in Fig. 3(b). Thus, the input current harmonics are reduced at most with this optimized selection of the fundamental vectors [13].



(a) Generation of voltage reference vector. (b) Waveform of input current.

Fig. 4. Optimized vector pattern for a minimum minimum rms value of inverter input current when i_u and i_v are positive and i_w is negative in the case of high modulation index.



(a) Generation of voltage reference vector. (b) Waveform of input current.

Fig. 5. Optimized vector pattern for a minimum minimum rms value of inverter input current when i_u and i_v are positive and i_w is negative in the case of low modulation index.

Fig. 5 shows the optimized vector pattern for the minimum rms value of the inverter input current when i_u and i_v are positive and i_w is negative in the case of the low modulation index. As shown in Fig. 5(a), one active vector ($\mathbf{V_1}$), one non-adjacent active vector ($\mathbf{V_3}$) and one zero vector ($\mathbf{V_0}$) are used in order to generate the voltage reference vector in the proposed SVM [9]. When the tip of voltage reference vector belongs to the triangle formed by the tips of these three fundamental vectors ($\mathbf{V_1}$, $\mathbf{V_3}$ and $\mathbf{V_0}$), i.e. the case of the low modulation index, the elimination of the zero vector cannot be achieved. However, the period of the zero vector can be reduced by selecting a non-adjacent active vector ($\mathbf{V_3}$) instead of the adjacent active vector ($\mathbf{V_2}$). Consequently, the difference between the instantaneous value and average value of input current as shown by the colored area in Fig. 5(b) becomes small. This reduces the input current harmonics compared with that of the conventional SVM even when modulation index is low.

D. *Approach to deal with variation of Load Power Factor*

As discussed in the previous section, the fundamental vectors are selected so that the zero vector periods are minimized for reducing the rms value of the inverter input current. However, when the power factor becomes low, the minimization of the zero vector period no longer reduces the input current harmonics.

Table 1 shows sector definitions of the proposed SVM. The sectors of the proposed SVM (A ~ F) are determined by the combination of the inverter three-phase output current's polarities, i.e. i_u, i_v and i_w. When load power factor changes and the magnitude relations of the output currents also changes, it is necessary to select the fundamental vectors so that the zero vector periods are minimized according to these changes. The vector patterns in Fig. 4 and Fig. 5 are effective to minimize the rms value of the inverter input current only when i_u and i_v are positive and i_w is negative, i.e. at sector B. Thus, by determining the sector from the magnitude relations of the output currents as Table 1, the vector patterns whose the rms value of the the inverter input current is minimum at that moment can be applied corresponding to the load power factor change without detecting the load power factor (cosφ). In particular, the sector of the proposed SVM is shifted corresponding to the phase angle of the output currents.

Table 2 shows the switching table of modulation method. When the power factor is lower than 0.866, i.e. the power factor angle (φ) is larger than 30 degrees, the areas which cannot be modulated by the optimized vector patterns occur. Therefore, the conventional SVM is selected in these periods. In order to solve this problem, first, these periods where the optimized vector patterns cannot be applied are determined by the sector information of the conventional and proposed SVM, then the conventional SVM is applied in these periods.

Fig. 6 shows the waveforms of the output voltage references, the output currents and the input current with the proposed SVM (Left hand) and space vector map of proposed SVM (Right hand) at different load power factors. Fig. 6(a) and 6(b) shows the cases of φ = 0° and φ = 60°, respectively. The sectors of proposed SVM (A ~ F) are determined from the combination of polarities of the output currents based on Table 1. In the case of unity power factor, it is found that the optimized vector patterns are effective to minimize the rms value of the inverter input current at all times from Table 2. Thus, the optimized vector patterns is applied at all times in the case of unity power factor. In the case of low power factor (cos φ = 0.5), there are areas which cannot be modulated by the optimized vector patterns expressed as shaded area in right hand of Fig. 6(b). Hence, the conventional SVM is applied in these areas and the optimized vector pattern is applied in other areas in the case of the low power factor.

Table 3 shows the selected vectors at each sector in the conventional SVM and optimized vector patterns for the minimum rms value of the inverter input current. Note that the zero vector ($\mathbf{V_0}$ or $\mathbf{V_7}$) is selected with the consideration that the number of switching at each switching period is minimized.

TABLE I. SECTOR DEFINITION OF PROPOSED SVM

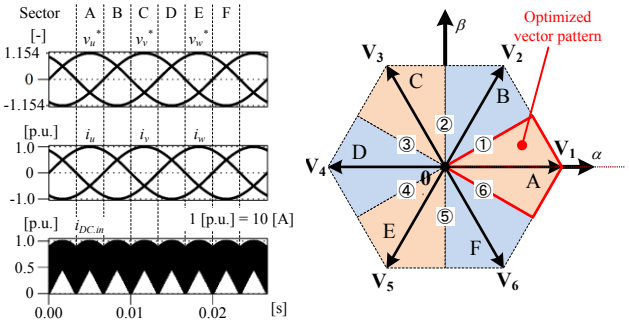
Sector	Current polarity		
	i_u	i_v	i_w
A	P	N	N
B	P	P	N
C	N	P	N
D	N	P	P
E	N	N	P
F	P	N	P

P : Positive,
N : Negative

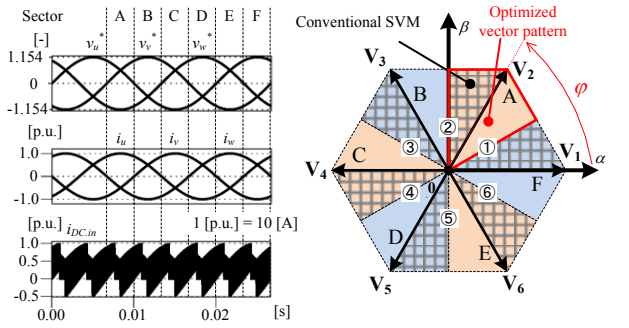
TABLE II. SWITCHING TABLE OF MODULATION METHOD

		Sector of proposed SVM					
		A	B	C	D	E	F
Sector of conventional SVM	①	O	O	C	O	O	C
	②	C	O	O	C	O	O
	③	O	C	O	O	C	O
	④	O	O	C	O	O	C
	⑤	C	O	O	C	O	O
	⑥	O	C	O	O	C	O

O : Optimized vector pattern
C : Conventional SVM



(a) φ = 0° (cosφ = 1.0).



(b) φ = 60° (cosφ = 0.5).

Fig. 6. Waveforms of output voltage references and output currents and input current with proposed SVM (Left hand), space vector map of proposed SVM (Right hand).

III. SIMULATION AND EXPERIMENTAL RESULTS

Table 4 shows the simulation and experimental conditions. In the experiment, a three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.), the rated power of which is 3.7 kW is used as the test motor, whereas the load power factor is varied from 0.258 to 0.866 by controlling the torque reference of the

load motor (GRK2371A, Fuji Electric Co., Ltd.). In this paper, the input current harmonics of three-phase VSI are evaluated as $I_{DC.in(\text{p.u.})}$ expressed as

$$I_{DC.in(\text{p.u.})} = \frac{I_{DC.in(RMS)}}{I_m} = \frac{1}{I_m}\sqrt{\sum_{n=1}^{m}\left(\frac{1}{\sqrt{2}} i_{DC.in,n}\right)^2} \qquad (10)$$

where, $I_{DC.in(\text{RMS})}$ is the RMS value of the input current harmonics, I_m is the maximum value of the output current, n is harmonic order and $i_{DC.in,n}$ is n-order component of the input current harmonics. The fundamental component of the input current harmonics is 75 Hz at rated load. Harmonic components of the input current up to 20-order of the switching frequency (up to m-order component of the input current harmonics) are considered in this calculation.

Fig. 7 shows the simulation results of the analysis of the input current harmonics with the conventional and proposed SVM. When the conventional SVM is applied, the maximum value of $I_{DC.in(\text{p.u.})}$ is 0.450 p.u. at the unity power factor and the modulation index of 0.6. By applying the optimized vector patterns, the maximum value of $I_{DC.in(\text{p.u.})}$ at this point is reduced by 0.313 p.u.. Furthermore, it is confirmed that compared to the conventional SVM, the input current harmonics are reduced in any case of the modulation index and the power factor. Besides, the higher the load power factor is, the greater the reduction effect of the input current harmonics is obtained. This is because the applying ratio of the optimized vector patterns becomes higher as the load power factor becomes higher.

Fig. 8 shows the waveforms of the driving test for the three-phase induction motor with each SVM at the power factor of 0.866, i.e. the load power factor is high, and the modulation index of 0.7. Fig. 8(a) and 8(b) are the waveforms with the conventional SVM and proposed SVM, respectively. When the load power factor is high, the applying ratio of the optimized vector patterns is also high. In particular, the optimized vector patterns are applied at all time at the load power factor of 0.866. It is confirmed from Fig. 8 that the width of the step change in the input current is reduced by applying the optimized vector patterns.

Fig. 9 shows the frequency analysis measurement results of inverter input current with each SVM at the load power factor of 0.866 and the modulation index of 0.7 (under the same conditions as Fig. 8). Fig. 9(a) and 9(b) are the results with the conventional SVM and proposed SVM, respectively. 100% of vertical axis implies the maximum value of output current I_m. When the conventional SVM is applied, the inverter input current includes large switching frequency-order harmonic, the value of which is 31.0%. By applying the optimized vector patterns for the minimum rms value of the inverter input current, the switching frequency-order harmonic is reduced by 6.60%.

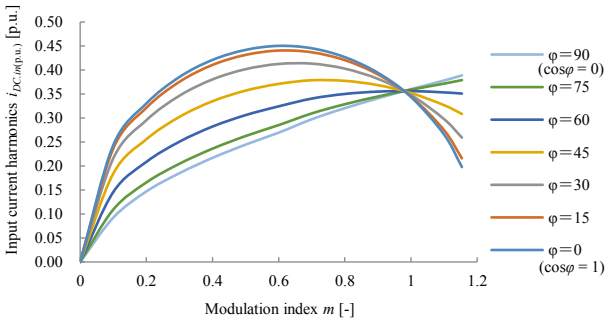
Fig. 10 shows the simulation and experimental results of the analysis of the input current harmonics with the conventional and proposed SVM. At the power factor of 0.866, i.e. when the load power factor is high, the value of $I_{DC.in(\text{p.u.})}$ with the conventional SVM is reduced by 33.9% at most by applying the proposed SVM. Besides, at the power factor of 0.259, i.e. when the load power factor is low, the value of $I_{DC.in(\text{p.u.})}$ with the conventional SVM is reduced by 6.19% at most by applying the proposed SVM. It is confirmed that as the load power factor becomes smaller, the input current harmonics-reduction effect diminishes from this results. Furthermore, the experimental

TABLE III. SELECTED VECTORS AT EACH SECTOR IN CONVENTIONAL SVM AND OPTIMIZED VECTOR PATTERNS FOR MINIMUM RMS VALUE OF INVERTER INPUT CURRENT

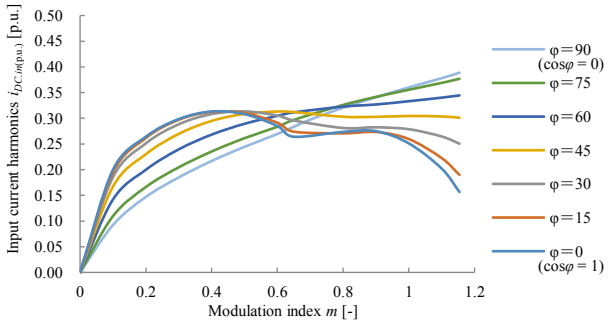
Conventional SVM		Optimized vector patterns		
Sector	Selected vectors	Sector	Selected vectors	
			High mod. index	Low mod. index
①	$\mathbf{V_1}$, $\mathbf{V_2}$, $\mathbf{V_0}$	A	$\mathbf{V_6}$, $\mathbf{V_1}$, $\mathbf{V_2}$	$\mathbf{V_6}$, $\mathbf{V_2}$, $\mathbf{V_7}$
②	$\mathbf{V_2}$, $\mathbf{V_3}$, $\mathbf{V_7}$	B	$\mathbf{V_1}$, $\mathbf{V_2}$, $\mathbf{V_3}$	$\mathbf{V_1}$, $\mathbf{V_3}$, $\mathbf{V_0}$
③	$\mathbf{V_3}$, $\mathbf{V_4}$, $\mathbf{V_0}$	C	$\mathbf{V_2}$, $\mathbf{V_3}$, $\mathbf{V_4}$	$\mathbf{V_2}$, $\mathbf{V_4}$, $\mathbf{V_7}$
④	$\mathbf{V_4}$, $\mathbf{V_5}$, $\mathbf{V_7}$	D	$\mathbf{V_3}$, $\mathbf{V_4}$, $\mathbf{V_5}$	$\mathbf{V_3}$, $\mathbf{V_5}$, $\mathbf{V_0}$
⑤	$\mathbf{V_5}$, $\mathbf{V_6}$, $\mathbf{V_0}$	E	$\mathbf{V_4}$, $\mathbf{V_5}$, $\mathbf{V_6}$	$\mathbf{V_4}$, $\mathbf{V_6}$, $\mathbf{V_7}$
⑥	$\mathbf{V_6}$, $\mathbf{V_1}$, $\mathbf{V_7}$	F	$\mathbf{V_5}$, $\mathbf{V_6}$, $\mathbf{V_1}$	$\mathbf{V_5}$, $\mathbf{V_1}$, $\mathbf{V_0}$

TABLE IV. SIMULATION AND EXPERIMENTAL CONDITIONS

Parameters	Symbol	Simulation	Experiment
DC link voltage	E_{dc}	200 V	200 V
Maximum output current	I_m	10.0 A	5.5 ~ 12.5 A
Switching frequency	f_{sw}	10 kHz	10 kHz
Modulation index	m	0 ~ 1.15	0.256 ~ 1.15
Load power factor	cos φ	0.0 ~ 1.0	0.259 ~ 0.866

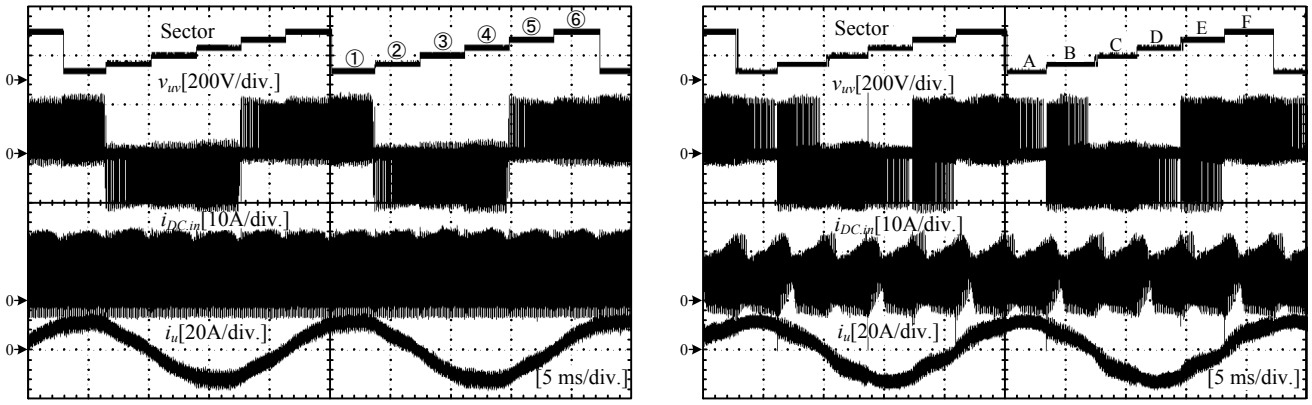


(a) Conventional SVM.



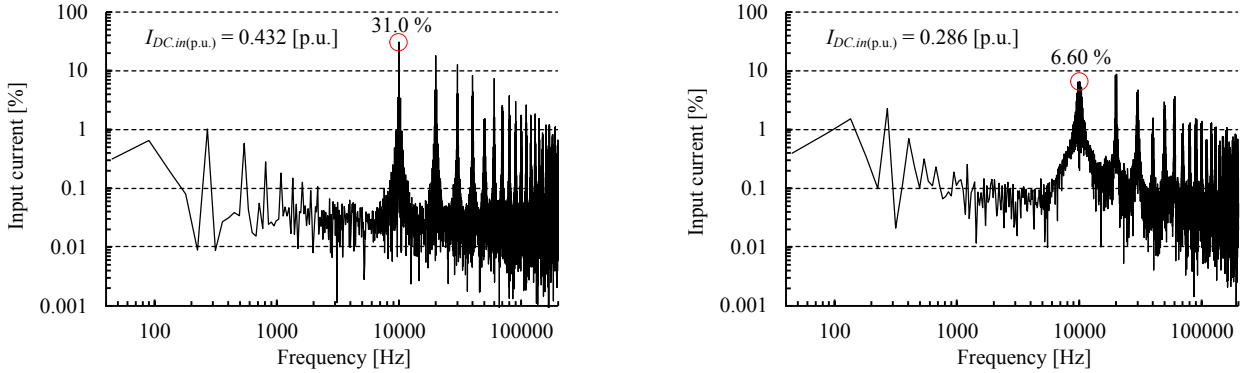
(b) Proposed SVM.

Fig. 7. Simulation results of input current harmonics.



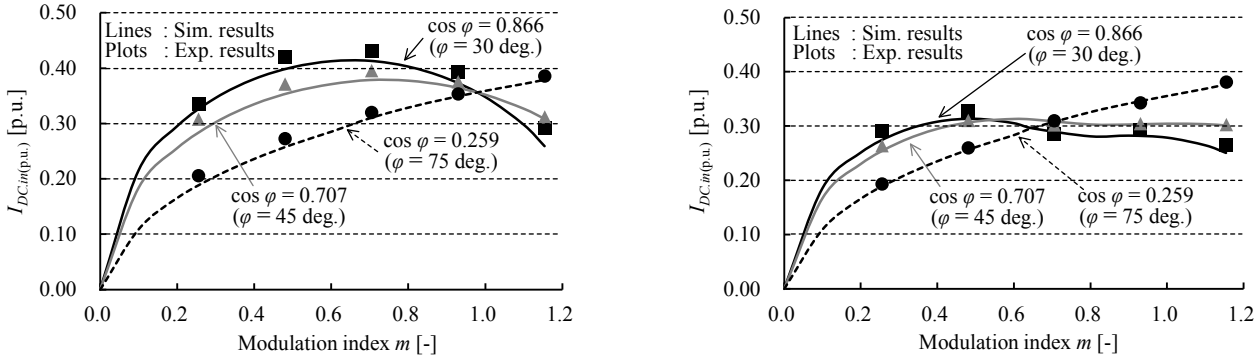
(a) Conventional SVM. (b) Proposed SVM.

Fig. 8. Experimental waveforms at cosφ = 0.866, m = 0.7 : Sector, output line voltage, input current and U-phase output current.



(a) Conventional SVM. (b) Proposed SVM.

Fig. 9. Frequency analysis measurement results of inverter input current at cosφ = 0.866, m = 0.7 (under the same conditions as Fig. 8). Fundamental frequency is 45 Hz.



(a) Conventional SVM. (b) Proposed SVM.

Fig. 10. Simulation and experimental results of input current harmonics.

results of $I_{DC.in(p.u.)}$ almost agree with the simulation results. These results confirm that the proposed SVM can reduce the inverter input current harmonics at any load power factor by both simulation and experiments.

Fig. 11 shows the total harmonic distortion (THD) of the U-phase output line current at the load power factor of 0.866. THD of the output line current is calculated as

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{40}\left(i_n^2\right)}}{i_1} \tag{11}$$

where, i_n is n-order component of the output line current harmonics. In this case, the rated fundamental component of the

output line current harmonics i_1 is 75 Hz. At all modulation index, the THD of the U-phase output line current increases by applying the proposed SVM. In particular, THD of the output line current increases in two times at the maximum by applying the proposed SVM. In the conventional SVM, three fundamental vectors, the tips of which are the closest to the tip of the voltage reference vector, are selected to modulate. Thus, the conventional SVM is the modulation scheme which achieves the minimum output harmonic [14]. In the proposed SVM, the reduction of the input current harmonics is achieved by actively selecting the fundamental vectors which is located far from the voltage reference vector in order to minimize the zero vector period. Furthermore, the line current ripple in the inverter-fed motor drive is caused by the instantaneous error between the applied voltage and reference voltage. In particular, the rms line current ripple can be calculated by using the time integral of the error voltage vector between the applied voltage and reference voltage [15-16]. Consequently, THD of the output current deteriorates when the proposed SVM is applied. However, the increase of the output line current with the proposed SVM can be suppressed by increasing switching frequency, i.e. shortening the integral time of the error voltage vector between the applied voltage and reference voltage. Note that the increase in the switching frequency have no influences on the inverter input current harmonics because the rms value of inverter input curretn is independent from the switching period.

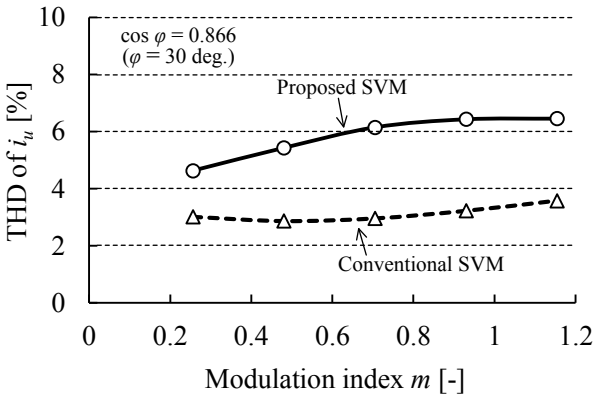


Fig. 11. Total harmonic distortion of output line current with each SVM at power factor of 0.866.

IV. Conclusion

In this paper, the new SVM to reduce the input current harmonics of the three-phase VSI in case that the power factor varies was proposed. This method contributed to the long lifetime of the smoothing capacitor in the motor drive system. The inverter input current harmonics was reduced by optimizing vector patterns in order to minimize the rms value of the inverter input current. In particular, three consecutive active vectors were selected in the case of the high modulation index, whereas two non-adjacent active vectors and one zero vector were selected in the case of the low modulation index. These optimized vector patterns were effective to reduce the rms value of the inverter input current under certain conditions of the output line currents. By determining sectors of the proposed SVM from three-phase output line currents magnitude relations, the input current harmonics are reduced over wide range of the load power factor.

The effectiveness of the proposed SVM was confirmed by both simulations and experiments with the motor. The experimental results confirmed that the input current harmonics was reduced by 33.9% by applying the proposed SVM. Moreover, it was also confirmed that the input current harmonics was reduced over all range of the power factor. On the other hand, THD of output line current deteriorated by applying the proposed SVM. However, the increase of the output line current THD with the proposed SVM can be suppressed by increasing the switching frequency because the increase in the switching frequnecy have no influences on the inverter input current harmonics.

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