Suppression of Short-circuit Current in Halt Sequence to StopTwo-level Inverter connected to PMSM during Regeneration Mode

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***Abstract*— This paper discusses an approach to suppress the rise of the short-circuit current in a halt sequence which is named "Flux-weakening Short-circuit halt sequence (FSHS)". When a back-to-back system with a small capacitor is stopped by grid faults during regeneration, the DC-link capacitor voltage increases rapidly due to regeneration current. FSHS stops the regeneration operation and suppresses the rise of the DC-link capacitor voltage without a dynamic brake circuit. However, FSHS cannot suppress the rise of short-circuit current caused by the q-axis current which rises during the short-circuit mode when the regeneration current is low or PMSM with small synchronous inductance is driven. The improved FSHS suppresses the rise of the short-circuit current in low-load region by maintaining the q-axis current around zero until before the mode is changed to Sequence II at zero-crossing point of the current. In the experiment, it is confirmed that the improved FSHS suppresses to 85% of the short-circuit current when the regeneration current is low.**

Keywords—Permanent magent synchoronous motor, Halt sequence, Short-circuit

I. INTRODUCTION

Recently, power converters are required to reduce the volume and to improve long life time in adjustable drive systems with regeneration mode such as elevator, crane, flywheel energy storage system and so on [1-5]. A back-to-back (BTB) system which consists of a PWM rectifier and an inverter is widely used for this kind of regeneration system. In order to achieve the improvement of long life time, a film capacitor is used as a DC-link capacitor [6]. However, the capacitor with small capacitance causes overvoltage problems of the DC-link part with grid faults. That is, when the BTB system is stopped by the grid faults during regeneration, the DC-link voltage increases rapidly. Consequently, the switching device will be broken when the DC-link capacitor voltage becomes higher than the voltage rating of them. Therefore, it is necessary to suppress the voltage rise of the DC-link capacitor when system accidents occur.

In one of conventional methods to suppress voltage increasing, a brake chopper circuit is connected in parallel to the DC-link capacitor, i.e. a dynamic brake circuit [7]. When the DC-link capacitor voltage exceeds the threshold voltage, the regeneration power is consumed by the resistance in the brake chopper circuit. However, the dynamic brake circuit requires additional switching device and components. Several methods to reduce the volume of the dynamic brake circuit have been reported in Ref. [8]. However, the cost and volume of the dynamic brake circuit is not desirable in the power conversion system, even it is operated only for the halt sequence during the system failures.

The authors have proposed a halt sequence that shorts the terminal of the motor according to the motor current when the grid is cutoff during the regeneration mode in order to avoid the overvoltage of the DC-link capacitor, and also prevents the overcurrent [9-10]. This halt sequence, which is named "Flux-weakening short-circuit halt sequence (FSHS)", can be also applied to the regeneration system such as flywheel energy storage systems. In addition, it is possible to downsize the BTB system because the dynamic brake circuit is not required in the fux-weakening short-circuit halt sequence. However, the flux-weakening short-circuit halt sequence cannot suppress the rise of short-circuit current caused by the q-axis current which rises during the short-circuit mode when the regeneration current is low or PMSM with small synchronous inductance is driven. Therefore, it is necessary to suppress the rise of the short-circuit current caused by the q-axis current.

This paper proposes an improved FSHS to suppress the rise current of the short-circuit in low-load region. In the improved FSHS, the q-axis current is maintained around zero by applying the lagging and leading voltage vector to PMSM depending on the q-axis current from the end of Sequence I to the beginning of Sequence II in order to suppress the rise of the q-axis current which causes the rise of the short-circuit current. This paper is organized as follows; Firstly, the principle of FSHS is discussed. Second, its problem in the low-load region is discussed. Next, the principle of the improved FSHS to solve

its problem is discussed. Next, the operation of short-circuit current suppression sequence is confirmed in simulation. Finally, the effectiveness of the short-circuit current suppression sequence is evaluated in experiments.

II. Flux-weakening Short-circuit Halt Sequence

A. Principle of short-circuit halt sequence

Fig. 1 shows the system configuration of the power conversion system. This system uses a two-level PWM inverter and rectifier in order to control an Interior Permanent Magnet Synchronous Machine (IPMSM). A DC-link capacitor with small capacitance is used to absorb the switching ripples. The regeneration power P from the motor depends on the rotating speed and braking torque as (1).

$$P = \omega T = \omega P_n i_q \left\{ \sqrt{3}\Psi_e + \left(L_d - L_q\right) i_d \right\} \qquad (1)$$

where ω is the rotational speed, T is torque of the PMSM, L_d and L_q are the d-axis and q-axis inductance, Ψ_e is the linkage magnetic flux of armature by permanent magnet, i_d and i_q are the d- and q-axis current, P_n is the number of the pairs of poles. From (1), the negative torque will cause the increase of the DC-link voltage if the q-axis current is not controlled to zero. Thus, in order to prevent the overvoltage at the DC-link voltage, the q-axis current should be zero immediately.

In [9], the flux-weakening short-circuit halt sequence prevents the over voltage at the DC-link capacitor by shorting the terminal of motor when the relay is cutoff. The Flux-weakening short-circuit halt sequence consists of two sequences; in Sequence I, the q-axis current is controlled to become zero by the reactive power without a current regulator while the DC-link voltage is maintained within a certain range by selecting the switching patterns between the charge mode and discharge mode. After the q-axis current becomes zero, Sequence II is implemented in order to conduct the short-circuit mode until the d-axis current becomes zero. In a matter of fact, Sequence II alone can achieve this halt sequence and preventing the DC-link capacitor from overvoltage, since the motor currents are circulating in the inverter during this halt sequence. However, the motor current will be increased drastically in high speed region because of the electromotive force in the motor. As a result of the short circuit condition, the large motor current causes the irreversible flux loss in the magnet of PMSM. In addition, the inverter is required to implement with high current rating switching devices. Therefore, Sequence I is introduced to prevent the occurrence of large current. The motor is typically designed in a matter that the maximum current is allowed up to 2.5 to 3.7 p.u. of the rated current [11-14]. By implementing Sequence I, the maximum current in the flux-weakening short-circuit halt sequence is suppressed to less than three times of the rating current.

Fig. 2 shows the relationship between the voltage command vector and the motor current vector in Sequence I. The instantaneous power p_{out} becomes zero when the motor current vector crosses the inverter voltage vector at the right angles as shown in Fig. 2. However, the instantaneous power p_{out} cannot always become zero because there are only eight space voltage

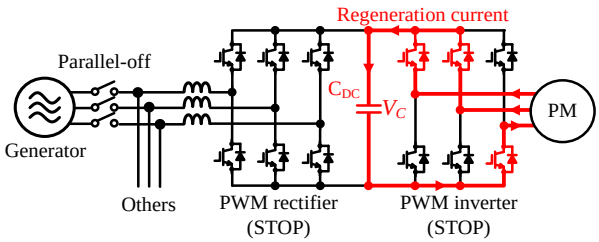


Fig. 1. System configuration of the motor drive system connected to the grid during the motor regeneration.

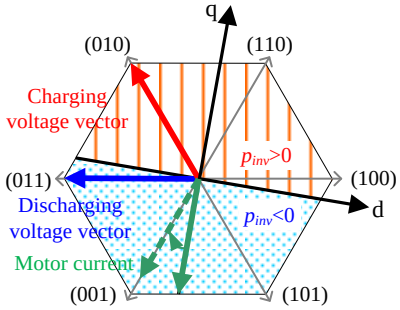


Fig. 2. Relation between space voltage vector and current vector of motor in Phase I. The two-level inverter has the switching patterns to charge and discharge the DC-link capacitor.

Table 1. Switching pattern of Phase I.

	Direction of current			State of switch of inverter					
	i_u	i_v	i_w	S_{pu}	S_{pv}	S_{pw}	S_{nu}	S_{nv}	S_{nw}
Discharge	+	-	-	**ON**	OFF	**ON**	OFF	**ON**	OFF
	+	-	+	OFF	OFF	**ON**	**ON**	**ON**	OFF
	-	-	+	OFF	**ON**	**ON**	**ON**	OFF	OFF
	-	+	+	OFF	**ON**	OFF	**ON**	OFF	**ON**
	-	+	-	**ON**	**ON**	OFF	OFF	OFF	**ON**
	+	+	-	**ON**	OFF	OFF	OFF	**ON**	**ON**
Charge	+	-	-	OFF	OFF	**ON**	**ON**	**ON**	OFF
	+	-	+	OFF	**ON**	**ON**	**ON**	OFF	OFF
	-	-	+	OFF	**ON**	OFF	**ON**	OFF	**ON**
	-	+	+	**ON**	**ON**	OFF	OFF	OFF	**ON**
	-	+	-	**ON**	OFF	OFF	OFF	**ON**	**ON**
	+	+	-	**ON**	OFF	**ON**	OFF	**ON**	OFF

vectors including zero voltage vectors in two-level inverter. The two-level inverter has the switching patterns to charge and discharge the DC-link capacitor. Therefore, in Sequence I, the switching pattern to maintain the DC-link capacitor voltage is selected according the current polarity while the instantaneous power p_{out} is arranged to become zero by charging and discharging the DC-link capacitor. Accordingly, the q-axis current achieves zero at the very short time because the active current is changed into a reactive current. Table 1 illustrated the switching table that is implemented in the inverter that is depending on the capacitor voltage in subjects to the charge and discharge modes. The voltage command vector becomes a lag of 30-90 degrees with respect to the motor current vector during the discharge mode. Similarly, the voltage command vector becomes the lead of 90-150 degrees with respects to the motor current vector during the charge mode. As a result, the voltage command vector becomes the lagging phase of 60-120 degree with respects to the motor current vector. Sequence I operation ends when the q-axis current becomes zero.

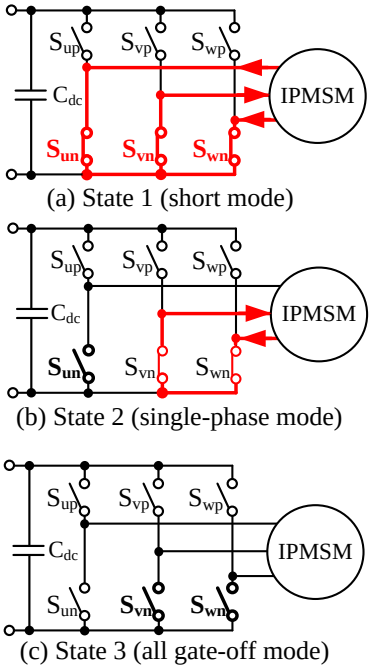


Fig. 3. Operational modes in Phase II. Phase II avoids the regeneration current flowing into DC-link capacitor to prevent its voltage from increase. In addition, Phase II interrupts the three-phase current.

Fig. 3 shows the short circuit operation mode that intends to prevent the DC-link capacitor voltage from rising by circulating the regenerating current inside the inverter. In Sequence II, the switching states create a short condition to prevent the DC-link voltage from increasing. The following shows the switching states of the inverter, first, all of upper or lower side arms of the inverter are short-circuited as shown in Fig. 3(a). This switching state can avoid the motor current flows into the DC-link capacitor because it is a short-circuit condition. Then, when the zero-crossing current is detected, the corresponded switch arm is opened sequentially as shown in Fig. 3(b). Thus, the inverter becomes a condition of a single phase operation. Finally, the remaining two switching arms are opened when the zero-crossing current are detected, respectively as shown in Fig. 3(c). Therefore, the suppression of the circulating current and the rising of the DC-link voltage can be achieved.

Fig. 4 shows the operation flow chart in Sequence I. Once the relay is opened, the current polarity is recorded then the q-axis current signal is comparing in the system to decide the operation between Sequence I and Sequence II. Then, the q-axis current is changed into reactive current by changing the voltage vectors in the inverter.

Fig. 5 shows the experimental waveform of the output current and the DC link capacitor voltage which are obtained by gate interruption. In the experiment, a relay is opened and all switches are turned off by interrupting the gate signal at the same time. The DC link capacitor voltage is increased by approximately 140 V after the relay is opened and all switches are turned off.

Fig. 6 shows the experimental result of the output current and the DC-link capacitor voltage which are obtained by the

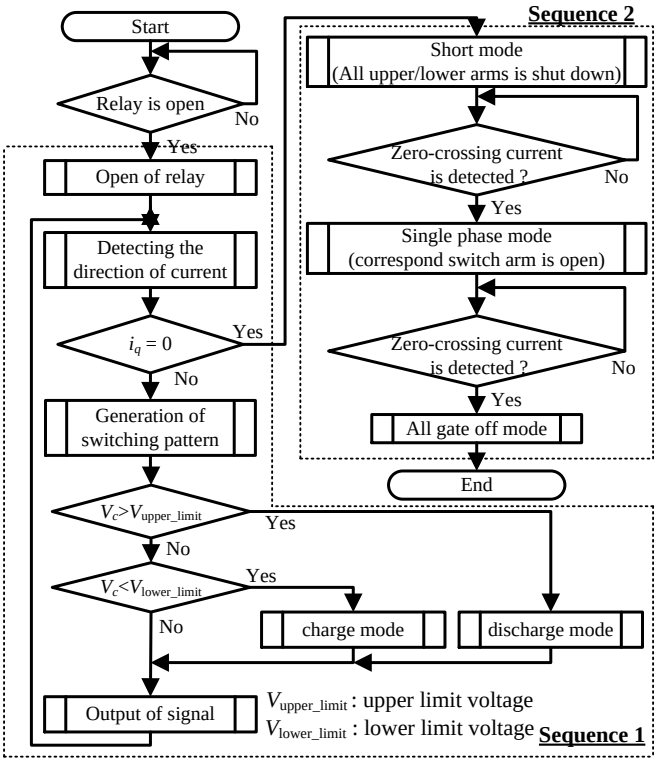


Fig. 4. Operation flow chart of Short-circuit halt sequence.

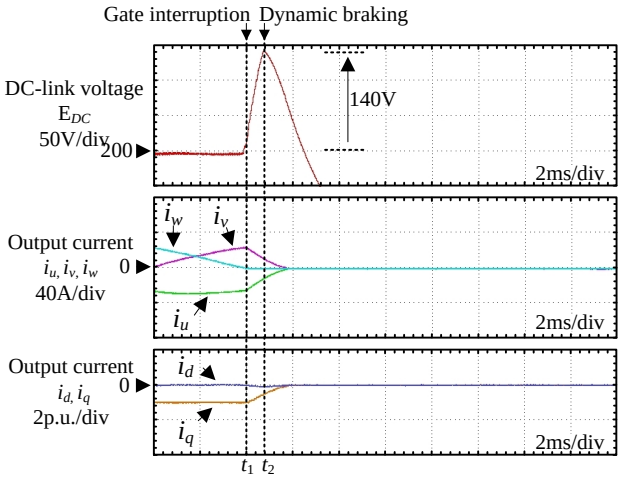


Fig. 11. Experimental results when all gate signals are interrupted as the halt sequence. the DC-link capacitor voltage rises by approximately 140 V after the relay is opened and all switches are turned off.

flux-weakening short-circuit halt sequence. In Fig. 6, once the relay is opened at 4 ms. At approximately 6 ms, the q-axis current reaches zero, then Sequence II begins to be operated. From the result, the output current can be suppressed to less than 2.5 p.u of the rated current by applying the flux-weakening short-circuit halt sequence. In addition, the fluctuation of the DC-link capacitor voltage is suppressed to less than 0.07 p.u. (= 22V) of the rated voltage, which is sufficiently small.

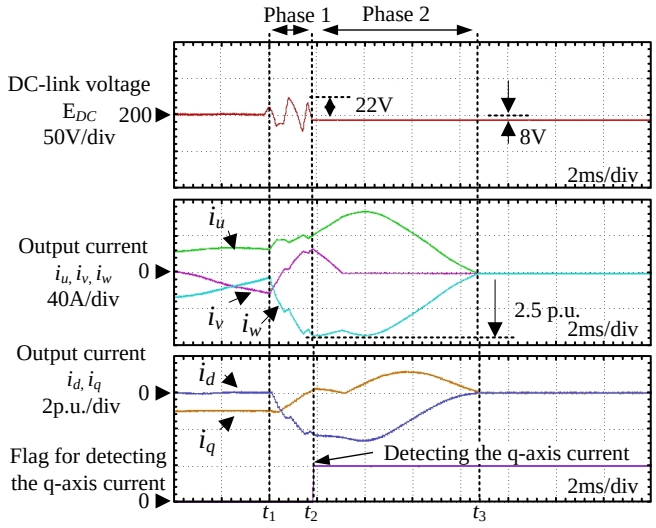


Fig. 6. Experimental result when the system is applied with the flux-weakening short-circuit halt sequence. i_q reaches zero, then Phase II begins to be operated. The output current can be suppressed to less than 2.5 p.u of the rated current.

Table 3. Simulation conditions.

Rated motor power	3 kW
Rated current	16.9 A_{rms}
Rated speed	7200 rpm
Number of poles	12
Winding resistance	0.127 Ω
d-axis inductance	0.389 mH
q-axis inductance	5.56 mH
Back-electromotive force	58 V_{rms}@7200rpm
Rated DC voltage	200 V
Threshold DC over-voltage	330 V

B. Problem of flux-weakening short-circuit halt sequence

Fig. 7 shows the simulation result when the flux-weakening short-circuit halt sequence cuts low regeneration current (0.5 p.u.) off. In Fig. 7, the q-axis current increase drastically during short-circuit mode of Sequence II. The q-axis voltage equation, when the sequence is changed to Sequence 2, is shown in (2).

$$L_q \frac{di_q}{dt} = -\omega_{re} L_d i_d - e \qquad (2)$$

Note that, the voltage drop caused by the resistance is neglected because it is very small. As shown in (2), the q-axis current variation of negative direction is decided by back electromotive force (back-EMF), the cross term of the d-axis current and the d- and q- axis inductance. In Fig. 7, the q-axis current flows in the negative direction during short-circuit mode. When the regeneration current is low in high speed region or PMSM with low inductance is driven, the q-axis current flows drastically in the negative direction during the short-circuit mode of Sequence II in Fig. 7. Accordingly, the short-circuit current which is more than 2.4 times of the regeneration current flows because the d-axis current to cancel the back-EMF is insufficient. In order to prevent the rise of the q-axis current, it is necessary to shorten the period of the short-circuit mode i.e. the period between the start of the short circuit and the first current zero-crossing point.

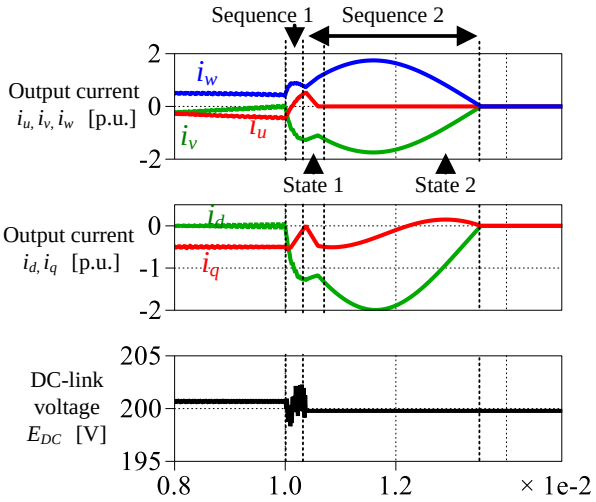
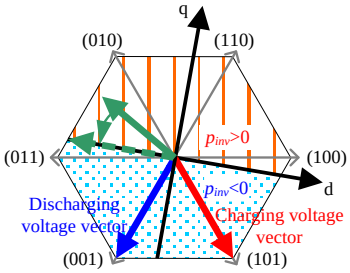
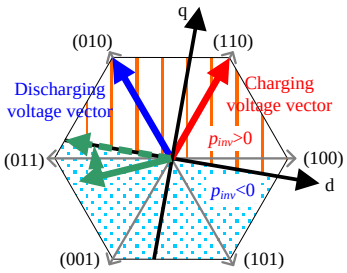


Fig. 7. Simulation result in PMSM which has low inductance. If the high back electromotive force, the cross term of the d-axis current and the d- and q- axis inductance, the q-axis current flows drastically in the negative direction during short-circuit mode.



(a)Lagging voltage mode (i_q<0)



(b)Leading voltage mode (i_q>0)

Fig. 8. Vector diagrams of lagging and leading voltage vector. When the q-axis current is negative, the inverter applies the lagging voltage vector to PMSM. On the other hand, when the q-axis current is positive, the inverter applies the leading voltage vector to PMSM during the short-circuit current suppression sequence

III. IMPROVED SHORT-CIRCUIT HALT SEQUENCE

In the improved the flux-weakening short-circuit halt sequence, the the short-circuit suppression sequence maintains the q-axis current of zero after the q-axis current reaches zero in Sequence I. After that, the sequence is changed to Sequence II at first current zero-crossing point.

Fig. 8 shows the vector diagrams of lagging and leading voltage mode in the short-circuit current suppression sequence.

When the two-level inverter applies the lagging voltage vector to PMSM, the q-axis current is rotated in the anticlockwise direction. When the inverter applies the leading voltage vector to PMSM, the q-axis current is rotated in the clockwise direction. The short-circuit current suppression sequence maintains the q-axis current around zero by applying the lagging and leading voltage vector to PMSM depending on the q-axis current.

Fig. 9 shows the flowchart of the improved short-circuit halt sequence with the short-circuit suppression sequence. The green line in Fig. 8 is the short-circuit current suppression sequence.

Fig. 10 shows the simulation result when the improved FSHS applied with the short-circuit current suppression sequence acts to stop the inverter. After the q-axis current reaches zero in Sequence I, the short-circuit current suppression sequence maintain the q-axis current around zero until just before V-phase current crosses zero because the inverter applies the lagging and leading voltage vector to PMSM depending on the q-axis current direction. From Fig. 10, the q-axis current is maintained around zero by applying the lagging and leading voltage vector depending on the q-axis current direction. After that, the inverter short-circuits PMSM.

IV. Experimental Resluts

Fig. 11 shows the experimental result when FSHS (without the short-circuit current suppression sequence) stops the inverter. In Fig. 6, d-axis current flows in negative direction. When the regeneration current is low in high speed region or PMSM with low inductance is driven, the q-axis current flows drastically in negative direction during short-circuit mode of Sequence II in Fig. 11. As a result, the short-circuit current which is more than 5 times of the regeneration current flows because the d-axis current to cancel the back-EMF is insufficient.

Fig. 12 shows the experimental result when the improved FSHS (with the short-circuit current suppression sequence) stops the inverter. After the q-axis current reaches zero in Sequence I, the short-circuit current suppression sequence maintains the q-axis current around zero until just before W-phase current crosses zero because the inverter applies the lagging and leading voltage vector to PMSM depending on the q-axis current direction. After that, the inverter short-circuits PMSM. The fluctuation of the DC-link capacitor voltage during the charge and discharge by the lagging and leading voltage vector is suppressed within 50V. In Fig. 12, the short-circuit current which is more than four times the regeneration current flows. On the other hand, the short-circuit current is suppressed to 85% of the shirt-circuit current in Fig. 11 because the q-axis current is maintain around zero until just before the W-phase current reaches zero. As a result, it is confirm that the improved FSHS with the suppression sequence stops the regeneration operation and suppress the rise of the DC-link capacitor voltage and the short-circuit current without the dynamic brake system when the regeneration current is low.

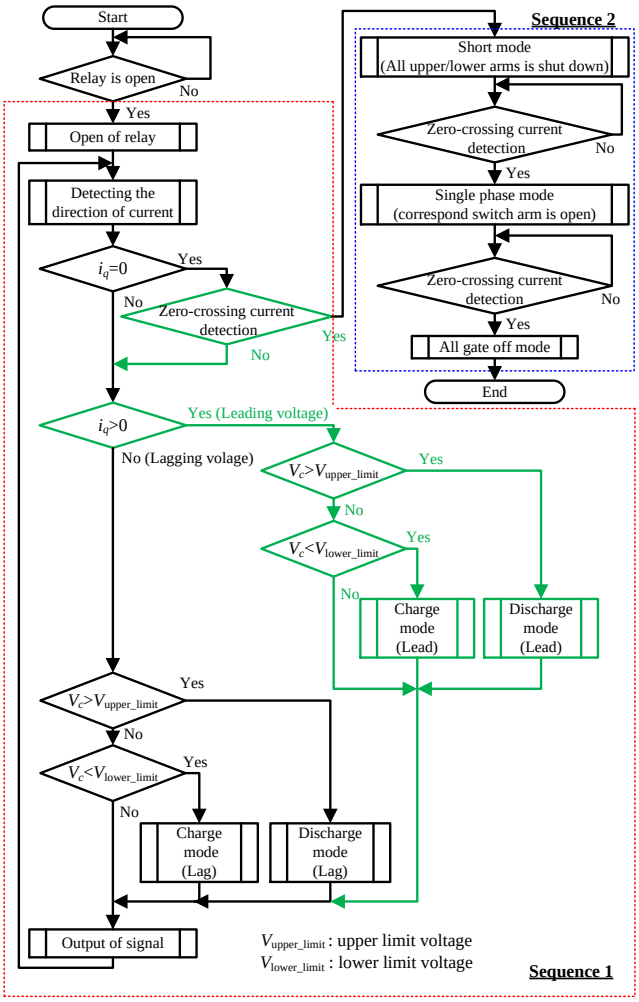


Fig. 9. Flowchart of the improved halt sequence with the short-circuit suppression sequence.

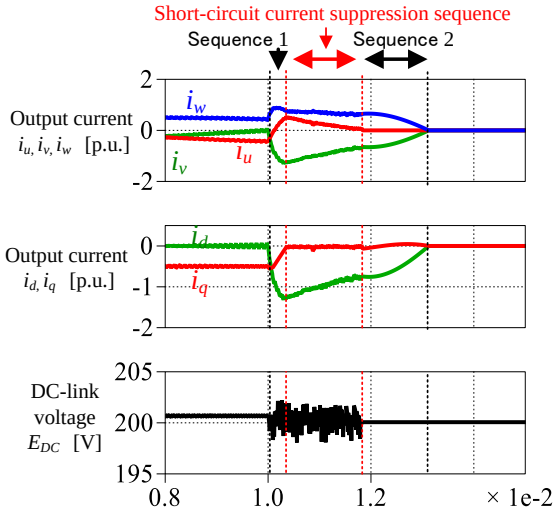


Fig. 10. Simulation result when the short-circuit halt sequence with the suppression sequence is applied in PMSM which has low inductance.

V. Conclusion

This paper proposed the improved FSHS to suppress the rise current of the short-circuit in low-load region. The improved FSHS stops the regeneration operation and suppresses the rise of the DC-link capacitor voltage without the dynamic brake circuit as well as FSHS. Moreover, the improved FSHS suppresses the rise current of the short-circuit in low-load region by maintaining the q-axis current around zero with the leading and lagging voltage vector until before the mode is changed to Sequence II at zero-crossing point of the motor current. In the experiment, it is confirmed that the improved FSHS with the suppression sequence suppresses to 85% of the short-circuit current when the regeneration current is low. In addition, the voltage rise in the DC-link capacitor is maintained within 50V.

In future work, the improved FSHS will be constructed on the hardware in terms of the reliability.

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Table 4. Experimental conditions.

Rated motor power	5.5 kW
Rated motor voltage	200 V_{rms}
Rated current	20 A_{rms}
Rated speed	1500 rpm
Number of poles	6 poles
Winding resistance	0.215 Ω
d-axis inductance	4.3 mH
q-axis inductance	10.2 mH
Back-electromotive force	164 V_{rms}@1500rpm
Rated DC voltage	200 V
Threshold DC over-voltage	330 V

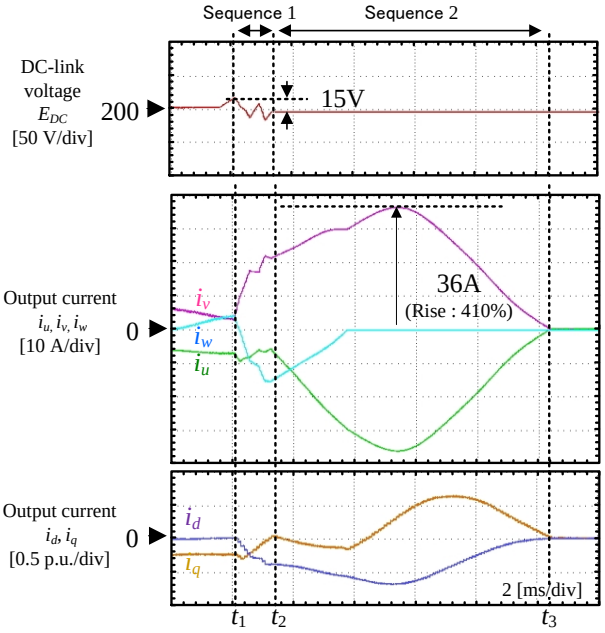

Fig. 11. Experimental result with the short-circuit halt sequence without the flux-weakening short-circuit current suppression sequence.

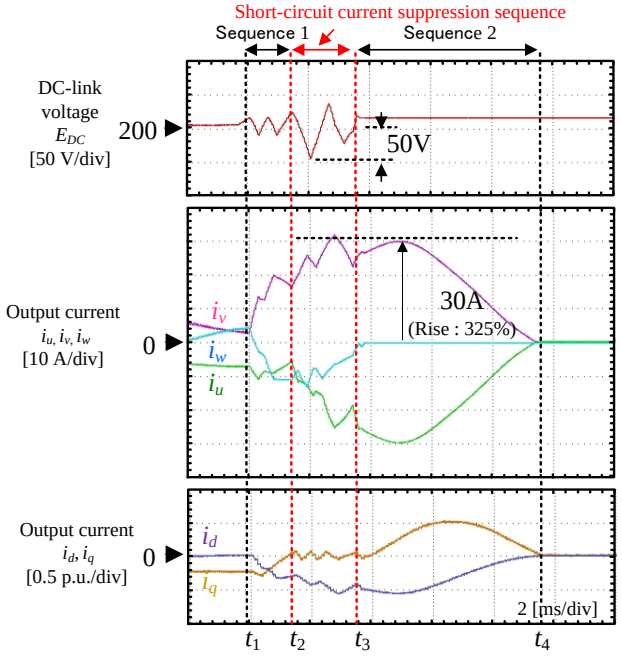

Fig. 12. Experimental result with the improved short-circuit halt sequence with the short-circuit current suppression sequence.