FRT Capability of Single-phase Grid-connected Inverter with Minimized Interconnected Inductor

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Abstract— This paper proposes a fault-ride-through (FRT) method for a single-phase grid-connected inverter with a minimized inductor by reducing the inverter output current overshoot. When a low-inductance interconnected inductor is used, the inverter output current overshoot becomes very high at a voltage sag and a voltage recovery. Therefore, a grid-voltage fault stops the operation of the grid-connected inverter due to an overcurrent protection. In the proposed method, the current overshoot is suppressed by using a momentary gate-block with a high-performance disturbance observer. Moreover, the inverter output current in steady state is also stabilized by using the high-performance disturbance observer. Consequently, by using the proposed method, the grid-connected inverter continues to operate without interruption during the fault of the grid voltage. The maximum overshoot rate of the inductor current at the voltage recovery moment after fault clearance is reduced from 534% in the conventional method to 46.5% in the proposed method.

Keywords—Grid-connected inverter; Fault ride through; Gate-block; Disturbance observer; Interconnected inductor.

I. INTRODUCTION

In recent years, photovoltaics systems (PV) have been actively studied for low carbon emission [1]-[2]. In order to supply the power to single-phase grid, a power conversion system (PCS) is used. PCSs have been required to reduce the cost and size. In particular, a minimization of the interconnected inductor in the PCS is necessary in order to increase the power density of the PCS [3]-[5]. This inductor can be minimized by reducing the inductance with high switching frequency. However, the inductance reduction of the inductor leads to the decrease in the disturbance suppression performance [6]. Moreover, the PCS is required to continue the operation during a voltage sag without disconnecting from the grid [7]-[12] in order to meet the fault ride through (FRT) requirements. When the inductance is reduced, the inverter output current overshoot becomes very high at a voltage sag and a voltage recovery. In order to meet the FRT requirements, the output current overshoot rate has to be less than 50% of the rated current. Therefore, it is not that simple to minimize the inductor by only increasing the switching frequency.

In a conventional FRT method, a reactive current is flown by the grid-connected inverter during the voltage sag in order to avoid the interruption of the inverter operation. In general, the interconnected inductor is usually designed in such a way that the impedance of the inductor is about %Z = 5% of the base impedance of the system. In this case, the grid-connected inverter can simply achieve FRT requirements because the inductor impedance is large, i.e. small current overshoots at grid fault. When the inductor is minimized, high current overshoots occur at the voltage sag and the voltage recovery. Furthermore, the conventional method is controlled by a low speed controller, e.g. Digital Signal Processor (DSP). Thus, it is difficult to suppress the inverter output current overshoot by the low speed control of DSP. As a conclusion, when the grid-connected inverter with the low inductance of the inductor is applied with the conventional FRT method, it is difficult to satisfy the FRT requirements due to the high inverter-output-current overshoot.

If the conventional FRT method employs a high-performance disturbance observer, it is observed that the disturbance observer can compensate for the disturbances caused by the voltage sag and the voltage recovery. Thus, the inverter output current overshoot can be suppressed by the high-performance disturbance observer. However, this method needs a high speed sampling and high speed PWM (Pulse Width Modulation) control, because the voltage sag and the voltage recovery are the disturbances which vary in very high speed. Therefore, the high-performance disturbance observer is still difficult to meet the FRT requirements

This paper proposes the FRT method that employs the high-performance disturbance observer realized on a field-programmable gate array (FPGA) and a momentary gate-block. The proposed FRT method has a current threshold to detect the voltage sag or the voltage interruption. When the inverter output current exceeds the current threshold, the inverter output current overshoot is suppressed by the momentary gate-block. The proposed method is confirmed by a 1-kW prototype with %Z of 1%. Furthermore, a zero voltage ride through (ZVRT) of the single-phase grid-connected inverter, i.e. the most stringent standards of the FRT requirements, is verified with the proposed FRT method. Moreover, the suppression of the inverter output current overshoot is confirmed at both the voltage interruption and the voltage recovery during the grid fault.

II. FAULT-RIDE-THROUGH CONTROL METHOD

Fig. 1 shows a circuit configuration of a single-phase grid-connected inverter. In this paper, a single-phase two-level inverter is employed due to its simplicity. By reducing the inductance L in order to minimize the inductor, the overshoot of the inverter output current i_{out} becomes very high at the voltage sag. The high current overshoot stops the grid-connected inverter due to an overcurrent protection. Therefore, the grid-connected inverter with a minimized inductor cannot achieve the FRT requirements.

Fig. 2 shows a reactive current control block for the FRT operation. The phase θ is locked by phase locked loop (PLL) based on the grid voltage detection value v_{ac}. During the voltage sag, the detection signal v_{frt} becomes high level, and the current phase θ' is the sum of the grid voltage phase θ and $\pi/2$. The reactive current control is realized by generating a current command value with the current phase θ'.

Fig. 3 shows the control block diagram of the conventional FRT operation where V_{dc} is the input DC voltage, T_d is the dead-time period, i_{Ldet} is the inductor current detection value and f_{sw} is the switching frequency, and $e^{-sT_{delay}}$ is the delay time of the current detection and the A/D conversion. The current controller is implemented by digital signal processor (DSP). Moreover, a dead-time error voltage of the inverter output is compensated by calculating the dead-time error voltage compensation at a steady state operation. When the inductance is low, it is difficult to compensate the grid disturbance by increasing the disturbance gain. Therefore, the inverter output current overshoot becomes high at the voltage sag due to the use of the conventional FRT control method.

Fig. 4 shows the control block diagram of the FRT operation with a disturbance observer, which has been proposed in [13]-[18]. It is possible to compensate a disturbance by the high-performance disturbance observer, which is implemented on the FPGA. The disturbance compensate voltage is estimated from the output current and the voltage command,

$$\hat{v}_{dis} = \frac{\omega_c}{\omega_c + s}\left(v_{conv}^* + \omega_c L i_{Ldet}\right) - \omega_c L i_{Ldet} \qquad (1)$$

where, ω_c is the cutoff angular frequency of the disturbance observer and v_{conv}^* is the output voltage command. The current controller is implemented by DSP. On the other hand, the disturbance observer is implemented by the FPGA. At the steady state operation, it is confirmed that the disturbance observer compensates the output voltage error such as the dead-time error voltage and the voltage drop on the switching devices [19]. However, the amount of the inductor current variation is large at the voltage drop and the voltage recovery. Therefore, even if the high-performance disturbance observer is implemented in the inverter, the inverter output current overshoot may still become very high at grid faults.

Fig. 5 shows the control block diagram of the disturbance observer with the momentary gate-block for the FRT operation. The proposed control method is employed by the FPGA. The
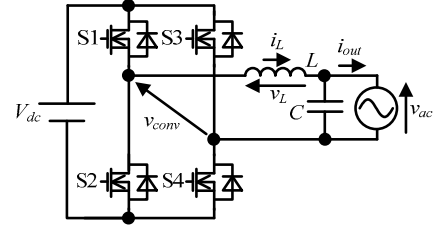

Fig. 1. Single-phase inverter circuit with LC filter. The inductance L is reduced by increasing the switching frequency.
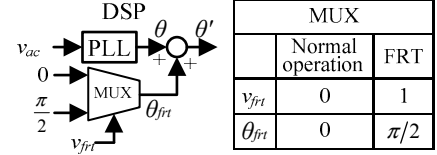

Fig. 2. Reactive current control method for FRT operation. When voltage sag occurs, the phase θ' becomes leading by $\pi/2$ from θ.

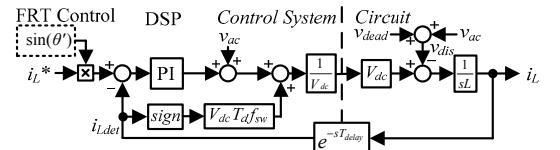| MUX		
	Normal operation	FRT
v_{frt}	0	1
θ_{frt}	0	$\pi/2$

Fig. 3. Control block diagram of conventional FRT operation. In the conventional method, the current controller is implemented by DSP.
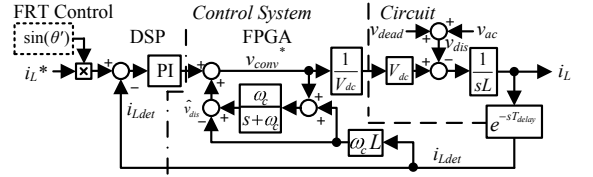

Fig. 4. Control block diagram of FRT operation with disturbance observer. The high-performance disturbance observer is still difficult to compensate large disturbances such as voltage sag.

momentary gate-block signal OC_L and the voltage sag determination signal FRT_ST are determined by

$$OC\_L = \begin{cases} 0 & \left(|i_{Ldet}| \geq I_{ref\_OC}\right) \\ 1 & \left(|i_{Ldet}| < I_{ref\_OC}\right) \end{cases} \qquad (2),$$

$$FRT\_ST = \begin{cases} 0 & \left(|v_{r\_th}| \leq |v_{rdet}|\right) \\ 1 & \left(|v_{r\_th}| > |v_{rdet}|\right) \end{cases} \qquad (3),$$

where I_{ref_OC} is the gate-block threshold of the inverter output current overshoot, v_{r_th} is the grid voltage lower threshold, v_{rdet} is the detected value of the grid voltage. When OC_L is zero, the momentary gate block is active. The gate-block period is the same as one period of the carrier. The integrator of the disturbance observer is initialized at the gate-block period after the voltage drop. After that, the gate-block is released in order to continue to operate the inverter. Note that the current over-
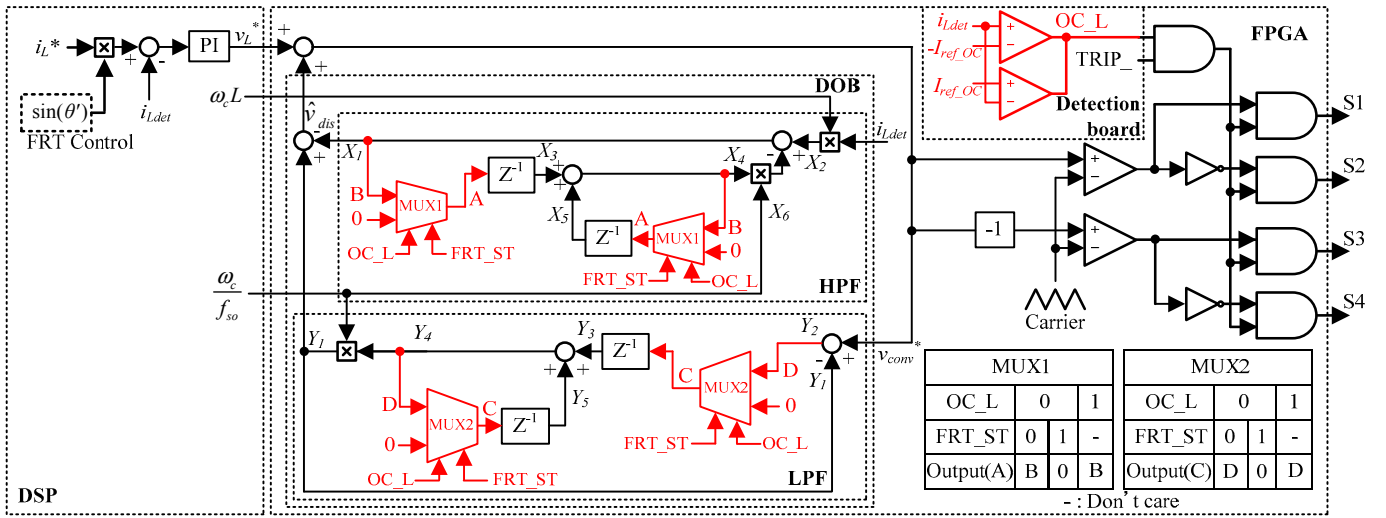
Fig. 5. Control block diagram of ZVRT operation by using high-performance disturbance observer with momentary gate-block.
By using the gate-block, the inverter output current overshoot is suppressed at the voltage drop and the voltage recovery.
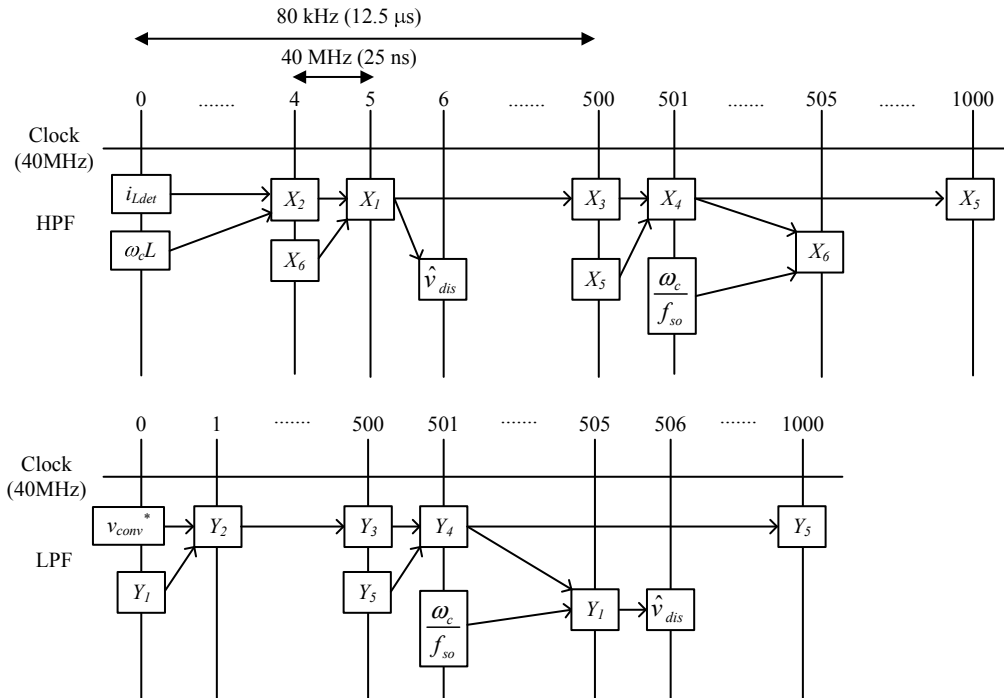

Fig. 6. Timing chart of FPGA controller for high-performance disturbance observer.
X_3, X_5, Y_3 and Y_5 are changed by table of MUX1 and MUX2 in fig. 5.

shoot rate should be less than 50% of the rated current in order to meet the FRT requirements.

Fig. 6 shows the timing chart of the HPF and the LPF in FPGA for implementing the high-performance disturbance observer. In the HPF, the multiplying result of X_2 is outputted with the delay of approximately 100 ns from the detected current of the interconnected inductor i_{Ldet}. The subtracting result X_1 is outputted after one clock. Note that one clock equals to 25 ns. X_3 is one-sampling-period-delayed value of X_1 or zero. X_3 value is selected from the table of MUX1 in Fig. 5. The adding result X_4 is outputted after one clock. X_5 is one-sampling-period-delayed value of X_4 or zero. X_5 value is also selected

from the table of MUX1 from Fig. 5. The multiplying result X_6 is outputted with the delay of approximately 100 ns from X_4. On the other hand, in the LPF, the subtracting result Y_2 is outputted after one clock. Y_3 is outputted as one-sampling-period-delayed value Y_2 or zero. Y_3 value is judged from the table of MUX2 in Fig. 5. The adding result Y_4 is output after one clock. Y_5 is outputted as one-sampling-period-delayed value of Y_4 or zero. Y_5 value is also judged from the table of MUX2 from fig. 5. The multiplying result Y_1 is outputted with a delay of approximately 100 ns from Y_4. Finally, the subtracting result $\hat{v}_{dis}$ is outputted after one clock. By the above timing, the disturbance observer is operated at high speed in FPGA.

III. CALCULATION OF ALLOWABLE DELAY TIME FOR GATE-BLOCK

Fig. 7(a) shows a circuit model for the interconnected inductor with the inverter output and the grid voltage. Focusing on the transient response at the grid voltage recovery, the relationship between the time t and the inductor current i_L is expressed by

$$v_{conv} = L\frac{di_L}{dt} + v_{ac} \qquad (4).$$

Considering to divide the circuit model into two states; a normal operation and an operation of transient response. The normal operation is shown by fig. 7 (b) and the operation of transient response is shown by fig. 7 (c). Note that i_{L_1} is the inductor current at the normal operation generated by an inverter output, i_{L_2} is the inductor current at the transient phenomenon generated by the voltage recovery. Then, i_{L_1} and i_{L_2} are shown by

$$i_{L\_1} = -I_L \qquad (5),$$

$$i_{L\_2} = -\frac{V_{ac}}{L}t \qquad (6),$$

where I_L is the peak of the inductor current, V_{ac} is the peak of the grid voltage. The inductor current i_L is shown by (7) that is expressed by adding (5) to (6).

$$i_L = -I_L - \frac{V_{ac}}{L}t \qquad (7)$$

Moreover, the allowable delay time of the gate-block t_{bd} is expressed by (8).

$$t_{bd} = t_{th} - t_b = \frac{L}{V_{ac}}(-I_L - i_{L\_th}) - (-I_L - i_{L\_b})$$
$$= \frac{L}{V_{ac}}(i_{L\_b} - i_{L\_th}) \qquad (8)$$

where, t_b is the period from the occurrence of the voltage recovery to when the inductor current reaches a gate-block threshold, t_{th} is the period from the occurrence of the voltage recovery to when the inductor current overshoot rate reaches the FRT requirements, i.e. 50% of the rated current, i_{L_b} is the gate-block threshold of the inductor current, i_{L_th} is 50% of the inductor current overshoot.

IV. DESIGN METHOD FOR MINIMIZATION OF INTERCONNECTED INDUCTOR

Fig. 8 shows the flowchart for the minimization of the interconnected inductor in LC filter. At first, the initial conditions which are the grid-voltage v_{ac}, the output power P_{out}, the
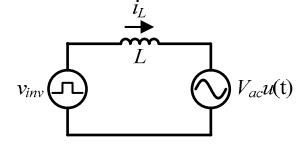
(a) Interconnected inductor with inverter output and grid voltage.
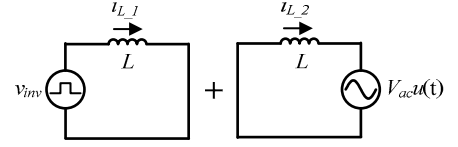
(b) Only inverter output. (c)Only grid voltage.
Fig. 7. Circuit model for interconnected inductor after recovery voltage. In the circuit model, the inverter output current is calculated.
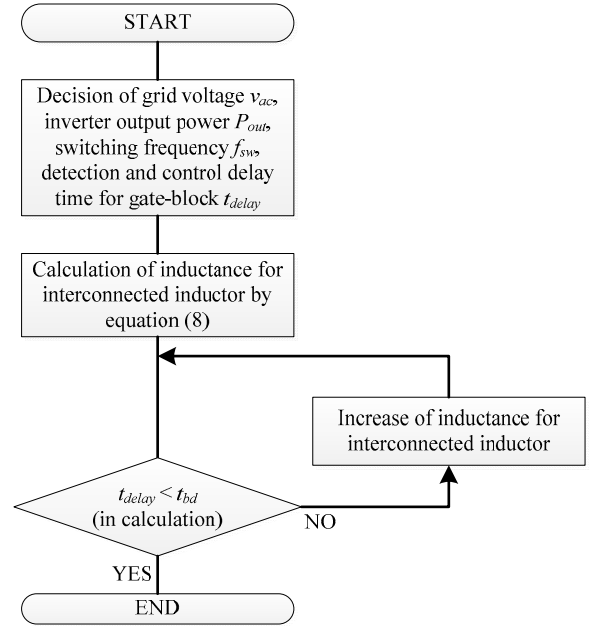

Fig. 8. Flowchart of design method for interconnected inductor. Inductance of interconnected inductor is decided by initial condition, after that, it is confirmed that allowable delay time of gate-block t_{bd} is more than total delay time t_{delay}.

switching frequency f_{sw}, the total delay time of the inductor current detection and the control for the gate-block t_{delay} are decided from the specifications of the grid-connected inverter. By using the initial conditions, the inductance of the interconnected inductor L is calculated by (8). Moreover, the total delay time t_{delay} must be shorter than the allowable delay time of gate-block t_{bd} calculated by (8) in order that it is possible to carry out the gate-block before the inductor current overshoot rate reaches the FRT requirements during the voltage recovery, i.e. t_{th}. Consequently, the FRT operation meets the FRT requirements by suppressing the inductor current overshoot. When t_{delay} is longer than t_{bd}, it is necessary to increase the inductance L to increase t_{bd} more than t_{delay}. Besides, the capacitance of the filter capacitor in LC filter is decided by the cut-off frequency depending on the switching frequency.

Table 1. Calculation result.

Initial condition	
Grid voltage peak V_{ac}	282.8 V
Output power P_{out}	1 kW
Rated inverter output current I_L	7.07 A
Interconnected inductor L (%Z for output impedance)	1.27 mH (1.0%)
Inverter output current threshold for gate-block i_{L_b}	9.0 A
Inverter output current limit by FRT requirement i_{L_th}	$I_L \times 1.5$
Calculation result	
Allowable delay time of gate-block t_{bd}	7.2 μs

(a) Waveform of ZVRT operation.

Voltage drop operation.

(c) Voltage recovery operation.
Fig. 9. Simulation result proposed FRT method during short grid failure. Inverter applied high-performance disturbance observer is also stopped due to the over current protection.

Table 1 shows the calculation result for the allowable delay time of the gate-block t_{bd}. As the initial conditions, the grid voltage peak V_{ac} is 282.8 V, the rated inverter output current peak I_L is 7.07 A, the inductance of the interconnected inductor L is 1.27 mH (%Z = 1.0%), the inverter output current threshold for the gate-block i_{L_b} is 9.0 A, the inverter output current limit by FRT requirements i_{L_th} is 10.6 A (1.5 times of I_L). By using the initial conditions, the allowable delay time t_{bd} is calculated from (8), which results in 7.2 μs. In order to achieve the FRT requirements, it is necessary to achieve that the total delay time of the inductor current detection and the control of gate-block is less than 7.2 μs. However, the inverter circuit has the delay time of the current detection and the sampling. It is difficult to reduce the total delay time less than 7.2 μs. Thus, the momentary gate-block signal OC_L is generated by the analog detection in the detection board in order to reduce the delay time less than 7.2 μs. The fast detection by the analog detection and the disturbance observer implemented on the FPGA together help to meet the FRT requirements.

Fig. 9 shows the simulation result of the proposed FRT method during short grid failure. In the simulation, the total delay time t_{delay} is 7.2 μs, whereas the others parameter are same as the initial conditions of Table 1. Fig. 9 (b) shows the simulation result at the voltage drop operation. In this result, the inductor current overshoot rate exceeds 50%. However, the FRT requirements does not restrict the current overshoot at the voltage drop. Fig. 9(c) shows the simulation result at the voltage recovery operation. In this simulation, the inductor current overshoot rate is suppressed to be less than 50%. Moreover, the error rate of the calculation result and the simulation result is 0.09%. Therefore, it is confirmed that (8) is valid equation.
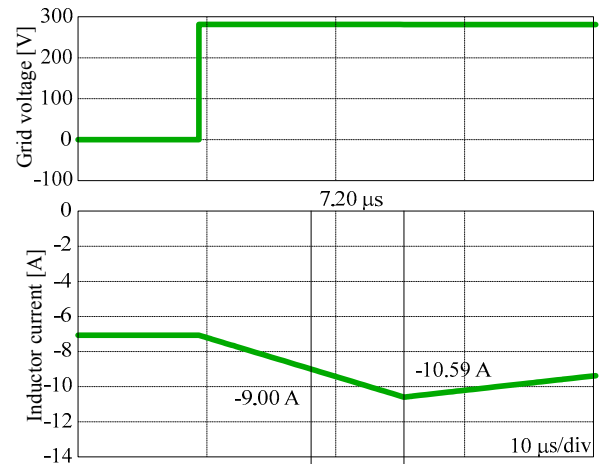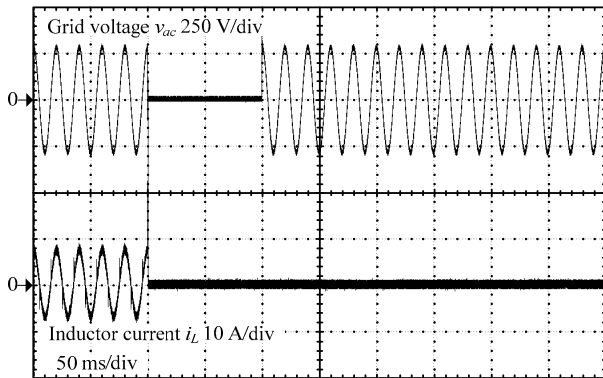
V. EXPERIMENTAL RESULTS

Table 2 shows the experimental conditions. In this paper, a 1-kW prototype is verified. The inductance of the interconnected inductor L is 1.27 mH (%Z = 1.0%), the carrier frequency f_{cry} is 80 kHz, the gate-block threshold for suppressing the inductor current overshoot OC_L is 9.0 A, and the over current protection threshold OC is 20 A. When the inductor current reaches to the OC value, the gate-block is active until reset manually.
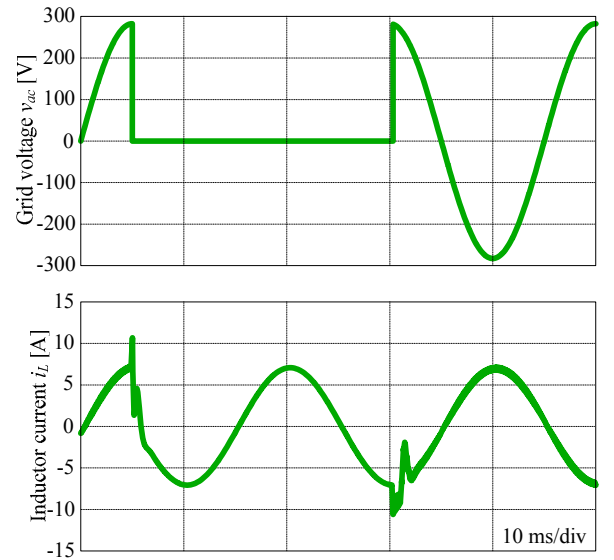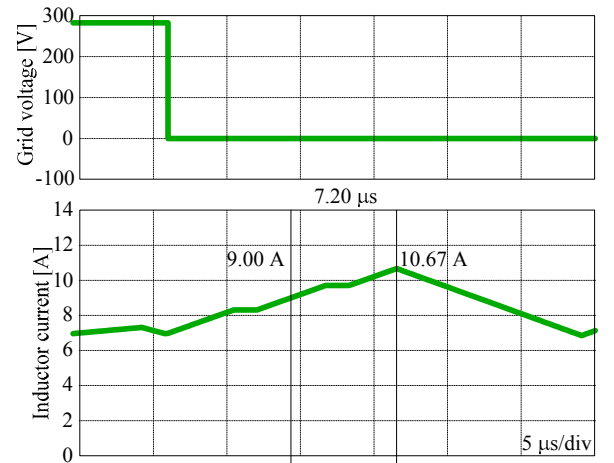
Fig. 10 shows the experimental result of the conventional FRT operation during short grid failure. It is observed from Fig. 10 (b) that, the inductor current i_L exceeds the over current threshold value of 20 A, and after that, the inverter output is stopped by the over current protection. The overshoot rate of the inductor current is 534%. The conventional FRT control method is difficult to suppress the output current overshoot. This problem is caused by the total delay time of the current control employed by DSP and the current detection. When the total delay time is longer than the time that the current overshoot rate reaches the FRT requirements, i.e. 50% of the rated current, it is impossible to suppress the inductor current overshoot under 50%.
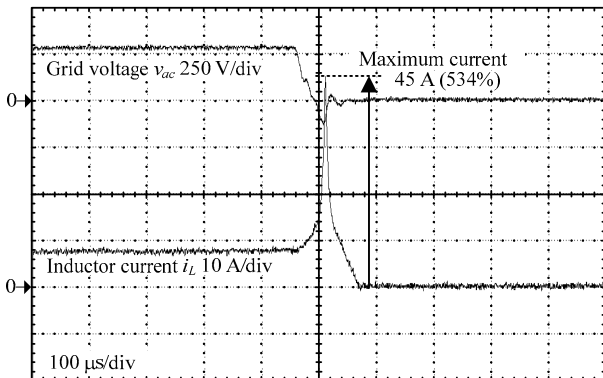
Fig. 11 shows the experimental result of the high-performance disturbance observer during short grid failure. In Fig. 11 (b), the inductor current i_L also exceeds the over current

threshold value of 20 A even with the high-performance disturbance observer. After that, the inverter output is stopped by the over current protection. The overshoot rate of the inductor current is 486%. Because the control speed of the high-performance disturbance observer is not fast enough, the inverter output current overshoot reaches the over current protection threshold before the high-performance disturbance observer compensates for the inverter output current overshoot. If the inductor current overshoot current is suppressed by only the high-performance disturbance observer, the high speed sampling for the current detection, the high speed control (e.g. MHz level) of the disturbance observer and PWM are needed. Therefore, it is difficult to realize the ZVRT by using only the high-performance disturbance observer.

Fig. 12 shows the experimental result of the proposed FRT operation method during short grid failure. The proposed method can realize the ZVRT operation without disconnecting from the grid. Fig. 12 (b) and (c) show the inductor current waveforms at the voltage drop and the voltage recovery. The maximum inductor current are 9.3 A and 10.4 A. These values are suppressed under the over current threshold of 20 A. Moreover, at the voltage drop, the overshoot from a rated inductor current peak of 7.1 A is 2.2 A, i.e. the overshoot rate of 31.0%. At the voltage recovery, the overshoot from an inductor current peak of 7.1 A is 3.3 A, i.e. the overshoot rate of 46.5%. Thus, the grid-connected inverter with the minimized inductor is possible to operate during the voltage sag without the disconnection from the grid and to suppress the current overshoot rate

Table 2. Experimental conditions.

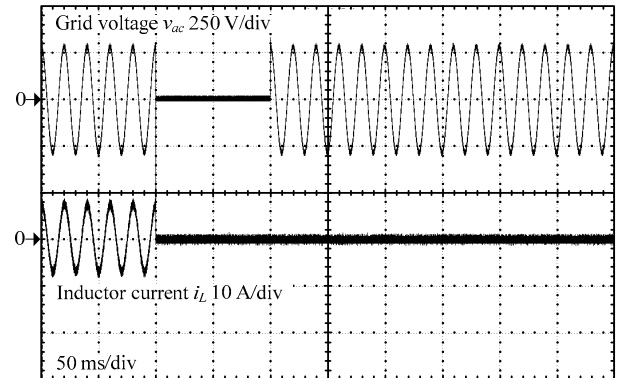| Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	80 kHz
DC link vol.	V_{dc}	380 V	Ang. fre. of ACR	ω_n	6000 rad/s
Grid voltage	v_{ac}	200 V$_{rms}$	Samp. fre. of ACR	f_{samp}	20 kHz
Dead-time	T_d	500 ns	Samp. fre. of DOB	f_{so}	80 kHz
Inter. Induc. (%Z)	L	1.27 mH (1.0%)	Cutoff fre. of DOB	f_c	2 kHz
			delay time of GB	t_{delay}	< 6.5 µs
OC level	OC	20 A	OC_L level	I_{ref_OC}	9 A

(a) Waveform of ZVRT operation.
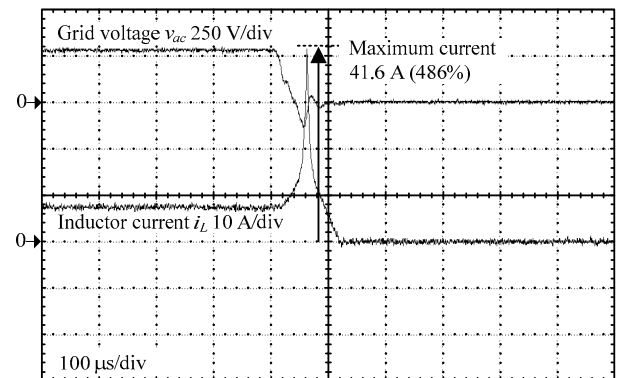

(b) Voltage drop operation.
Fig. 10. Experimental result of conventional FRT operation during short grid failure. The grid-connected inverter is stopped due to the over current protection.

(a) Waveform of ZVRT operation.

(b) Voltage drop operation.
Fig. 11. Experimental result of high-performance disturbance observer during short grid failure. Inverter with high-performance disturbance observer is also stopped due to the over current protection.

less than 50% of rated inverter output current. Fig. 12 (d) shows the stability period of the inverter output after the voltage recovery. The period from the grid voltage recovery to the stability of the inverter output is 175.4 ms. This period depends on the response time of PLL. Moreover, the E. ON code requires that the grid-connected inverter outputs more than 90% before a voltage sag of less than 1.0 sec. Therefore, Fig. 12 (d) satisfies the E. ON code.

VI. CONCLUSION AND FUTURE WORK

This paper proposed the FRT control method by using the momentary gate-block with the high-performance disturbance observer. By using the proposed method, it was confirmed that the single-phase inverter with the minimized inductor of $\%Z = 1\%$ achieved the ZVRT operation without stopping the grid-connected inverter output. Moreover, the inductor current overshoot was suppressed less than 50% of rated inverter output current. Thus, it was confirmed that the inductance of the interconnected inductor was reduced by 1% of $\%Z$ and still satisfied the FRT requirements. Therefore, it was possible to minimize the interconnected inductor by reducing the inductance.

Future work is the further minimization of the interconnected inductor with the application of a *LCL* filter.

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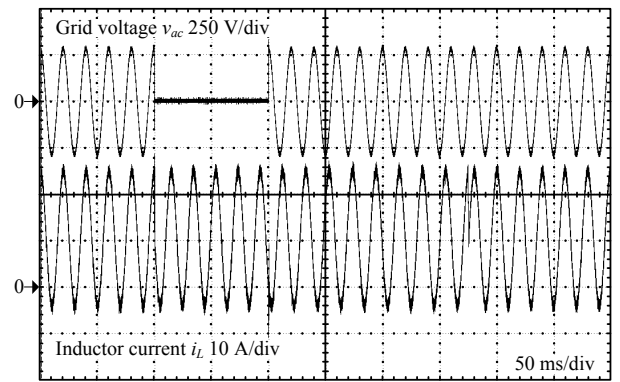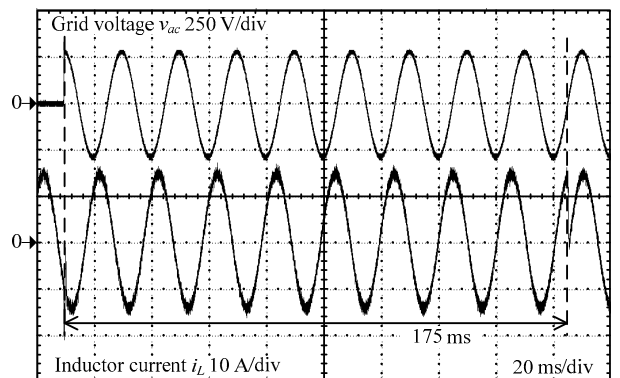
(a) Waveform of ZVRT operation.
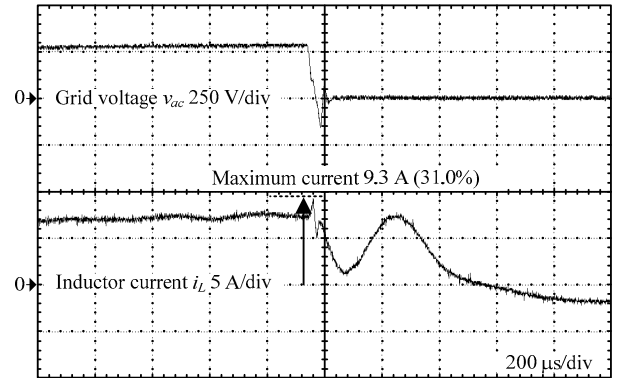
(b) Voltage drop operation.
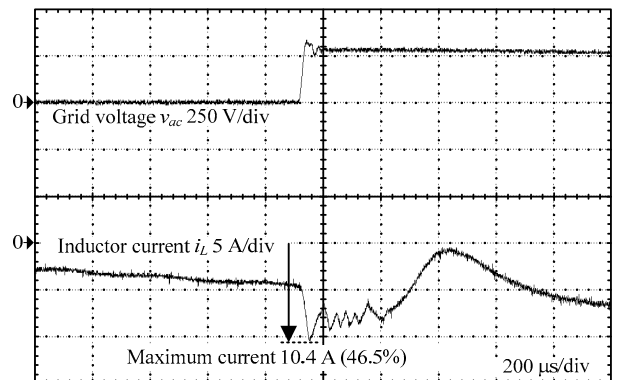
(c) Voltage recovery operation.

(d) Stable period of output after voltage recovery.
Fig. 12. Experimental result of proposed FRT control method during short grid failure. The grid-connected inverter operates without disconnecting from the grid.

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