### Paper

## Design Guidelines of Circuit Parameters for Modular Multilevel Converter with H-bridge Cell

Toshiki Nakanishi<sup>\*a)</sup> Student member, Jun-ichi Itoh<sup>\*</sup> Senior member

(Manuscript received Jan. 00, 20XX, revised May 00, 20XX)

This paper presents theoretical formulae for circuit parameter design as design guidelines in a step-down rectifier in a power system connected to a 6.6-kV AC power grid, where a modular multilevel converter (MMC) is applied. In particular, this paper focuses on the design of heat sinks, capacitors, and arm inductors. In addition, the worst case for each component design is shown as the first step of the converter design. First, the formula for the ripple current in the electrolytic capacitor is derived in order to evaluate the capacitor lifetime. Second, the formulae for the semiconductor losses are clarified on the basis of the analysis of the arm current. Third, the formula for the ripple current in the arm inductor is derived on the basis of the ripple current model of a chopper circuit. Finally, all formulae are verified by experiments with a miniature model. It is confirmed that theoretical values from formulae agree with the measured values with the errors lower than 12%.

Keywords : Modular Multilevel Converter, High power density design, H-bridge cell, Step-down rectifier

#### 1. Introduction

Recently, DC micro-grids have been actively researched as next generation power distributions<sup>(1)-(3)</sup>. In the DC micro-grid, a transformer and a rectifier are required in order to convert from 6.6-kV AC voltage to several hundred volts DC voltage<sup>(2)-(3)</sup>. However, the isolated transformer is bulky due to the operation at the utility frequency. In addition, the conventional power system for 6.6-kV AC grid also requires bulky static capacitors for power factor correction and series reactors for the reduction of the harmonic distortion of the grid current<sup>(4)-(8)</sup>.

For the volume reduction of the above system, neutral-pointclamped (NPC) converters or diode-clamped converters have been actively researched in order to avoid the utilization of the bulky transformer<sup>(9)</sup>. In the three-level diode-clamped converter, the high voltage IGBTs with the voltage rating more than 6.5 kV are required. However, it is generally difficult to employ the IGBTs with the voltage rating more than 6.5 kV due to their unique specifications. Moreover, if the five-level diode-clamped converter is applied to solve the problem with the switching devices, the voltage balancing circuit is required as the auxiliary circuit in order to correct the unbalanced voltage among four capacitors in the DC link<sup>(9)</sup>. In addition, the above converters cannot achieve step-down rectification. Therefore, the specification of the NPC converter are different from the requirements of the proposed system.

On the other hand, the employment of a modular multilevel converter (MMC) with an H-bridge cell can achieve the step-down operation without the isolated transformer in the DC micro-gird<sup>(10)</sup>. The MMC has been actively researched as a next generation high voltage power converter without the bulky transformer<sup>(11)-(14)</sup>. In addition, the H-bridge cell type MMC also achieves the reduction of static capacitors and series reactors because the MMC controls

\* Nagaoka University of Technology

the output DC voltage and the circulating current for the volume reduction of the MMC and the isolated DC-DC converter.
 In AC-DC converters using the MMC topology for the medium voltage application, (i) capacitors, (ii) heat sinks and (iii) arm

voltage application, (i) capacitors, (ii) heat sinks and (iii) arm inductors are the majorities of the overall volume as same as general power converters<sup>(15)</sup>. The design guideline in order to achieve each individual purpose such as the high power density or high efficiency has been considered so far<sup>(16)-(35)</sup>.

the input power factor and reduces the harmonic distortion without

large capacitors and inductors<sup>(14)</sup>. Besides, it is possible to apply 1.7-kV or 1.2-kV IGBTs with the low loss characteristic with the

increase in the number of cells in the MMC. Therefore, these IGBTs

On the other hand, in the output side of the MMC, an isolated DC-DC converter is connected to achieve the isolation between the

AC power grid and the DC micro-grid<sup>(10)</sup>. Thus, the high step-down

function from 6.6 kV to several hundred volts is accomplished by

both the MMC and the isolated DC-DC converter. In the H-bridge

cell type MMC, the degree of freedom in the design of the output

DC voltage is high because the output DC voltage of the MMC is

easily controlled by adjusting the DC bias in each cell output

voltage<sup>(14)</sup>. Moreover, the rating of the circulating current (DC

component) changes responding to the output voltage when the

power rating is same. Thus, it should determine the combination of

can operate at the high frequency for the volume reduction.

First, a capacitor design based on the ripple voltage have been reported<sup>(18)-(19)</sup>. In the MMC, the capacitor voltage includes the ripple component. Consequently, the capacitance is generally determined dependent on the ripple factor as with general power converters. Moreover, the formula of the capacitor voltage included the ripple voltage has been already clarified. In addition, customized film capacitors or ceramic capacitors under a fixed number of cells have also been investigated as the cell capacitor<sup>(20)-(21)</sup>. When the film capacitor or the ceramic capacitor is used in the MMC, the capacitor volume is evaluated by the capacitance and the electrostatic energy<sup>(21)-(23)</sup>. On the other hand, the employment of the electrolytic capacitor to the cell in the prototype or the miniature

a) Correspondence to: Toshiki Nakanishi.

E-mail: nakanishi@stn.nagaokaut.ac.jp

<sup>1603-1,</sup> Kamitomioka-machi, Nagaoka, Niigata, Japan

model of the MMC has also been reported<sup>(24)-(26)</sup>. In general, it is commonly known that the capacitance per unit volume of the electrolytic capacitor is high compared to film capacitors or ceramic capacitors. Moreover, the required voltage rating is simply achieved by changing the number of the series connected capacitors. Besides, in terms of the lifetime, it is possible to adjust the ripple current of one capacitor by changing the number of the parallel connected capacitors. In the MMC, the capacitor voltage rating changes depending on the number of cells because the divided voltage of each cell is varied. In addition, the ripple current of the capacitor is varied by the output DC voltage of the MMC because the DC component of the arm current changes. However, the ripple current of the cell capacitor has not been thoroughly considered although the ripple current is the important factor in the design guideline for the electrolytic capacitor. In addition, the formulae of the ripple current and the ripple voltage focused on the number of cells and the output voltage of the MMC have not been also clarified.

Second, in terms of the heat sink design, the loss analysis and the breakdown of the semiconductor losses have been reported in the chopper cell type MMC<sup>(27)-(28)</sup>. Besides, the evaluation of the heat sink volume in IGBTs with the voltage rating of which varies from 600 V to 6.5 kV has been also discussed<sup>(29)</sup>. However, the formulae of the semiconductor losses in the H-bridge cell type MMC have not been thoroughly clarified. In the H-bridge cell type MMC, the arm current is varied by the input active power i.e. the output power because the circulating current changes. In particular, the arm current becomes AC including the DC component or DC including the AC component. Hence, it is necessary to analyze the current path in the H-bridge cell and the magnitude of each device current based on the arm current. Thus, the semiconductor loss should be clarified based on the analysis of the arm current. However, the detail analysis, the process of the formula clarification and the verification of the theoretical formula have not been considered.

Third, as the design of the arm inductor, the design guideline which the inductance is determined to be several percent of the impedance rating of the MMC has been explained<sup>(30)-(31)</sup>. In addition, the design guideline which focuses on the harmonic components of the circulating current and the resonance phenomenon between the arm inductor and capacitors in cells has been also considered<sup>(32)</sup>. On the other hand, as the design guideline for the inductor in general power converters, the inductance is determined based on the ripple factor of the inductor current<sup>(33)-(34)</sup>. In the MMC, the ripple current changes responding to the switching frequency and the number of cells due to the change of the equivalent switching frequency. In particular, when the unipolar modulation is used in the H-bridge cell, the equivalent switching frequency is different compared to the MMC with the chopper cell. Thus, it is greatly important to consider the relationship between the ripple current of the arm inductor and the equivalent switching frequency including the number of cells as the variables. However, when the unipolar modulation is applied, the design formula of the ripple current in the arm inductor based on the relationship between the ripple current and the equivalent switching frequency has not been thoroughly reported.

The problem of the conventional design method is that the number of cells and the output voltage of the MMC are not focused in the design of the H-bridge cell type MMC. Besides, the fundamental design guideline, i.e. the worst case for the ripple component or the semiconductor loss, has not also been considered due to the above reasons. The formulae for the ripple component or the semiconductor loss have many variables in the MMC. Hence, it is difficult to find the worst case for each circuit component design. In addition, it is also difficult to acquire required values such as the minimum ripple current and the minimum semiconductor loss with circuit simulations, because there are many factors which affect the ripple component or the semiconductor loss. Therefore, it is necessary to clarify the theoretical formulae to find the worst case for each component design in the H-bridge cell type MMC.

This paper presents the theoretical formulae to find the worst case for the circuit parameter design in the H-bridge cell type MMC. The main contribution of this paper is to show the factors which decides the worst case for each component design after the clarification of the theoretical formulae focused on the number of cells and the output voltage of the MMC. It is expected that the discussion of the design for the optimum number of cells and the optimum value of the output voltage will be promoted to achieve for the minimum ripple component or the minimum semiconductor loss. This paper is a first step of the optimum design for the H-bridge cell type MMC.

In this paper, the formulae of (i) the ripple current of the cell capacitor, (ii) semiconductor loss and (iii) the ripple current of the arm inductor are derived. First, the formula of the ripple current in the cell capacitor is derived for the lifetime design of the electrolytic capacitor. It is necessary to clarify the relationship between the input power factor and the ripple current because the ripple current changes according to the input active power i.e. the output power. Second, the conduction loss and the switching loss in switching devices are derived based on the analysis of the arm current. The semiconductor losses change depending on the arm current. Thus, it is required to obtain the relationship between the arm current and each switching device loss in order to design the heat sink in the maximum point of the semiconductor loss. Third, the formula of the ripple current in the arm inductor is derived in order to determine the inductance of the arm inductor. From the relationship between the duty which changes depending to the number of cells and the ripple current, the maximum point of the ripple current is clarified. Finally, the theoretical formulae are verified by using a miniature model in order to obtain the validity of the theoretical formulae.

#### 2. Circuit Configuration

2.1 Conventional power system connected to utility grid of 6.6 kV Fig. 1 shows a structure of the conventional power system of 200 kVA connected to the AC power grid of 6.6 kV. The model of this system is "cubicle-type high-voltage power receiving equipment" which is widely applied in Japan<sup>(4)-(8)</sup>. The conventional power system has several isolated transformers in order to convert the grid voltage of 6.6 kV into the AC distribution voltage of 200 V or 100 V. Moreover, the power system also includes the static capacitors in order to correct the input power factor and the series reactor in order to reduce the harmonic distortion of the grid current. Transformers, static capacitors and series reactors are main factors which increase the system volume. In the conventional system, the component volume which is defined as the total volume of transformers, static capacitors and series reactors is 1605 dm<sup>3 (4)-(8)</sup>.

**2.2** Front-end converter with MMC and isolated DC-DC converter Fig. 2 shows the configuration of the front-end converter using the H-bridge cell type MMC and the isolated DC-DC converter. Each arm of the MMC consists of the arm inductor  $L_a$  and cascaded H-bridge cells in order to operate as the step-down rectifier. The MMC outputs a multi-level voltage waveform which reduces the harmonic distortions of the input current. In addition, the MMC is able to reduce the voltage rating of devices on each cell

due to cascade connections of cells. Therefore, lower voltage rating devices are utilized. On the other hand, the output DC voltage of the MMC depends on the sum of the output average voltage of cells. Thus, the cell output voltage includes both the AC component and the DC component to control the input current and the output voltage. Moreover, the MMC converts the high AC voltage to the DC voltage of several hundred volts. After this step, the DC voltage of 400 V is supplied to the DC bus of the DC distribution by the isolated DC-DC converter. The isolation capability between the AC power grid and the DC micro-grid is achieved by the isolated DC-DC converter. Hence, the high step-down functions from 6.6 kV to several hundred volts is accomplished by both the MMC and the isolated DC-DC converter. As a result, the output voltage rating of the MMC can be designed with a high freedom degree. In the MMC, the circulating current (DC component) is changed responding to the output voltage of the MMC under the conditions of same power rating. Thus, a variety of the combination between the output voltage and the circulating current can be determined for the volume reduction of the MMC and the isolated DC-DC converter.

#### **3.** Control Strategy of Step-Down MMC

**3.1 Control concept for MMC** Fig. 3 shows a control block diagram of the H-bridge cell type MMC<sup>(10)</sup>. The control block consists of the capacitor voltage control, the arm current control and the MMC output voltage control. In addition, the capacitor voltage control and the capacitor voltage balancing control.

**3.2** Capacitor voltage averaging control The capacitor voltage averaging control is employed in order to maintain the average value of all capacitor voltages in the arm<sup>(35)</sup>. Therefore, the average value of all capacitor voltages has to be calculated in each arm. The output value of the PI controller is given as the command of a positive sequence component in the arm current. Moreover, the voltage command  $\nu_{c}$ \*is given by (1).

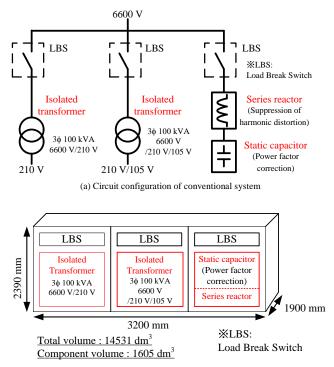
where *E* is an root-mean-square (rms) value of the input line-to-line voltage,  $V_{mmc}$  is the output DC voltage of the MMC, and *n* is the number of cells at each leg.

**3.3 Arm current control** The arm current control is employed to control the AC component of the arm current which flows from the AC power grid. The AC component is defined as the positive sequence component. From the previous section, the command of the positive sequence component is generated by the capacitor voltage averaging control. In other words, the positive sequence component is controlled in order to maintain the average value of all capacitor voltages in each arm constant.

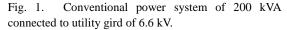
On the other hand, the arm current also includes the DC component (a zero sequence component). Thus, it is necessary to eliminate only the zero sequence component from the arm current in order to control the capacitor voltage.

**3.4 MMC output voltage control** In the MMC output voltage control, the command of the output DC voltage  $V_{mmc}^*$  is added into the output value of the controller in the arm current control. The zero sequence component is applied to supply the power to the output side of the MMC. Moreover, the output DC voltage is divided by each cell. Thus, the output DC voltage of one cell is fundamentally set as  $V_{mmc}^*/n$ .

3.5 Capacitor voltage balancing control The



(b) Volume of conventional system



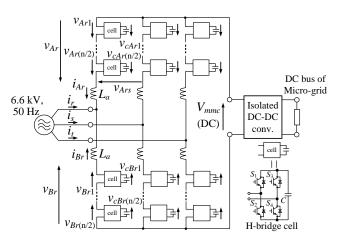


Fig. 2. Circuit configuration of front-end converter with H-bridge cell type MMC and isolated DC-DC converter.

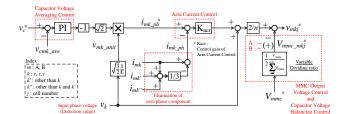


Fig. 3. Control block diagram for each arm in H-bridge cell type MMC. Note that *m* is the index of the arm group A or B, *k*, k' or k'' is the index of the phase such as *r*, *s* and *t*, and *j* is the index of the cell number.

capacitor voltage balancing control corrects the unbalanced voltage which occurs among capacitors in same arm. In the conventional

balancing control, it is required to design the control parameters. On the other hand, in the proposed voltage balancing control, it is not necessary to design control parameters<sup>(35)</sup>. In particular, each cell has the DC bias of  $V_{mmc}^*/n$  in the ideal state. In the proposed method, the dividing ratio is adjusted automatically depending on the capacitor voltage. Each cell output power is adjusted by varying the dividing ratio. Therefore, each capacitor voltage is automatically balanced by varying the dividing ratio.

#### 4. Clarification of Ripple Voltage and Ripple Current Formulae for Capacitor Design

In this chapter, the formula of the ripple current is clarified for the design guideline of the electrolytic capacitor. In this paper, it is assumed that the electrolytic capacitor is applied as the cell capacitor. In fact, the employment of the electrolytic capacitor to the prototype MMC has been reported<sup>(24)-(25)</sup>. It is well known that it is possible to easily vary the voltage rating and the rated ripple current by varying the numbers of series connection and the parallel connection of electrolytic capacitors. On the other hand, the ripple current which flows to the electrolytic capacitor affects the lifetime of the capacitor. Thus, the ripple current is one of the important factors for the MMC design.

**4.1 Calculation of capacitor's voltage rating** The capacitor voltage in the cell depends on both the input voltage and the output voltage. The output DC voltage  $V_{nunc}$  is applied to each leg because each leg is connected to the load in parallel. In addition, the maximum value of the input phase voltage is applied to each arm. Therefore, each capacitor voltage depends on both the input voltage and the output voltage. The capacitor voltage command  $v_c^*$  is given by (1). Note that the modulation index  $\lambda$  is set to 0.95 or less. In the circuit analysis of this paper, the voltage drop on the arm inductor is ignored in order to consider the fundamental operation. As an actual fact, the voltage drop on the arm inductor is sufficiently small compared to the input phase voltage and the output voltage of the MMC because the arm inductance in the MMC can be reduced.

**4.2 Calculation of ripple voltage** In order to employ the ripple current as the evaluation index for the selection or the design of the electrolytic capacitor, it is important to understand the relationship between the ripple current and the circuit parameters of the MMC. Thus, it is necessary to clarify the formula of the ripple current which flows to the electrolytic capacitor. In this section, as a first step of the clarification for the formula of the ripple current, the formula of the capacitor voltage is clarified.

First, the cell output voltage  $v_{cell}$  is given by (2). The formula of (2) means that the input phase voltage is divided by each cell per arm and the output DC voltage  $V_{nunc}$  is divided by each cell per leg. On the other hand, the arm current  $i_{arm}$ , which includes the AC component and the DC component, is given by (3). The AC current flows from the AC grid in order to maintain the capacitor voltage. Whereas, the DC current flows into the load in order to supply the power. Moreover, the arm current  $i_{arm}$  flows into each cell in same arm. Note that the sign of positive or negative is decided based on the lower arm of Fig. 2.

$$v_{cell}(t) = \frac{1}{n} \left( 2\sqrt{\frac{2}{3}} E \cos(\omega t + \phi) + V_{mmc} \right) \dots (2)$$
$$i_{amm}(t) = -\frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \cos \omega t + \frac{P}{3V_{mmc}} \dots (3)$$

where S is an apparent input power, P is an input active power, Q is

an input reactive power, and  $\phi$  is an input phase difference. The apparent input power *S* is defined by (4).

$$S = \sqrt{P^2 + Q^2} \quad \dots \qquad (4)$$

From (2) and (3), the instantaneous power of the cell is calculated. The energy which is stored in the capacitor is calculated by the integration of the instantaneous power and is given by (5).

$$W_{c}(t) = \int v_{cell} i_{amn} dt$$
  
=  $-\frac{1}{2} \sqrt{\frac{2}{3}} \frac{V_{mnc} S}{n\omega E} \sin \omega t + \frac{2}{3} \sqrt{\frac{2}{3}} \frac{EP}{n\omega V_{mnc}} \sin (\omega t + \phi)$   
 $-\frac{S}{6n\omega} \sin(2\omega t + \phi) + W_{c0}$ 

where  $W_{C0}$  is the constant of integration, which does not change with time. Thus, the constant of integration  $W_{C0}$  is defined as the average value of the energy which is stored in the capacitor. The relationship between the capacitor voltage  $v_c(t)$  and the energy  $W_C(t)$  is given by (6) in terms of the electrostatic energy.

$$W_{c}(t) = \frac{1}{2} C v_{c}(t)^{2}$$
 (6)

From (5) and (6), the capacitor voltage  $v_c(t)$  is given by (7). Note that the theoretical formula is calculated by the linear approximation of Taylor expansion.

$$v_{c}(t) = V_{C0} - \frac{1}{2} \sqrt{\frac{2}{3}} \frac{V_{mmc} S}{n\omega CE V_{C0}} \sin \omega t$$
  
+  $\frac{2}{3} \sqrt{\frac{2}{3}} \frac{EP}{n\omega C V_{mmc} V_{C0}} \sin(\omega t + \phi) \cdots (7)$   
-  $\frac{S}{6n\omega CV_{C0}} \sin(2\omega t + \phi)$ 

where the constant value  $V_{C0}^2$  is defined by  $2W_{C0}/C$ ,  $V_{C0}$  is defined as the average value of the capacitor voltage because  $W_{C0}$  does not change with time.

The ripple voltage includes the fundamental frequency component whose frequency is same as the frequency of the input voltage source and the second-order frequency component with twice the frequency of the input frequency. Moreover, the MMC has to control the power factor and reduce the harmonic distortion in order to eliminate the static capacitors and the series reactor. Thus, it is necessary to evaluate the ripple voltage over the wide range of the input power factor.

Fig. 4 shows the relationship between the input power factor and the ripple voltage. The fundamental frequency component and the second-order frequency component is drawn by (7). The second-order frequency component of the ripple voltage does not change against the change of the input power factor because the input apparent power *S* is constant. On the other hand, the fundamental frequency component becomes maximum when the input power factor is 1.0 or -1.0. Thus, it is necessary to design the capacitance only when the input power factor is 1.0, i.e. the worst case.

**4.3 Clarification of ripple current** In this section, the formula of the ripple current in the cell capacitor is clarified. In general, the ripple current value of the capacitor is shown in the datasheet of commonly-marketed electrolytic capacitors which are generally implemented into products. The capacitor should be selected in order that the ripple current value which flows to each

capacitor is sufficiently small compared to the specified value on each datasheet in terms of the lifetime. Additionally, the number of the capacitors which are connected in parallel on each cell should be increased in order to meet the specification of the ripple current. Hence, it is necessary to clarify the relationship between the ripple current and the circuit parameters in order to design the lifetime.

The relationship between the capacitor current  $i_c$  and the capacitor voltage  $v_c$  is given by (8).

$$i_c = C \frac{dv_c}{dt}$$
(8)

From (7) and (8), it is concluded that the relationship between the input phase difference  $\phi$  and the maximum value does not change even with the use of the differential of the ripple voltage. Therefore, the ripple current reaches maximum when the input phase difference  $\phi$  is 0. The maximum RMS value of the fundamental frequency component in the ripple current  $I_{C_{-}1}$  is given by (9). As a result, the maximum RMS value of the ripple current does not change when the number of cells and the capacitance changes.

$$I_{C_{-1}} = \sqrt{\frac{1}{3}} \frac{\lambda P}{\left(2\sqrt{\frac{2}{3}}E + V_{nnc}\right)} \left(\frac{2}{3} \frac{E}{V_{nnc}} - \frac{1}{2} \frac{V_{nnc}}{E}\right) \dots (9)$$

In conclusion, as the worst case for the electrolytic capacitor design in the MMC, the ripple current should be designed when the input power factor is 1.0. In particular, the fundamental frequency component with the same frequency as the grid frequency is maximum in the unity power factor.

#### 5. Clarification of Semiconductor Losses for Heat Sink Design

In this chapter, the formulae of semiconductor losses in the Hbridge cell are clarified for the design of the heat sink. First, it is necessary to analyze the arm current which flows to each switching device because the arm current becomes AC including the DC component or DC including the AC component according to the input power factor. Second, the formulae of semiconductor losses are derived based on the analysis of the arm current.

**5.1 Analysis of arm current** Fig. 5 shows the circuit model of the H-bridge cell in order to analyze the semiconductor losses. As a first step of the circuit analysis, it is necessary to consider the circuit operation in an ideal state. Hence, the capacitor is replaced with the ideal voltage source in order to neglect the effect of the ripple voltage. Similarly, the inductor is replaced with the ideal current source in order to neglect the effects of the ripple current and the harmonic distortion.

First, the cell output voltage and the arm current in the lower side of the MMC are defined by (2) and (3) respectively. The cell output voltage and the arm current includes the DC component and the AC component. From (3), the condition which the arm current becomes the DC current including the AC component is given by (10).

$$\frac{P}{3V_{nmc}} \ge \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \tag{10}$$

The condition where the arm current becomes DC including the AC component is given by (11).

$$\frac{2}{3}\sqrt{\frac{3}{2}}\frac{E}{V_{mnc}}\cos\phi - 1 \ge 0 \cdots (11)$$

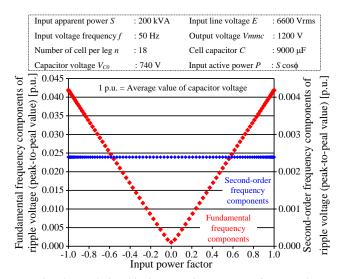


Fig. 4. Relationship between input power factor and ripple voltage.

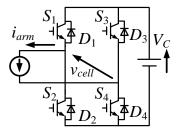


Fig. 5. Circuit model of H-bridge cell for loss analysis.

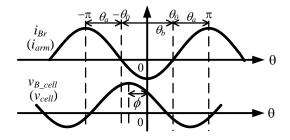


Fig. 6. Relationship between cell output voltage and arm current in lower side of MMC.

In contrast, the arm current becomes AC which includes the DC component when the left part of (11) is negative. The angle  $\theta_0$  whose direction of the arm current changes is defined by (12) when the arm current is AC.

From (12), the angle  $\theta_a$  depicting the duration when the direction of the arm current becomes positive is given by (13). In contrast, the angle  $\theta_b$  depicting the duration when the arm current becomes negative is given by (14).

$$-\theta_0 \le \theta_b \le \theta_0 \tag{14}$$

Fig. 6 shows the relationship among the cell output voltage, the arm current and the angles  $\theta_a$  and  $\theta_b$ .

5.2 Calculation of conduction loss In the H-bridge cell,

the semiconductor losses are same in pair devices. For example,  $S_1$  and  $S_4$  which are shown in Fig. 5 operate in pairs. Moreover,  $S_2$  and  $S_3$  operate in pairs. Therefore, the semiconductor losses of only one leg in the H-bridge cell are calculated.

The average value of the conduction loss during one cycle  $P_{con}$  is given by (15)<sup>(36)</sup>.

$$P_{con} = \frac{1}{2\pi} \int_{\alpha}^{\beta} \left( V_0 + R i_{B_{cell}} \right) i_{B_{cell}} d_{SD} \ d\theta \ \cdots \ (15)$$

where  $V_0$  is the voltage drop of the switching device when the current is zero, R is the on-resistance of the device,  $i_{B\_cell}$  is the current which flows to the device,  $d_{SD}$  is the duty of each switching device<sup>(36)</sup>. The voltage drop  $V_0$  and the on-resistance R are obtained from the datasheets.

When the arm current becomes positive, by substituting the variable number  $\theta$  of (15) by the angle  $\theta_a$  of (13), the current which flows to S<sub>1</sub>, S<sub>4</sub>, D<sub>2</sub> and D<sub>3</sub> is given by (16). In contrast, when the arm current becomes the negative, by substituting the variable number  $\theta$  of (15) by the angle  $\theta_b$  of (14), the current which flows to S<sub>2</sub>, S<sub>3</sub>, D<sub>1</sub> and D<sub>4</sub> is given by (17).

$$i_{B_{cell_{P}}} = -\frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \cos\theta_a + \frac{P}{3V_{nmc}}$$
(16)  
$$i_{B_{cell_{N}}} = \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \cos\theta_b - \frac{P}{3V}$$
(17)

Next, each duty is given by (18), (19), (20) and (21) respectively.

$$d_{S2} = \frac{1}{2} \left\{ 1 - \frac{1}{nV_c} \left( 2\sqrt{\frac{2}{3}E\cos(\theta_b + \phi)} + V_{mmc} \right) \right\} \cdots (19)$$

$$d_{D1} = 1 - d_{S2}$$
(20)

where  $V_C$  is the capacitor voltage.

Each conduction loss of  $S_1$ ,  $S_2$ ,  $D_1$  and  $D_2$  is given by (22), (23), (24) and (25) respectively.

$$P_{B_{S_{1}}Con} = \frac{V_{0_{SW}}}{4\pi} \left[ \left( 1 + \frac{V_{mmc}}{nV_{C}} \right) \left\{ \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} + \frac{2}{3} \frac{P}{V_{mmc}} (\pi - \theta_{0}) \right\} \\ + \frac{1}{nV_{C}} \left\{ -\frac{P}{3} \left( 2(\pi - \theta_{0}) - \sin 2\theta_{0} \right) - \frac{4}{3} \sqrt{\frac{2}{3}} \frac{PE}{V_{mmc}} \cos \phi \sin \theta_{0} \right\} \right] \\ + \frac{R_{SW}}{4\pi} \left[ \left( 1 + \frac{V_{mmc}}{nV_{C}} \right) \left\{ \frac{1}{12} \frac{S^{2}}{E^{2}} \left( 2(\pi - \theta_{0}) - \sin 2\theta_{0} \right) \right. \\ + \frac{2}{3} \sqrt{\frac{2}{3}} \frac{PS}{EV_{mmc}} \sin \theta_{0} + \frac{2}{9} \frac{P^{2}}{V_{mmc}^{2}} (\pi - \theta_{0}) \right\} \\ + \frac{1}{nV_{C}} \left\{ -\frac{1}{6} \sqrt{\frac{2}{3}} \frac{PS}{E} \left( 3\sin \theta_{0} + \frac{1}{3}\sin 3\theta_{0} \right) \right. \\ \left. - \frac{4}{9} \frac{P^{2}}{V_{mmc}} \left( (\pi - \theta_{0}) - \frac{1}{2}\sin 2\theta_{0} \right) - \frac{4}{9} \sqrt{\frac{2}{3}} \frac{P^{2}E}{V_{mmc}^{2}} \cos \phi \sin \theta_{0} \right\} \right]$$
(22)

$$P_{B_{-}S2_{-}Con} = \frac{V_{0_{-}SW}}{4\pi} \left[ \left( 1 - \frac{V_{mm}}{nV_{c}} \right) \left\{ \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} - \frac{2}{3} \frac{P}{V_{mm}} \theta_{0} \right\} - \frac{1}{nV_{c}} \left\{ \frac{P}{3} \left( 2\theta_{0} + \sin 2\theta_{0} \right) - \frac{4}{3} \sqrt{\frac{2}{3}} \frac{PE}{V_{mmc}} \cos \phi \sin \theta_{0} \right\} \right] + \frac{R_{SW}}{4\pi} \left[ \left( 1 - \frac{V_{mm}}{nV_{c}} \right) \left\{ \frac{1}{12} \frac{S^{2}}{E^{2}} \left( 2\theta_{0} + \sin 2\theta_{0} \right) - \frac{2}{3} \sqrt{\frac{2}{3}} \frac{PS}{EV_{mm}} \sin \theta_{0} + \frac{2}{9} \frac{P^{2}}{V_{mmc}^{2}} \theta_{0} \right\} - \frac{1}{nV_{c}} \left\{ \frac{1}{6} \sqrt{\frac{2}{3}} \frac{PS}{E} \left( 3\sin \theta_{0} + \frac{1}{3}\sin 3\theta_{0} \right) - \frac{4}{9} \frac{P^{2}}{V_{mmc}} \left( \theta_{0} + \frac{1}{2}\sin 2\theta_{0} \right) + \frac{4}{9} \sqrt{\frac{2}{3}} \frac{P^{2}E}{V_{mmc}^{2}} \cos \phi \sin \theta_{0} \right\} \right]$$
(23)

$$P_{B_{-}D1_{-}Con} = \frac{V_{0_{-}FWD}}{4\pi} \left[ \left( 1 + \frac{V_{mmc}}{nV_{C}} \right) \left\{ \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} - \frac{2}{3} \frac{P}{V_{mmc}} \theta_{0} \right\} \\ + \frac{1}{nV_{C}} \left\{ \frac{P}{3} \left( 2\theta_{0} + \sin 2\theta_{0} \right) - \frac{4}{3} \sqrt{\frac{2}{3}} \frac{PE}{V_{mmc}} \cos \phi \sin \theta_{0} \right\} \right] \\ + \frac{R_{FWD}}{4\pi} \left[ \left( 1 + \frac{V_{mmc}}{nV_{C}} \right) \left\{ \frac{1}{12} \frac{S^{2}}{E^{2}} \left( 2\theta_{0} + \sin 2\theta_{0} \right) \right. \\ \left. - \frac{2}{3} \sqrt{\frac{2}{3}} \frac{PS}{EV_{mmc}} \sin \theta_{0} + \frac{2}{9} \frac{P^{2}}{V_{mmc}^{2}} \theta_{0} \right\} \\ + \frac{1}{nV_{C}} \left\{ \frac{1}{6} \sqrt{\frac{2}{3}} \frac{PS}{E} \left( 3\sin \theta_{0} + \frac{1}{3}\sin 3\theta_{0} \right) \right. \\ \left. - \frac{4}{9} \frac{P^{2}}{V_{mmc}} \left( \theta_{0} + \frac{1}{2}\sin 2\theta_{0} \right) + \frac{4}{9} \sqrt{\frac{2}{3}} \frac{P^{2}E}{V_{mmc}^{2}} \cos \phi \sin \theta_{0} \right\} \right]$$
(24)

$$P_{B_{-D2_{-}Con}} = \frac{V_{0_{-}FWD}}{4\pi} \left[ \left( 1 - \frac{V_{nmc}}{nV_{c}} \right) \left\{ \sqrt{\frac{2}{3}} \frac{S}{E} \sin\theta_{0} + \frac{2}{3} \frac{P}{V_{nmc}} (\pi - \theta_{0}) \right\} - \frac{1}{nV_{c}} \left\{ -\frac{P}{3} \left( 2(\pi - \theta_{0}) - \sin 2\theta_{0} \right) - \frac{4}{3} \sqrt{\frac{2}{3}} \frac{PE}{V_{mmc}} \cos\phi\sin\theta_{0} \right\} \right] + \frac{R_{FWD}}{4\pi} \left[ \left( 1 - \frac{V_{nmc}}{nV_{c}} \right) \left\{ \frac{1}{12} \frac{S^{2}}{E^{2}} \left( 2(\pi - \theta_{0}) - \sin 2\theta_{0} \right) + \frac{2}{3} \sqrt{\frac{2}{3}} \frac{PS}{EV_{nmc}} \sin\theta_{0} + \frac{2}{9} \frac{P^{2}}{V_{mmc}^{-2}} (\pi - \theta_{0}) \right\} \right]$$

$$- \frac{1}{nV_{c}} \left\{ -\frac{1}{6} \sqrt{\frac{2}{3}} \frac{PS}{E} \left( 3\sin\theta_{0} + \frac{1}{3}\sin3\theta_{0} \right) - \frac{4}{9} \sqrt{\frac{2}{3}} \frac{P^{2}E}{V_{nmc}^{-2}} \cos\phi\sin\theta_{0} \right\} \right]$$

$$(25)$$

**5.3** Calculation of switching loss and recovery loss The switching loss  $P_{SW}$  and the recovery loss  $P_{Rec}$  are given by  $(26)^{(36)}$ .

$$P_{SW(Rec)} = V_C \frac{1}{2\pi} \int_{\alpha}^{\beta} i_B d\theta \frac{W}{V_{dcd} I_{md}} f_c$$
 (26)

where *w* is the loss energy which is described in the datasheet,  $V_{dcd}$  and  $I_{md}$  are the voltage value and the current value when *w* is measured,  $f_c$  is the carrier frequency<sup>(36)</sup>.

Each switching loss in  $S_1$  and  $S_2$  is given by (27) and (28)

respectively. Similarly, each recovery loss in  $D_1$  and  $D_2$  is given by (29) and (30) respectively.

$$P_{B_{-}S1_{-}SW} = \frac{V_{c}}{\pi} \left\{ \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} + \frac{P}{3V_{nnc}} (\pi - \theta_{0}) \right\} \frac{w_{on} + w_{off}}{V_{dcd} I_{nd}} f_{c}$$

$$P_{B_{-}S2_{-}SW} = \frac{V_{c}}{\pi} \left\{ \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} - \frac{P}{3V_{nnc}} \theta_{0} \right\} \frac{w_{on} + w_{off}}{V_{dcd} I_{nd}} f_{c}$$

$$P_{B_{-}D1_{-}Rec} = \frac{V_{c}}{\pi} \left\{ \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} - \frac{P}{3V_{nnc}} \theta_{0} \right\} \frac{w_{r}}{V_{dcd} I_{nd}} f_{c}$$

$$P_{B_{-}D2_{-}Rec} = \frac{V_{c}}{\pi} \left\{ \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} + \frac{P}{3V_{nnc}} \theta_{0} \right\} \frac{w_{r}}{V_{dcd} I_{nd}} f_{c}$$

$$(29)$$

$$P_{B_{-}D2_{-}Rec} = \frac{V_{c}}{\pi} \left\{ \frac{1}{2} \sqrt{\frac{2}{3}} \frac{S}{E} \sin \theta_{0} + \frac{P}{3V_{nnc}} (\pi - \theta_{0}) \right\} \frac{w_{r}}{V_{dcd} I_{nd}} f_{c}$$

$$(30)$$

**5.4 Relationship between input power factor and semiconductor losses** The relationship between the input power factor and semiconductor losses of the H-bridge cell is clarified in order to design the heat sink in the worst case. The formulae of the semiconductor losses include the number of cells as the variable. However, the switching device should be selected when the number of cells changes. The semiconductor loss drastically changes depending to the loss characteristic of the applied switching device. Therefore, this paper focuses on only the relationship between the input power factor and the semiconductor loss as the fundamental consideration of the design in the MMC.

Fig. 7 shows the comparison result of the theoretical formula of the semiconductor loss and the simulation. Note that the input apparent power S is constant. The theoretical values of the formulae agree with the simulation values in the maximum error of 1.0% or less even though the arm current changes from AC to DC in the input power factor of 0.22. Moreover, the losses of S1 and D2 increase as raising of the input power factor. In contrast, the losses of S2 and D1 decrease. The reason why the semiconductor losses change is because the DC component in the arm current changes depending on the input power factor. When the input power factor is zero, the semiconductor loss is generated by only the AC component because the active input power, i.e. the output power is zero. The semiconductor loss which is generated by the DC component increases gradually when the input power factor moves toward 1.0. Thus, the losses of S1 and D2 increase as increasing of the DC component. In contrast, the losses of S2 and D1 decrease to zero because the arm current does not flow to S2 and D1. As a result, the total loss becomes maximum when the input power factor is 1.0.

In conclusion, as the worst case for the semiconductor loss and the design guideline of the heat sink in the MMC, it is necessary to design the heat sink when the input power factor is 1.0. Besides, it is also necessary to focus on the switching device which the loss generates because the semiconductor loss occurs in the particular switching device at the unity power factor.

# 6. Clarification of Ripple Current Formula for Arm Inductor Design

In this chapter, the formula of the ripple current in the arm inductor is clarified for the design of the arm inductor based on the

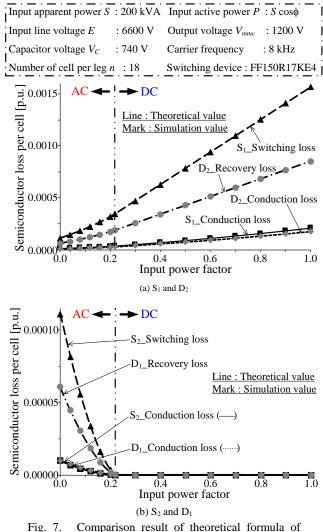


Fig. 7. Comparison result of theoretical formula of semiconductor loss and simulation.

ripple factor of the inductor current. In particular, the ripple current changes drastically as the feature of the multilevel converter when the number of cells or the switching frequency changes. Therefore, both the number of cells and the switching frequency should be included in the formula of the ripple current as the variable. First, the relationship between the ripple current and the number of cells is clarified by the equivalent circuit model in the simulation. Second, from the derived relationship, the formula of the ripple current is clarified based on a chopper circuit. Finally, the theoretical value with the formula and the simulation result are compared.

**6.1 Modulation for H-bridge cell** Fig. 8 shows the diagram of the unipolar modulation for the H-bridge cell (ex.  $v_{Arj}^*$ ). In Fig. 5, the leg of the H-bridge cell is constructed by S<sub>1</sub> and S<sub>2</sub>. The other leg is constructed by S<sub>3</sub> and S<sub>4</sub>. The switching patterns of S<sub>1</sub> and S<sub>2</sub> are determined by the voltage command  $v_{Arj}^*$ . Moreover, the switching patterns of S<sub>3</sub> and S<sub>4</sub> are determined by the inverted voltage command  $-v_{Arj}^*$ . In the H-bridge type circuit such as the grid-tied inverter with the unipolar modulation, the waveform of the inverter output voltage is three-level.

In addition, the phase-shifted triangular carrier is applied to each cell. The phase shift angle  $\theta_{PF}$  is determined by (31).

$$\theta_{\rm PF} = 2\pi \,/\, n \, \cdots \, (31)$$

where n is the number of cells per leg.

Note that the phase shift angle in each cell is determined based on the arm. On the other hand, it is possible to reduce the ripple component of the output voltage or the ripple component of the input current by adjusting the phase shift angles in the upper arm and the lower arm<sup>(37)</sup>. The phase shift angles in each arm should be set according to the objectives of the user's system.

In the MMC, the number of levels in the output voltage waveform is determined by the number of cells. In particular, in the H-bridge cell type MMC, the number of levels of the arm output voltage including the zero level is determined by (32).

where  $N_{ao}$  is the number of levels of the arm output voltage.

**6.2** Analysis of ripple current on each arm inductor with equivalent circuit model As a first-step of the arm inductor design, it is necessary to clarify the relationship between the ripple current and the number of cells.

Fig. 9 shows the equivalent circuit model of the single-phase circuit in the MMC. The circuit operation and the change of the ripple current are simply determined by the single-phase circuit. In the equivalent circuit, the cell capacitor is replaced by the ideal voltage source to neglect the ripple voltage of the capacitor. Note that the output voltage of the cell is determined by (2). Therefore, the total output voltage and the half value of the MMC output voltage. Hence, only the ripple component is extracted.

Fig. 10 shows the frequency analysis of the ripple current. The carrier frequency of the cell is 1.5 kHz. In Fig. 10, the fundamental component is 12 kHz, whereas the frequencies of the second-order component and the third-order component are 24 kHz and 36 kHz.

In the H-bridge cell, with the employment of the unipolar modulation, the output voltage of the cell has twice the frequency of the carrier frequency. The equivalent switching frequency of the cell total output voltage  $v_{Br}$  in each arm  $f_{tc\_eq}$  is given by (33).

$$f_{ic\_eq} = \frac{n}{2} * 2f_c = nf_c$$
(33)

From (33), under the condition which the number of cells is 8 and the carrier frequency is 1.5 kHz, the equivalent switching frequency  $f_{ic\_eq}$  is 12 kHz. It is confirmed that the theoretical value by (33) is equal to the result from the frequency analysis. Moreover, the above result implies that the frequency of the ripple current on each arm inductor is determined by the equivalent switching frequency  $f_{ic\_eq}$ .

From the above result, in following considerations of the ripple current, only the lower arm in Fig. 9 is focused on.

**6.3** Relationship between duty of switching device and ripple current in chopper circuit The relationship between the duty and the ripple current is clarified based on the general power converter as the fundamental consideration.

Fig. 11 shows the circuit diagram of a chopper circuit and the pattern which shows the relationship between the duty and the ripple current<sup>(38)</sup>. In the chopper circuit, the duty of SW<sub>1</sub> is defined as  $D_{on}$ . In contrast, the duty of SW<sub>2</sub> is defined as  $(1-D_{on})$ . In Fig. 11 (b), the ripple current in the chopper circuit  $\Delta i_{L_cch}$  is varied by  $D_{on}$ .

The peak-to-peak value of the ripple current in the chopper circuit  $\Delta i_{Lpp\_ch}$  is given by (34)<sup>(38)</sup>.

$$\Delta i_{Lpp_{ch}} = \frac{V_{in_{ch}}}{L} T_{on} = \frac{V_{in_{ch}}}{L} D_{on} T$$
(34)

where  $V_{in\_ch}$  is the input voltage, *L* is the inductance,  $T_{on}$  is the ontime of SW<sub>1</sub>, and *T* is the switching cycle.

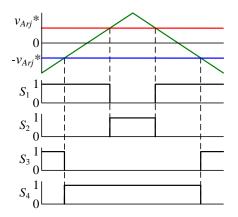


Fig. 8. Unipolar modulation for H-bridge cell (ex. *v*<sub>Arj</sub>\*)

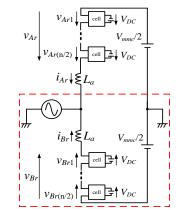


Fig. 9. Equivalent circuit model of single phase circuit in MMC.

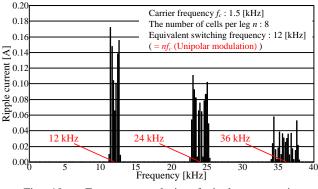


Fig. 10. Frequency analysis of ripple current in simulation.

The boost ratio  $\alpha$  is defined by (35)<sup>(38)</sup>.

$$\alpha = \frac{V_{out\_ch}}{V_{in\_ch}} = \frac{1}{1 - D_{on}}$$
(35)

where  $V_{out\_ch}$  is the output voltage of the chopper circuit.

From (35), the relationship between the input voltage  $V_{in\_ch}$  and the output voltage  $V_{out\_ch}$  is given by (36).

By substituting (36) into (34), the peak-to-peak value  $\Delta i_{Lpp\_ch}$  and the maximum value  $\Delta i_{Lm\_ch}$  is given by (37) and (38) respectively. Note that the average value of the inductor current is set to zero in order to calculate only the ripple component.

$$\Delta i_{Lpp_{ch}} = \frac{V_{in_{ch}}}{L} D_{on} T = \frac{V_{out_{ch}}}{L} T D_{on} (1 - D_{on}) \dots (37)$$

$$\Delta i_{Lm_{ch}} = \frac{\Delta i_{Lpp_{ch}}}{2} = \frac{V_{out_{ch}}}{2L} TD_{on} (1 - D_{on}) \dots (38)$$

**6.4 Definition of duty in each multilevel-voltage step for clarification of ripple current formula** In this section, the ripple current in the arm inductor is clarified. From (37) and (38), the relationship between the duty of the switching device and the ripple current of the inductor in the chopper circuit is clarified. In the same way, it is possible to clarify the formula of the ripple current in the MMC with the duty of the multilevel voltage. The general duty is given by (18), (19), (20) and (21). However, these duties cannot express the variation of the pulse width in each step of the multilevel voltage. As discussed above, the ripple current is varied by the variation of the pulse width. Thus, it is necessary to define a duty with which the variation of the pulse width in each step of the multilevel voltage waveform is considered.

First, the basic level in each step of the multilevel voltage is employed in order to consider the variation of the pulse width in each step of the multilevel voltage.

Fig. 12 (a) shows the multilevel waveform of the cell total output voltage  $v_{Br}$ , the command waveform of the cell total output voltage and the basic level voltage. The multilevel waveform is obtained, whereas the basic level in each step of the multilevel voltage is also obtained as the lower limit of each step. In other words, the MMC outputs the pulse voltage based on the basic level in each step.

Fig. 12 (b) shows the command duty of the cell total output voltage  $v_{Br}$  as well as the duty of the basic level voltage. It is possible to calculate the duty of the basic level voltage  $d_{mlbi}$  by (39).

$$d_{mibl} = \frac{1}{n} \left( N_{mi} - 1 \right) \qquad \qquad N_{mi} = 1, 2, 3 \cdots n$$
 (39)

where  $N_{ml}$  is the index which is varied from 1 to n.

For example, in n = 8, the step of the multilevel voltage varies periodically when  $d_{mlbi}$  is 0.125, 0.250 or 0.375. From (39) and Fig. 12, it is understood that the variation of the duty in each step such as 0.125, 0.250 is determined solely by the number of cells n.

Fig. 12 (c) shows the duty  $d_{mlvs}$  in each step of the cell total output voltage. The duty  $d_{mlvs}$  varies from 0.0 to 1.0 in each step. As the derivation of the duty  $d_{mlvs}$ , first, the difference between the command voltage and the basic level voltage is calculated. Then, the difference is divided by the capacitor voltage. As a result, the duty  $d_{mlvs}$  is defined by (40).

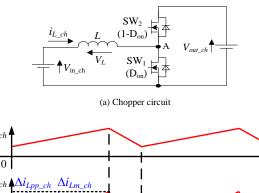
$$d_{mlvs} = |(N_{ml} - 1) - nD|$$
 (40)

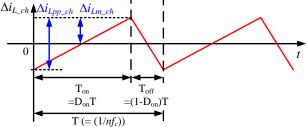
where *D* is the duty of the cell output voltage such as (18). Note that it is possible to replace *D* to  $d_{s1}$ . Moreover,  $N_{ml}$  should be modified according to the number of voltage levels when the number of voltage levels changes depending on the modulation.

**6.5** Clarification of ripple current formula In order to clarify the formula of the ripple current in the arm inductor, each parameter of (38) is replaced respectively as following;

$$V_{out\_ch} = V_C, \ T = \frac{1}{nf_C}, \ D_{on} = d_{mlv}, \ L = L_a$$
 .....(41)

The maximum value of the ripple current  $\Delta i_{Lm}$  is given by (42).





(b) Pattern diagram of ripple current in chopper circuit Fig. 11. Circuit diagram of chopper circuit and pattern diagram of ripple current in chopper circuit.

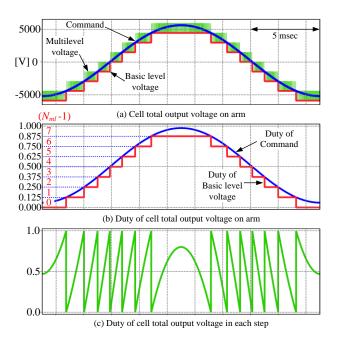


Fig. 12. Multilevel waveform of total output voltage, command of cell total output voltage and basic level voltage.

In (42), the maximum value of the ripple current is varied by the duty  $d_{mlvs}$  which changes frequently. Therefore, the formula of (42) shows the envelope of the ripple current which traces the maximum value of the ripple current. The peak value of the ripple current is given by differentiating (42) with  $d_{mlvs}$  and clarifying the extremum.

From (43), when  $d_{mlvs}$  is 0.5, the formula reaches the extremum. Thus,  $\Delta i_{Lm}$  reaches the peak value when  $d_{mlvs}$  is 0.5.

Fig. 13 shows the multilevel voltage waveform of the cell total

output voltage in one arm, the duty of the cell total output voltage in each step and the waveforms of the ripple current, the envelope of the ripple current and the reversed envelope of the ripple current. It is confirmed that the envelope of the ripple current calculated by (42) traces the maximum value of the ripple current. Additionally, the ripple current has the peak value when  $d_{mlvs}$  is 0.5.

In conclusion, as the worst case for the design of the arm inductor, it is necessary to determine the inductance when the duty  $d_{mlvs}$  in each step of the cell total output voltage is 0.5. In addition, it is

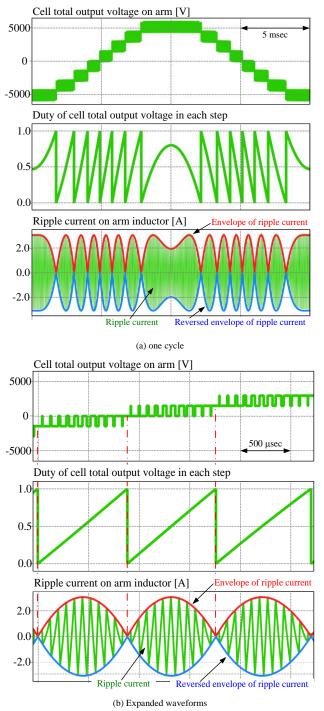


Fig. 13. Multilevel voltage waveform of cell total output voltage in one arm, duty of cell total output voltage in each step and waveforms of ripple current, envelope of ripple current and reversed envelope of ripple current.

necessary to focus on the number of voltage levels because the number of voltage levels changes depending on the modulation.

### 7. Experimental Result in Miniature Model

In this chapter, the theoretical formulae are verified by the experiment in the miniature model. Note that it is assumed that the unity power factor is obtained over entire load range where the theoretical values are calculated. Thus, the apparent power *S* in each formula is replaced by the output power *P*. In addition, the output voltage  $V_{mmc}$  is calculated from the output power and the load resistor in the calculation of theoretical values.

7.1 Verifications of fundamental operation for stepdown rectifier using MMC Table I shows experimental conditions. The miniature model is constructed by four cells per leg. Additionally, as fundamental experiments, the resistance of  $5.3 \Omega$ is employed as the load of the MMC without a smoothing capacitor.

Fig. 14 shows the waveforms of the input phase voltage, the input current of R-phase and the output DC voltage. First, from the waveforms of the input phase voltage and the input current, it is confirmed that the unity power factor is obtained in the input stage. Moreover, the total harmonic distortion (THD) of the input current is 3.1% when the normalized impedance %Z of the inductor is 6.1%. Second, the waveform of the output DC voltage in the lower side of Fig. 14 shows that the step-down rectifier converts from the input voltage of 200 V into the output DC voltage of 75 V, which is maintained at constant. Moreover, it is possible to determine the output DC voltage freely because the output voltage. As a result, the proposed rectifier of the MMC achieves the step-down rectification.

Fig. 15 shows the waveforms of the arm voltage which is the summation of the output voltage of all cells in each arm and the waveform of the line voltage between R-phase and S-phase in the upper side. First, the arm voltage of five levels is obtained because one of the H-bridge cells with the unipolar modulation obtains three-level voltage and the arm has two cells. In addition, the waveforms are not symmetry in the positive side and the negative side because the cell output voltage includes the DC component.

Besides, the waveform of the line voltage between R-phase and S-phase in the upper side is nine levels. However, the multilevel voltage waveform becomes non-uniform. This reason is that the arm voltage is not symmetry in the positive side and the negative side because the command voltage of the cell includes the DC bias with the MMC output voltage control. However, the voltage fluctuation is still smaller compared to the employments of the chopper cells and the H-bridge cells with bipolar modulation. Thus,

Table I. Experimental conditions

| Rated output power $P_O$           | 1000 W           |  |
|------------------------------------|------------------|--|
| Input line voltage E               | 200 Vrms         |  |
| Input voltage frequency            | 50 Hz            |  |
| Output voltage V <sub>mmc</sub>    | 75 V             |  |
| Number of cell per leg <i>n</i>    | 4                |  |
| DC capacitor C                     | 1300 μF          |  |
| Load R                             | 5.3 Ω            |  |
| Carrier frequency                  | 8 kHz            |  |
| Arm inductor <i>L</i> <sub>a</sub> | 8 mH (%Z = 6.1%) |  |

the MMC achieves the size reduction of the arm inductors.

Fig. 16 shows the waveforms of all cell capacitor voltages which are connected to the R-phase leg. The cell capacitor voltage is controlled according to the capacitor voltage command  $v_c^*$ . As a result, the proposed step-down rectifier maintains the capacitor voltage of each H-bridge cell to the voltage command of 130 V. Therefore, the MMC also achieves the capacitor voltage control. In addition, the maximum voltage error between the voltage command of the cell capacitor and the measured voltage is 2% or less.

**7.2** Verifications for theoretical formula of ripple current in capacitor In this section, the verification result for the theoretical formula of the capacitor ripple current is shown. In order to evaluate the ripple current of the capacitor, the frequency analysis of the capacitor voltage is conducted because it is difficult to measure the ripple current of the capacitor directly in the miniature model. However, because the ripple voltage is caused by the ripple current, the validity of the formula is still verified when the measured ripple voltage and the theoretical value by (7) are proved to be same. In particular, the fundamental frequency component and the second-order frequency component of the ripple voltage which are given by (7) and the measured value are compared.

Fig. 17 shows the comparison result of the theoretical value and the measured value of the fundamental frequency component in the ripple voltage. From the result, measured values agree with theoretical values with the small error. In particular, the maximum error between the theoretical value and the measured value is 4.0 %.

Fig. 18 shows the comparison result of theoretical values and measured values of the second-order frequency component. The difference between the theoretical value and the measured value is large. The maximum error is 49.0%. The cause of the large error is the mismatch of the input active power and the output power due to the semiconductor loss and the inductor loss.

Fig. 19 shows the comparison result of theoretical values and measured values of the second-order frequency component based on the input active power. In particular, the input active power is assigned to the power P in the theoretical formula of (7). From the result, the maximum error is reduced to 10.3% compared to the results from Fig. 18. Hence, this result clarifies the reason of the high error between the theoretical value and the measured value of the second-order frequency component in Fig. 18, which is the mismatch of the input active power and the output power due to the semiconductor loss and the inductor loss. In the practical converter, every losses are minimized in order to obtain the high efficiency. Thus, the error in the second-order frequency component based on the output power is small because of the low loss. On the other hand, in the above evaluation, when the output power is low, the error between the theoretical value and the measured value of the secondorder frequency component may be large because the unity power factor is not obtained. However, the ripple voltage including the second-order frequency component should be designed in the worst case when the ripple voltage is maximum in the rated output power. Hence, the effect of the above error is small for the design.

In conclusion, the validity of the formula for the capacitor voltage ripple is verified. Besides, this result confirms that the capacitor ripple current can be calculated exactly by the formula.

**7.3** Verifications for theoretical formula of ripple current in arm inductor In this section, the verification result of the ripple current in the arm inductor is shown.

Fig. 20 shows the expanded waveforms of the lower arm voltage in the R-phase and the arm current. The arm voltage is the total

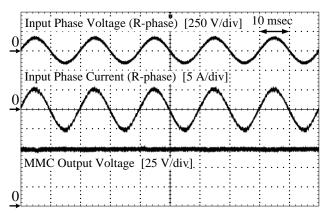


Fig. 14. Waveforms of input phase voltage, input phase current and output voltage.

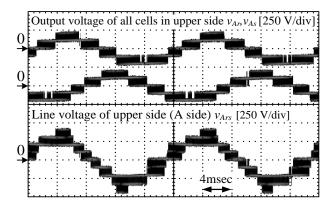


Fig. 15. Waveforms of arm voltage which is the summation of output voltage of all cells in each arm and line voltage between R-phase and S-phase in upper side.

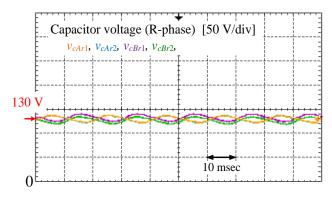


Fig. 16. Waveforms of all capacitor voltage in R-phase.

output voltage of two cells. In addition, the expanded waveform focuses on the output voltage of which the duty in each step of the cell total output voltage  $d_{mlvs}$  is 0.5, i.e. when the ripple current becomes maximum. As shown in Fig. 20, the measured peak-to-peak value of the ripple current is 118 mA. The theoretical value of the twice value by (42) is 124 mA because the peak-to-peak value is twice value of the maximum value. As a result, the error between the theoretical value and the measured value is 4.9%. Note that the inductance used in (42) is measured at the frequency of 32 kHz because 32 kHz is the equivalent frequency of one arm in the miniature model. Moreover, the unipolar modulation is employed.

Fig. 21 shows the comparison result of theoretical values and measured values of the ripple current in the arm inductor dependent

on the capacitor voltage. In the low voltage section, the error between the theoretical value and the measured value is 10% or less. In the high voltage section, the error is increased to the maximum value of 11.8%. Whereas theoretical values increase linearly, measured values have non-linear characteristic. Besides, in the high voltage section, measured values are larger than theoretical values. This is caused by the decrease of the inductance due to the characteristic of the core. In general, the permeability of the core changes according to the core temperature. In the experiment, the

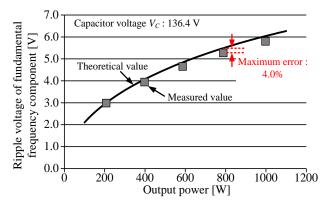


Fig. 17. Comparison result of theoretical values and measured values of fundamental frequency component in ripple voltage.

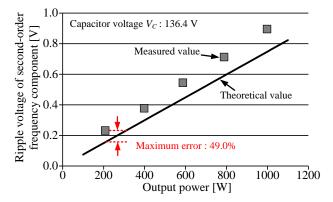


Fig. 18. Comparison result of theoretical values and measured values of second-order frequency component in ripple voltage.

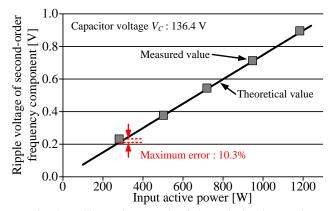


Fig. 19. Comparison result of theoretical values and measured values of second-order frequency component based on input active power.

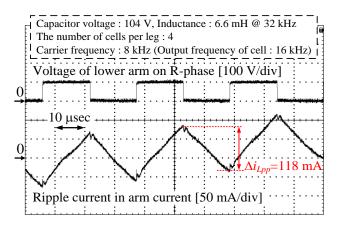


Fig. 20. Waveforms of lower arm voltage in R-phase and arm current.

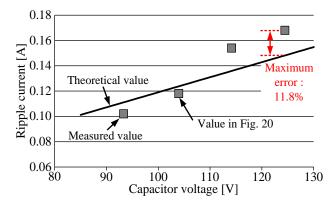


Fig. 21. Comparison result of theoretical values and measured values of ripple current in arm inductor dependent on capacitor voltage.

magnetic flux increases due to the increase of the capacitor voltage, which increases the iron loss of the core. As a result, the core temperature becomes higher at the high voltage section. Thus, the inductance decreases due to the decrease of the permeability when the core temperature raises.

7.4 Verifications theoretical formulae for of semiconductor losses In this section, the verification result for the theoretical formula of the semiconductor loss is shown. In the experiment, semiconductor losses, inductor losses and the no-load loss are considered. The no-load loss is measured when the MMC operates in state where the converter does not connects to the load. In general converters, the switching device has the parasitic capacitor and the current flows between the parasitic capacitor and the switching device when the switching device turns on. In this state, the measured input power is defined as the no-load loss. Next, the input power, the output power and the inductor loss are measured same time when the MMC operates in state where the converter connects to the load. By subtracting the output power, the inductor loss and the no-load loss from the input power, the semiconductor loss is obtained.

Table II shows the circuit parameters and the loss parameters in the verification for formulae of semiconductor losses. The loss parameters relating to the conduction loss are obtained from the datasheet of the used device, whereas the loss parameters relating to the switching loss and the recovery loss are obtained from the measured values in the switching test. Fig. 22 shows the comparison result of measured values and theoretical values. The theoretical value is defined as the total value of the conduction loss, the switching loss and the recovery loss in all cells. The maximum error is 3.4%. On the other hand, in all range, measured values are larger than theoretical values. The reason of this error is the loss in the equivalent series resistance (ESR) of the capacitor and the wiring loss which is not considered in the measurement. Thus, the semiconductor loss which is measured in the experiment includes the above losses which are not considered. As a result, measured values are larger than theoretical values. Besides, the error between the measured value and the theoretical value increases with the increase of the output power. This reason is that both the loss in the capacitor and the wiring loss increase with the increase of the output power because the ripple current of the capacitor and the arm current increases.

On the other hand, the switching device has the tolerance in the loss characteristic. This tolerance may affect the errors between calculated and measured losses. However, the MMC consists of many switching devices. As a result, the effect of the difference between the nominal value and the practical value of each switching device is small for overall system by averaging tolerance of the switching device. In addition, the relationship between the input power factor and the semiconductor loss is not changed in principle. Thus, it is possible to design the heat sink as same as general power converters after considering the worst case or the margin even when the tolerance in the loss characteristic exists.

Fig. 23 shows the breakdown of the losses in the MMC. The noload loss is constant against the change of the output power. On the other hand, the semiconductor loss and the inductor loss increase with the increase of the output power because the arm current increases. From Fig. 23, it is understood that the semiconductor loss is the majority of the overall loss. Hence, the semiconductor loss should be decreased by the design to achieve the high efficiency. One of methods to reduce the semiconductor loss is to decrease the arm current by raising the MMC output voltage because the semiconductor loss varies according to the arm current drastically.

#### 8. Conclusion

This paper presented the theoretical formula focused on the number of cells and the output DC voltage for the circuit parameter design in the H-bridge cell type Modular Multilevel Converter (MMC) in order to show the design guideline. Moreover, the worst case for each component design was also clarified as following;

(i) As the worst case in the cell capacitor design, the ripple component was maximum when the input power factor was 1.0. In particular, it was necessary to design the rated ripple current in this point when the electrolytic capacitor was applied.

(ii) As the worst case in the heat sink design, the semiconductor loss was maximum when the input power factor was 1.0.

(iii) As the worst case in the arm inductor design, the ripple current was maximum when the duty in each step of the cell total output voltage was 0.5.

In addition, theoretical formulae were verified in the miniature model of the MMC. As a result, the following results were obtained.

(a) As the verification of the capacitor ripple voltage, the measurement resulted in the maximum error of 4.0% between theoretical values and measured values. Because the ripple voltage was caused by the ripple current, it is possible to calculate exactly the ripple current of the electrolytic capacitor with the formula.

(b) As the verification of the ripple current in the arm inductor,

Table II. Circuit parameters and loss parameters for verification

| T (1° L) E                             | 200 1/ | TTI 1 C 11   | 4.4    |  |
|--|--------|--|--------|--|
| Input line voltage E                   | 200 V  | The number of cells n  | 4 /leg |  |
| Capacitor voltage $V_C$                | 135 V  | Load resistance R  | 5.3 Ω  |  |
| Carrier frequency $f_C$                | 8 kHz  |  |        |  |
| Output power $P_O$                     |        | 200 - 1000 W   |        |  |
| Switching device                       |        | FGW30N60VD   |        |  |
| Drop voltage of switch $V_{0_{SW}}$    |        | 0.74 V @ <i>Tj</i> =25 °C                                    |        |  |
| Resistance of switch $R_{SW}$          |        | 0.0536 Ω @ <i>Tj</i> =25 °C                                  |        |  |
| Drop voltage of FWD $V_{0_FWD}$        |        | 0.8 V @ <i>Tj</i> =25 °C                                     |        |  |
| Resistance of FWD R <sub>FWD</sub>     |        | 0.0492 Ω @ <i>Tj</i> =25 °C                                  |        |  |
| Turn-on energy of switch won           |        | 75.46 $\mu$ J@V <sub>dcd</sub> =135 V I <sub>md</sub> =6.7 A |        |  |
| Turn-off energy of switch woff         |        | 53.98 $\mu$ J@V <sub>dcd</sub> =135 V I <sub>md</sub> =8.3A  |        |  |
| Recovery energy of FWD w <sub>rr</sub> |        | $6.21 \ \mu J @V_{dcd}{=}135 \ V \ I_{md}{=}0.6 \ A$         |        |  |

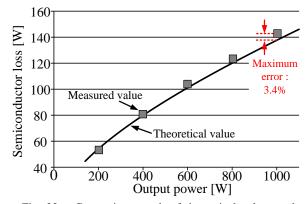


Fig. 22. Comparison result of theoretical values and measured values of semiconductor loss.

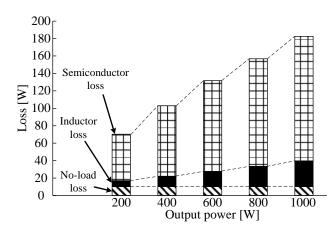


Fig. 23. Breakdown of losses in MMC. The inductor loss and the semiconductor loss increase with the increase of the output power because the arm current increases.

the measurement resulted in the maximum error of 11.8% between theoretical values and measured values. The error was caused by the change of the core characteristic.

(c) As the verification for the formulae of semiconductor losses, the measurement resulted in the maximum error of 3.4% between the theoretical value and the measured value. Hence, it is possible to calculate the semiconductor loss for design of the heat sink.

It is expected that these results promote the discussion of the design focused on the number of cells and the MMC output voltage.

#### References

- (1) "Microgrids", IEEE Power Energy Mag., Vol. 6, No. 3, pp. 26-94 (2008)
- (2) H. Kakigano, Y. Miura, T. Ise: "Low-Voltage Bipolar-Type DC Microgrid for Super High Quality Distribution", IEEE Trans. on Power Electronics, Vol. 25, No. 12, pp. 3066-3075 (2010)
- (3) D. Salomonsson, L. Söder, A. Sannino: "Protection of Low-Voltage DC Microgrids", IEEE Trans. on Power Delivery, Vol. 24, No. 3, pp. 1045-1053 (2010)
- (4) [Online] http://new.abb.com/high-voltage/capacitors/mv/capacitorbanks/metal-enclosed-capacitor-banks-abbacus
- (5) [Online] [Japanese] http://www.daihen.co.jp/products/electric/pdf/receiving/ receiving01.pdf
- (6) [Online] [Japanese] https://ntec.nito.co.jp/prd/pdf/N2015/N15S1420.pdf
- (7) [Online] [Japanese] http://www.daihen.co.jp/products/electric/pdf/trans/ trans01.pdf
- (8) [Online] [Japanese] http://dl.mitsubishielectric.co.jp/dl/fa/document/catalog/ capa/k-k06-8-c3698/K-K06-8-C3698-N.pdf
- (9) N. Hatti, Y. Kondo, and H. Akagi, "Five-Level Diode-Clamped PWM Converters Connected Back-to-Back for Motor Drives," *IEEE Trans. on Industrial Applications*, vol. 44, no. 4, pp. 1268–1276, 2008.
- (10) T. Nakanishi, J. Itoh, "Evaluation for Overall Volume of Capacitor and Heatsink in Step-down Rectifier using Modular Multilevel Converter", European Conference on Power Electronics and Applications 2015 (EPE'15), No. 584 (2015)
- (11) M. Glinka, R. Marquardt: "A New AC/AC Multilevel Converter family", IEEE Trans. on Industrial Electronics, Vol. 52, No. 3, pp. 662-669 (2005)
- (12) M. Hagiwara, H. Akagi: "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters", IEEE Trans. on Power Electronics, Vol. 24, No. 7, pp. 1737-1746 (2009)
- (13) M. Vasiladiotis, S Kenzelmann, N. Cherix, A. Rufer: "Power and DC Link Voltage Control Considerations for Indirect AC/AC Modular Multilevel Converters", European Conference on Power Electronics and Applications 2011. (EPE'11), (2011)
- (14) N. Thitichaiworakorn, M. Hagiwara, H. Akagi: "Experimental Verification of a Modular Multilevel Cascade Inverter Based on Double-Star Bridge Cells", IEEE Trans. on Industry applications, Vol. 50, No. 1, pp. 509-519 (2014)
- (15) [Online] https://library.e.abb.com/public/13cdf35faf4c362f48257e0700331e b4/ACS 2000%20Product%20brochure\_low-res\_RevG.pdf
- (16) A. Hillers, J. Biela: "Optimal Design of the Modular Multilevel Converter for an Energy Storage System Based on Split Batteries", European Conference on Power Electronics and Applications 2013 (EPE'13), No. LS7b (2013)
- (17) J. E. Huber, J. W. Kolar: "Analysis and Design of Fixed Voltage Transfer Ratio DC/DC Converter Cells for Phase-Modular Solid-State Transformers", 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 5021-5029 (2015)
- (18) Y. Zhang, G. P. Adam, T.C. Lim, S. J. Finney, B. W. Williams: "Analysis and Experiment Validation of a Three-level Modular Multilevel Converters", International Conference on Power Electronics – ECCE Asia, No. WeE2-2 (2011)
- (19) H. Bärnklau, A. Gensior, S. Bernet: "Submodule Capacitor Dimensioning for Modular Multilevel Converters", IEEE Trans. on Industry Applications, Vol. 50, No. 3, pp. 1915-1923 (2014)
- (20) D. Gao, S. Jiang, F. Z. Peng: "Optimal Design of a Multilevel Modular Capacitor-Clamped DC–DC Converter", IEEE Trans. on Power Electronics, Vol. 28, No. 8, pp. 3816–3826 (2013)
- (21) A. Hillers, M. Stojadinovic, J. Biela: "Systematic Comparison of Modular Multilevel Converter Topologies for Battery Energy Storage Systems Based on Split Batteries", European Conference on Power Electronics and Applications 2015 (EPE'15), No. DS2g (2015)
- (22) S. P. Engel. R. W. De Doncker: "Control of the Modular Multi-Level Converter for minimized cell capacitance", European Conference on Power Electronics and Applications 2011 (EPE'11), No. LS1h (2011)
- (23) A. Escobar-Mejia, Y. Liu, J. C. Balda, K. George: "New Power Electronic Interface Combining dc Transmission, a Medium-Frequency Bus and an acac Converter to Integrate Deep-Sea Facilities with the ac Grid", 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 4335-4344, 2014.
- (24) [Online] http://www.egr.msu.edu/pelab/projects/TUPFC%20presentation\_ 2014.pdf
- (25) F. Z. Peng, Y. Liu, S. Yang, S. Zhang, D. Gunasekaran, and U. Karki, "Transformer-Less Unified Power-Flow Controller Using the Cascade Multilevel Inverter," *IEEE Trans. on Power Electronics*, vol. 31, no. 8, pp. 5461-5472, 2016.
- (26) Y. Xu, X. Xiao, Y. Xu, Y. Long, C. Yuan: "Detailed Design, Integration and Testing of Submodule for 1000V/85kVA Modular Multilevel Converter", 1st

International Future Energy Electronics Conference, pp. 460-464 (2013)

- (27) M. W. Cong, Y. Avenas, M. Miscevic, R. Mitova, J. P. Lavieville, P. Lasserre: "Thermal analysis of a submodule for modular multilevel converters", 2014 IEEE Applied Power Electronics Conference and Exposition (APEC), pp.2675-2681 (2014)
- (28) S. Rohner, S. Bernet, M. Hiller, R. Sommer: "Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters", IEEE Trans. on Industrial Electronics, Vol.57, No.8, pp. 2633-2642 (2010)
- (29) J. E. Huber, J. W. Kolar: "Optimum Number of Cascaded Cells for High-Power Medium-Voltage Multilevel Converters", 2013 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 359-366 (2013)
- (30) Y. Miura, K. Inubushi, M. Ito, T. Ise: "Multilevel Modular Matrix Converter for High Voltage Applications", Annual Conference of the IEEE Industrial Electronics Society (IECON'14), pp. 4690–4696 (2014)
- (31) H-C. Chen, P-H Wu, C-W, Wang, P-T. Cheng: "Voltage Balancing Control Based on Average Power Flow Management for the Delta-Connected Cascaded H-bridges Converter", 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2104-2111 (2015)
- (32) A. Marzoughi, R. Burgos, D. Boroyevich, Y. Xue: "Investigation and Design of Modular Multilevel Converter in AFE Mode with Minimized Passive Elements", 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 6770-6776 (2015)
- (33) S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, K. Hatua: "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters", IEEE Trans. on Industrial Application, Vol. 51, No. 4, pp. 3343–3360 (2015)
- (34) Y. Ohnuma, J. Itoh: "A Novel Single-Phase Buck PFC AC–DC Converter With Power Decoupling Capability Using an Active Buffer", IEEE Trans. on Industrial Application, Vol. 50, No. 3, pp. 1905–1914 (2014)
- (35) T. Nakanishi, J. Itoh: "Capacitor Volume Evaluation based on Ripple Current in Modular Multilevel Converter", 2015 International Conference on Power Electronics (ICPE), No. WeA1-5 (2015)
- (36) Y. Kashihara, J. Itoh: "Power Losses of Multilevel Converters in Terms of the Number of the Output Voltage Levels", 2014 International Power Electronics Conference (IPEC), No. 20A4-4, pp. 1943-1949 (2014)
- (37) B. Li, R. Yang, D. Xu, G. Wang, W. Wang, D. Xu: "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters", IEEE Trans. on Power Electronics, Vol. 30, No. 1, pp. 297-310 (2015)
- (38) H. N. Le, K. Orikawa, J. Itoh: "Clarification of Relationship between Current Ripple and Power Density in Bidirectional DC-DC Converter", 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1911-1918 (2016)

#### Toshiki Nakanishi



(Student member) received the B.S. degrees in electrical, electronics and information engineering from Nara National College of Technology (NNCT), in 2011. He received master degrees in Nagaoka University of Technology (NUT) in 2014. And he has been in doctoral course of NUT. He is the student member of IEEJ and IEEE. His main research interests include multilevel converters.

Jun-ichi Itoh



(Senior Member) received his M.S. and PhD degrees in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan in 1996 and 2000, respectively. From 1996 to 2004, he was with Fuji Electric Corporate Research and Development Ltd., Tokyo, Japan. Since 2004, He has been with Nagaoka University of Technology as an associate professor. He received the IEEJ Academic

Promotion Award (IEEJ Technical Development Award) in 2007 and the Isao Takahashi Power Electronics Award in 2010. His research interests include matrix converters, DC/DC converters, power factor correction techniques and motor drives. He is a senior member of the Institute of Electrical Engineers of Japan and the Society of Automotive Engineers of Japan.