Reduction of DC-link current harmonics for Three-phase VSI over Wide Power Factor Range using Single-Carrier-Comparison Discontinuous PWM

Koroku Nishizawa^{*}, Jun-ichi Itoh^{*}, Akihiro Odaka^{**}, Akio Toba^{**}, and Hidetoshi Umida^{**}
^{*}Nagaoka University of Technology
1603-1 Kamitomioka-cho, Nagaoka city Niigata, Japan Tel., Fax: +81 / (258) – 47.9533.
E-Mail: koroku_nishizawa@stn.nagaokaut.ac.jp, itoh@vos.nagaokaut.ac.jp
URL: http://itohserver01.nagaokaut.ac.jp/itohlab/jp/index.html
^{*}Fuji Electric Co., Ltd.
1 Fuji-cho, Hino city Tokyo, Japan Tel.: +81 / (42) – 583.6118. Fax: +81 / (42) – 586.9665.
E-Mail: odaka-akihiro@fujielectric.com, toba-akio@fujielectric.com, umida-hidetoshi@fujielectric.com
URL: http://www.fujielectric.co.jp/

Keywords

«DC-link current harmonics», «Three-phase voltage source inverter», «Discontinuous PWM»

Abstract

This paper proposes a novel discontinuous PWM (DPWM) in order to reduce dc-link current harmonics of a voltage source inverter (VSI) over wide load-power-factor range. This modulation method, which requires only one carrier, contributes to a lifetime extension of smoothing capacitors in a motor drive system. Furthermore, by realizing this modulation method with only one carrier, a high cost hardware such as a field-programmable gate array (FPGA) is not necessary. By adding an offset to voltage references of conventional DPWM, and shifting two unclamped voltage references in every half control period, the dc-link current harmonics are reduced even when load power factor changes. It is clarified by experiments that the proposed DPWM reduces the dc-link current harmonics by 18.4% at most at modulation index of 0.705 and load power factor of 0.819.

I. Introduction

Three-phase AC motors are widely used in both the industrial and household applications [1]-[7]. Recently, lifetime extension of AC motor drive systems has been actively researched [8]-[9].

Generally, electrolytic capacitors are used as a smoothing capacitor in dc-link of three-phase VSI. The smoothing capacitor absorbs inverter dc-link current harmonics, and eventually deteriorates as a result of exothermic reaction of its electrolyte. Therefore, the lifetime of the smoothing capacitor is the most critical issue for the lifetime extension of the whole motor drive system. In order to extend the lifetime of the smoothing capacitor, a method applying film capacitors instead of the electrolytic capacitor as the smoothing capacitor has been proposed [10]. However, this method makes the motor drive system bulkier because of low energy density of the film capacitors compared to the electrolytic capacitors.

On the other hand, it is also possible to extend the lifetime of the smoothing capacitor by reducing the dc-link current harmonics of VSI. Therefore, modulation methods of VSI, which reduce the dc-link current harmonics of VSI, have been also proposed [8]-[9], [11]. In [8]-[9], double carriers, which consist of an original triangular carrier and a second triangular carrier whose phase is opposite to the

first one, are used for the modulation as a double-carrier-comparison pulse width modulation (PWM). In particular, the dc-link current harmonics are reduced by minimizing the zero vector period by comparing only one voltage reference with the inverse triangular carrier and comparing the other voltage references with the original carrier. However, this method leads to a constraint of the digital hardware due to the generation of the inverse triangular carrier. Furthermore, when the load power factor becomes lower than 0.866, the dc-link current harmonics cannot be reduced by these methods.

As another approaches to minimize the dc-link current harmonics, a novel space vector PWM (SVPWM) has been proposed in [11]. In this SVPWM, the output voltage space vectors are selected in order that the zero vector period is shortened. Besides, by changing the output voltage space vectors according to polarities of output phase currents, the SVPWM in [11] can adapt to the variation of the load power factor. However, the employment of the proposed SVPWM also leads a constraint of the digital hardware because the SVPWM needs to not only compare the on-duties of the selected output voltage space vectors with single carrier but also decide the gating signals based on the carrier comparison results in order to realize the optimized combinations of the output voltage space vectors for the reduction of the dc-link current harmonics.

This paper proposes a novel carrier-comparison DPWM which uses only one carrier in order to reduce the switching-frequency-order dc-link current harmonics of VSI and eliminates the need of the complex digital hardware. In other words, the proposed DPWM can be simply implemented by the general-purpose micro-computer for power electronics. In order to use just only one carrier, two unclamped phase voltage references of the conventional DPWM are shifted in every half control period. This leads to a smaller fluctuation of the dc-link current around its average value, which reduces the dc-link current harmonics. Furthermore, by adding an offset to all voltage references of the DPWM in order to optimize the phase of clamped voltage reference and its clamped value, the dc-link current harmonics are reduced even when the load power factor varies.

This paper is organized as follows; first, the reduction method of the dc-link current harmonics by using the novel voltage references of the DPWM is introduced. Next, the mechanism to adapt the variation of the load power factor is explained. Finally, the effectiveness of the proposed DPWM is confirmed by simulation and experiment.

II. Proposed PWM method to reduce dc-link current harmonics of VSI

A. Conventional discontinuous PWM

Fig. 1 shows a three-phase VSI employed in the motor drive system. The three-phase VSI consists of three half bridges. If the semiconductor switching devices are assumed to be ideal, the conduction status of each half bridge can be represented by the binary switching functions as

$$s_{x} = \begin{cases} 1, & (S_{xp} : ON, S_{xn} : OFF) \\ 0, & (S_{xp} : OFF, S_{xn} : ON) \end{cases}, \quad (x = u, v, w)$$
(1).



Fig. 1. Three-phase two-level VSI employed in motor drive system.

Output phase currents of the VSI at steady state operating condition can be expressed as

$$\begin{cases}
i_{u} = I_{m} \cos(2\pi ft - \varphi) \\
i_{v} = I_{m} \cos\left(2\pi ft - \frac{2\pi}{3} - \varphi\right) \\
i_{w} = I_{m} \cos\left(2\pi ft + \frac{2\pi}{3} - \varphi\right)
\end{cases}$$
(2),

where, I_m is the maximum value of the output phase current, f is the fundamental frequency, and φ is the load power factor angle, i.e. the phase difference between the phase voltage and phase current, respectively.

Fig. 2 shows the normalized voltage references of the continuous PWM (CPWM) and DPWM and an offset for the DPWM at the modulation index of 0.8. These voltage references of the DPWM are obtained by adding the offset v_{offset}^* to the voltage references of the CPWM [12]. The voltage references of the CPWM and DPWM and the offset are expressed as

$$\begin{cases} v_{u,CPWM}^{*} = m \cdot \cos(2\pi ft) \\ v_{v,CPWM}^{*} = m \cdot \cos\left(2\pi ft - \frac{2\pi}{3}\right) \\ v_{w,CPWM}^{*} = m \cdot \cos\left(2\pi ft + \frac{2\pi}{3}\right) \end{cases}$$
(3),
$$v_{x,DPWM}^{*} = v_{x,CPWM}^{*} + v_{offset}^{*}, \quad (x = u, v, w)$$
(4),
$$v_{offset}^{*} = \begin{cases} 1 - |v_{max}| & \text{if } |v_{max}| \ge |v_{min}|, \\ -1 + |v_{min}| & \text{if } |v_{max}|, \\ 1 - 1 + |v_{min}| & \text{if } |v_{max}|, \end{cases}$$
(5),
$$\text{and } \begin{cases} v_{max} = \max[v_{u,CPWM}^{*}, v_{v,CPWM}^{*}, v_{w,CPWM}^{*}] \\ v_{min} = \min[v_{u,CPWM}^{*}, v_{v,CPWM}^{*}, v_{w,CPWM}^{*}] \end{cases}$$
(5),

where, *m* is the modulation index.



Fig. 2. Normalized voltage references of CPWM, conventional DPWM and offset at m = 0.8.

Fig. 3 shows the zoomed-in waveform of the dc-link current of VSI $i_{DC.in}$ and the switching functions $s_u \sim s_w$ with the conventional DPWM at the modulation index of 0.8, the phase angle of 50 degrees and the unity load power factor. The instantaneous value of the dc-link current of VSI is the superposition summation of the switched current pulses from each phase leg [13] and calculated as

$$i_{DC.in} = \sum_{x=u,v,w} (s_x \times i_x)$$
(6).

The shaded area in the instantaneous waveform of the dc-link current of VSI in Fig. 3 indicates the time integral of the difference between the instantaneous value and average value of the dc-link current of VSI. This difference is absorbed by the smoothing capacitor. Therefore, the shaded area in Fig. 3 expresses the instantaneous root-mean-square (RMS) value of the current flowing into the smoothing capacitor, which is calculated as

$$i_{C.RMS}(T_s) = \sqrt{i_{DC.in,RMS}^2(T_s) - \bar{i}_{DC.in}^2}$$
and
$$\begin{cases}
i_{DC.in,RMS}(T_s) = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{DC.in}^2 dt} \\
\bar{i}_{DC.in} = \frac{3}{4} m \cdot I_m \cos\varphi
\end{cases}$$
(7).

where, T_s is the control period, I_m is the maximum value of the output phase current of VSI and φ is the load power factor angle. It is obvious that the shaded area, expressing the dc-link current harmonics of VSI, becomes larger when the fluctuation of the dc-link current around its average value is large [14]. In the case of the conventional DPWM, the center of the gate pulses is the same as the center of the control period. As a result, the overlapping period of the gate pulses becomes the longest at any time. This leads to the large fluctuation of the dc-link current around its average value, i.e. the large dc-link current harmonics.

B. Proposed discontinuous PWM

The operations of the proposed DPWM change corresponding to the load power factor. At the unity load power factor, two unclamped voltage references of the conventional DPWM are shifted in every half control period to reduce the dc-link current harmonics. On the other hand, when the load power factor becomes low, first, three voltage references is added with an offset, then, two unclamped voltage references are shifted in half control period.



Fig. 3. Zoomed-in waveforms of dc-link current and switching functions with conventional DPWM at m = 0.8, $2\pi ft = 50$ deg., $\cos \varphi = 1$.

B-I. Operation at unity load power factor

Fig. 4 shows the zoomed-in waveform of the dc-link current of VSI and the switching functions with the proposed DPWM at the modulation index of 0.8, the phase angle of 50 degrees and the unity load power factor. In the proposed DPWM, the fluctuation of the dc-link current around its average value is reduced by displacing the center of the gate pulses. Note that the proposed voltage references are realized based on the premise that the voltage references can be updated at the positive peak and negative peak of the carrier by the general-purposed micro-computer for power electronics. In particular, the voltage references of the proposed DPWM for the reduction of the dc-link current harmonics are generated as follows:

- 1. Splitting the control period into "DOWN" and "UP" periods.
- 2. Shifting two voltage references, other than the clamped voltage reference of the DPWM, to reach 1 or -1 one after the other in these periods as
 - In "DOWN" period:

$$v_{a}^{*} = \begin{cases} 2v_{a,\text{DPWM}}^{*} - 1 & \text{if } v_{a,\text{DPWM}}^{*} \ge 0, \\ -1 & \text{if } v_{a,\text{DPWM}}^{*} \le 0, \end{cases}$$

$$v_{b}^{*} = \begin{cases} 1 & \text{if } v_{b,\text{DPWM}}^{*} \ge 0, \\ 2v_{b,\text{DPWM}}^{*} + 1 & \text{if } v_{b,\text{DPWM}}^{*} \le 0. \end{cases}$$

$$(8)$$

• In "UP" period:

where, *a* and *b* indicate phases whose the voltage references are not clamped, i.e. the *u* and *v* phases in Fig. 4 for example, $v_{a,DPWM}^*$ and $v_{b,DPWM}^*$ are the conventional voltage references, v_a^* and v_b^* are the shifted voltage references in the proposed DPWM.

Note that the average values of these shifted voltage references in the control period are as same as those of the conventional voltage references. With these shifted voltage references, the overlapping period of the switching functions is shortened. Consequently, this leads the reduction of the dc-link current harmonics.



Fig. 4. Zoomed-in waveforms of dc-link current and switching functions with proposed DPWM at m = 0.8, $2\pi ft = 50$ deg., $\cos \varphi = 1$.

However, note that the reduction effect on the dc-link current harmonics of the proposed DPWM depends on the load power factor because the instantaneous value of the dc-link current of VSI depends on the output phase currents. Therefore, it is necessary to deal with the variation of the load power factor in order to reduce the dc-link current harmonics of VSI over wide power factor range, which is a typical requirement of the motor drive system.

B-II. Operation over wider load-power-factor range

Table I shows the definitions of the sectors which are determined by the combination of the detected output phase currents of VSI. These sectors (A~F) are necessary to recognize the conditions of the output phase currents.

Fig. 5 shows the conventional and shifted voltage references at the modulation index of 0.8 and the load power factor of 0.966 ($\varphi = 15$ deg.). In order to employ the proposed DPWM to any condition of the load power factor, first, three conventional voltage references $v_{x,DPWM}^*$ (x = u, v, w) are added with the offset $v_{offset.2}^*$ to obtain the voltage references with the offset $v_{x,DPWM}^*$. Note that the offset value $v_{offset.2}^*$ is optimized according to the conditions of the output phase currents and the clamped phase. In the case of sector B, for example, where i_u and i_v are positive and i_w is negative, the switching function of w phase must be 0 to obtain the minimum fluctuation of the dc-link current around its average value. If the switching function of w phase becomes 1 during sector B, the instantaneous value of the dc-link current around its average value, i.e. the large dc-link current harmonics. Next, two unclamped phase voltage references are shifted in every half control period according to (8)-(9), which results in the voltage references v_x^* of the proposed DPWM.

TABLE I				
SECTOR DEFINITIONS OF PROPOSED DPWM.				
Sector	Current polarity (P: Positive, N: Negative)			Optimized clamped value
	i_u	i_v	i_w	K_{OCV}
А	Р	Ν	Ν	1
В	Р	Р	Ν	-1
С	Ν	Р	Ν	1
D	Ν	Р	Р	-1
Е	Ν	Ν	Р	1
F	Р	Ν	Р	-1



Fig. 5. Proposed voltage references at m = 0.8, $\cos \varphi = 0.966$ ($\varphi = 15$ deg.). $v_{x,pDPWM}^*$ are generated by adding an offset $v_{offset.2}^*$ to $v_{x,DPWM}^*$ in order to keep the clamped period of the voltage reference at each proposed sector. The voltage references of the proposed DPWM v_x^* are finally generated by shifting two unclamped voltage references of $v_{x,PDPWM}^*$ in every half control period.



Fig. 6. Proposed voltage references at m = 0.8, $\cos \varphi = 0.707$ ($\varphi = 45$ deg.). In gray periods, the voltage references of the conventional DPWM are applied to avoid the overmodulation operation due to adding the $v^*_{offset.2}$.

In the proposed DPWM, by adding the offset to all voltage references of the conventional DPWM, the phase of the clamped voltage reference and its clamped value are adjusted optimally for the reduction of the dc-link current harmonics of VSI at each proposed sector. The voltage references $v_{x,\text{PDPWM}}^*$ of the proposed DPWM and the offset $v_{offset.2}^*$ adding to the conventional voltage references $v_{x,\text{DPWM}}^*$ is calculated as

$$v_{x,\text{PDPWM}}^{*} = v_{x,\text{DPWM}}^{*} + v_{offset2}^{*}, \quad (x = u, v, w),$$

and $v_{offset2}^{*} = \begin{cases} K_{OCV} - v_{u,\text{PWM}}^{*} & \text{if sector} = A, D, \\ K_{OCV} - v_{v,\text{PWM}}^{*} & \text{if sector} = B, E, \\ K_{OCV} - v_{w,\text{PWM}}^{*} & \text{if sector} = C, F. \end{cases}$ (10),

where, K_{OCV} is the optimized clamped value of the voltage reference at each proposed sector, as shown in table I.

Fig. 6 shows the proposed voltage references at the load power factor of 0.707 ($\varphi = 45$ deg.). When the load power factor is lower than 0.866 ($\varphi < 30$ deg.), the periods when the absolute values of the proposed voltage references $v_{x,PDPWM}^*$ becomes more than 1 due to adding the offset $v_{affset.2}^*$ at each sector. Therefore, the voltage references $v_{x,DPWM}^*$ of the conventional DPWM are applied in these periods as shown in the shaded areas in Fig. 6, in order to avoid the overmodulation operation. Accordingly, the phase of the clamped voltage reference is not the optimized value for the reduction of the dc-link current harmonics in these periods. Thus, the shifting of two unclamped voltage references in every half control period are not performed in these periods.

III. Simulation and experimental results

The performances of the conventional and proposed DPWM are investigated by simulation and experiment. The switching frequency of VSI is 10 kHz. In the experiment, a three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.), the rated power of which is 3.7 kW, is used as a test motor. The load power factor is varied from 0.259 to 0.819, in the case of driving mode, by controlling the torque of a load motor.

Fig. 7 shows the *u*-phase voltage reference, the measured line voltage, the dc-link current and *u*-phase output line current of VSI with each modulation method at the modulation index of 0.705 and the load power factor of 0.819. When the load power factor is 0.819, the applying interval of the proposed DPWM is long and two unclamped voltage references are shifted in half control period as shown in Fig. 7(b). It is confirmed that the width of the step change in the dc-link current of VSI is reduced by applying the proposed DPWM. On the other hand, the switching-frequency-order harmonic components of the output line voltage are worsened by the proposed DPWM as it could be predicted since an instantaneous voltage error during the control period is higher with the gate pulses of the proposed DPWM than those with the conventional DPWM.

Fig. 8 shows the harmonic components of the dc-link current of VSI under the same conditions as Fig. 7. The value of 100% at the vertical axis means the maximum value of the output phase current. By applying the proposed DPWM, the switching-frequency-order harmonic components of the dc-link current is reduced by 5.49%.

Fig. 9 shows the simulation and experimental results of the dc-link current harmonics with each modulation method when the modulation index and the load power factor is varied respectively. Note that the dc-link current harmonics are evaluated as $I_{DC.in(p.u.)}$, which is the RMS value of the dc-link current ($I_{DC.in.RMS}$) normalized by the maximum value of the output current (I_m) of VSI.

$$I_{DC.in(p.u.)} = \frac{I_{DC.in.RMS}}{I_m} = \frac{1}{I_m} \sqrt{\sum_{k=1}^{\infty} \left(\frac{1}{\sqrt{2}} i_{DC.in.k}\right)^2}$$
(11),

where, k is the harmonic order and $i_{DC.in.k}$ is the k-order component of the dc-link current harmonics. The fundamental component of the dc-link current harmonics is 50 Hz at rated load. The harmonic



Fig. 7. *u*-phase voltage reference, line voltage, dc-link current and *u*-phase output line current of VSI at m = 0.705 and $\cos \varphi = 0.819$.



Fig. 8. Harmonic components on dc-link current of VSI at m = 0.705 and $\cos \varphi = 0.819$ (under same conditions of Fig. 7). The fundamental frequency is 30 Hz. By the employment of the proposed DPWM, the switching-frequency-order harmonic component is reduced by 5.5%.

components of the dc-link current up to 20^{th} -order of the switching frequency are considered in this evaluation because the switching frequency harmonic components of the dc-link current with the conventional and proposed DPWM above 20^{th} -order are small and comparable as shown in Fig. 8. The dc-link current harmonics are reduced over entire range of the modulation index and the load power factor by applying the proposed DPWM. At the load power factor of 0.819, i.e. the high load power factor, the value of $I_{DC.in(p.u.)}$ is reduced by 18.4% at most by applying the proposed DPWM compared to that of the conventional DPWM. It is also confirmed that as the load power factor becomes lower, the dc-link current-harmonic-reduction effect of the proposed DPWM decreases because the applying interval of the proposed DPWM is short as shown in Fig. 6. However, when the load power factor is low, the dc-link current harmonics are also low. On the other words, the large dc-link current harmonics in the case of the high load power factor which can be drastically reduced by applying the proposed DPWM should be focused.

Fig. 10 shows the total harmonic distortion (THD) of the *u*-phase output line current at the load power factor of 0.819. The harmonic components of the *u*-phase output line current up to 40th-order of the fundamental frequency are considered in this evaluation. Although the proposed DPWM reduces the dc-link current harmonics, it also worsens the output voltage harmonics as a trade-off as shown in Fig. 7. However, the worsened components by the proposed DPWM is the switching-frequency-order harmonic components. This means that the impacts of the employment of the proposed DPWM on the low-order harmonic components of the output line voltage and phase current is low. Therefore, the load current qualities of the conventional and proposed DPWM are comparable.



Fig. 9. Simulation and experimental results of dc-link current harmonics with each modulation method when modulation index and load power factor are varied respectively.



Fig. 10. Measured total harmonic distortion of *u*-phase output line current with each modulation method at $\cos \varphi = 0.819$. The switching frequency is 10 kHz.

IV. Conclusion

This paper proposed the novel DPWM to reduce the dc-link current harmonics of VSI over entire load power factor range. This modulation method, which required only one carrier, contributed to the long lifetime of the smoothing capacitor in the motor drive system. By realizing this modulation method with only one carrier, high cost hardware such as FPGA was not necessary. The dc-link current harmonics were reduced by adding an offset to the all voltage references of the conventional DPWM, and shifting two unclamped voltage references in every half control period. These optimized the phase of the clamped voltage reference and its clamped value for the reduction of the dc-link current harmonics of VSI even when the load power factor varied.

The effectiveness of the proposed DPWM was confirmed by the simulation and experiment. These results confirmed that the dc-link current harmonics were reduced by 18.4% at most at the load power factor of 0.819 by applying the proposed DPWM. Moreover, it was also confirmed that the dc-link current harmonics were reduced over entire range of the load power factor.

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