Current THD Reduction for High-Power-Density LCL-Filter-Based Grid-Tied Inverter Operated in Discontinuous Current Mode

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Keywords

«Single-phase grid-tied inverter», «Continuous current mode», «Discontinuous current mode», «Disturbance compensation», «Nonlinearity compensation»

Abstract

This paper proposes a discontinuous current mode (DCM) feedback current control for a single-phase grid-tied inverter in order to minimize a LCL filter without worsening total harmonic distortion (THD) of a grid current. In DCM, there are two nonlinearities occurring in the transfer functions; the first nonlinearity occurs in the duty-ratio-to-current transfer function which worsens the current command response, whereas the second nonlinearity occurs in the disturbance-to-current transfer function which reduces the disturbance effect. In the proposed DCM current control, the first nonlinearity is compensated by utilizing the duty ratio at the previous calculation period in order to achieve the same control performance of the current command response as in continuous current mode. Meanwhile, the second nonlinearity is utilized in order to reduce the disturbance effect when the LCL filter with a small impedance is applied. Furthermore, a design procedure of the LCL filter is introduced under the condition that the impedance of the LCL filter can be minimized without worsening the grid current THD by applying the proposed DCM control. A 1-kW 100-kHz inverter with several LCL filters of different impedances (3.0%, 0.6% and 0.04%) is constructed in order to confirm the operation of the proposed DCM current control. As a result, the grid current THD is reduced from 8.5% to 3.7% at rated load. Furthermore, the inductor volume is reduced by 77.0%, whereas the converter loss is reduced by 17.1%.

I. Introduction

Grid-tied inverters are used in order to connect photovoltaic (PV) cells to a single-phase ac grid. A filter is required between the inverter and the grid for reducing harmonics of the inverter output current. LCL filters have been commonly used in grid-tied inverters because they can achieve the size reduction by the use of small values of inductors and capacitors comparing to the L filter and LC filter [1]-[3]. The high attenuation of the LCL filter allows the design of the high cutoff frequency in the filter to meet harmonic constraints as defined by standards such as IEEE-519-1992 [4]. However, the small impedance of the LCL filter highly increases the disturbance gain of the conventional PI-controller-based continuous current mode (CCM) feedback current control. In order to overcome this problem, a disturbance observer which is designed based on CCM is utilized. This disturbance observer estimates the disturbances and eliminates them from the current feedback control. However, this method requires high speed controllers in order to estimate the rapidly-changing disturbances, e.g. the dead-time error voltage [5].

On the other hand, the effects of the disturbances can be reduced by discontinuous current mode (DCM). In particular, a DCM nonlinearity occurs in the disturbance-to-current transfer function, which results in the natural decrease in the disturbance gain. However, another nonlinearity occurs in the duty--to-current transfer function, which worsens the current command response [6]-[7]. In past few years,

many researches focusing on the control of DCM have been reported to solve this problem [8]-[13]. However, in those control methods, the DCM nonlinearity compensation method becomes circuit-parameter-dependent. In the PV application, the system is usually required to deal with the severe change of the ambient environment, where the circuit condition such as the operation temperature varies frequently. This leads to the instability of the circuit-parameter-dependent control.

This paper proposes a circuit-parameter-independent DCM current control. The original idea is that the nonlinearity compensation in the DCM current control is constructed by utilizing the duty ratio at the previous calculation period instead of using the circuit parameter, whereas the DCM nonlinearity occurring in the disturbance-to-current transfer function is used to reduce the disturbance effect, i.e. the reduction of the current distortion. This paper is organized as follows; first two DCM nonlinearities which occur in the current command response and the disturbance response are investigated. Then, the compensation for the DCM nonlinearity in the current command response is proposed and the mechanism to utilize the DCM nonlinearity in the disturbance response to reduce the current distortion is explained. After that, the volume evaluation of the LCL filter is conducted. Finally, the effectiveness of the proposed DCM feedback current control is confirmed experimentally.

II. Proposed DCM Current-Feedback Control

Fig. 1 indicates the circuit configuration of the single-phase grid-tied inverter. In this paper, a single-phase H-bridge inverter is applied due to its simplicity. The LCL filter connects the inverter to the grid for smoothing the inverter output current i_{out}. Note that the grid has its own intrinsic inductor L_g, the value is different depending on the type of the grid [3]-[4].

Fig. 2 indicates the equivalent circuit of the single-phase grid-tied inverter when the grid voltage is positive. The grid-side inductors L_g, L_f, and the filter capacitor C_f are omitted due to the simplification. Note that the grid-tied inverter is operated in bipolar modulation.

Fig. 3 depicts the inductor current waveform in DCM, where D_1, D_2 and D_3 denote the duty ratios of the first, the second and the zero-current interval. The equation based on the average model of the inverter shown in Fig. 5 is given by (1) [6]-[7],

$$V_L = D_1(V_{dc} - V_g) - D_2(V_{dc} + V_g) \tag{1}$$

where V_L is the average inductor voltage, V_{dc} is the DC-link voltage and V_g is the grid voltage. The average current i_{avg} and the current peak i_{peak}, which are shown in Fig. 3 are expressed as,

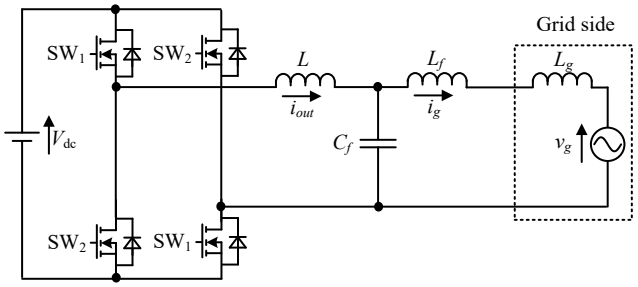
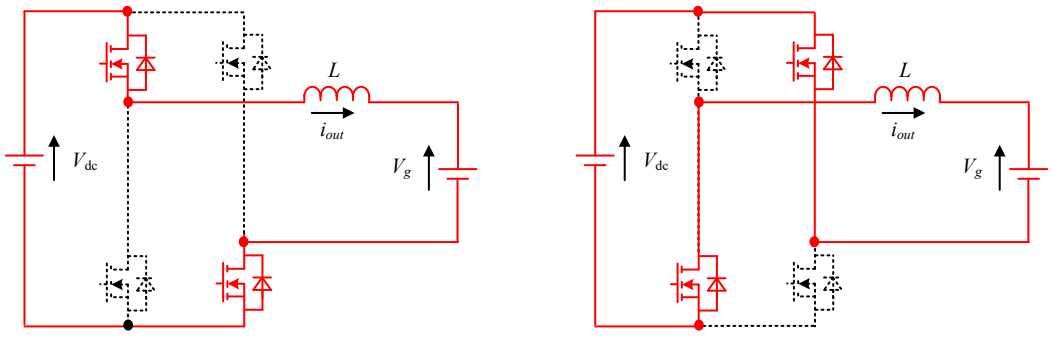


Fig. 1. Single-phase H-bridge grid-tied inverter with LCL filter. A single-phase H-bridge inverter is applied due to its simplicity, which is important for stability analysis and reliability design.



(a) Charging of inductor (b) Discharge of inductor

Fig. 2. Equivalent circuit of inverter when grid voltage is positive. The bipolar modulation is applied to reduce common-mode current.

$$i_{avg} = \frac{i_{peak}}{2}(D_1 + D_2) \tag{2}$$

$$i_{peak} = \frac{V_{dc} - V_g}{L} D_1 T_{sw} \tag{3}$$

where T_{sw} is the switching period. Substituting (3) into (2) and solving the equation for the duty ratio D_2. The duty ratio D_2 is expressed by (4),

$$D_2 = \frac{2Li_{avg}}{D_1 T_{sw}(V_{dc} - V_{ac})} - D_1 \tag{4}$$

Substituting (4) into (1) in order to remove the duty ratio D_2 and represent (1) as a function of only the duty ratio D_1, then (5) is obtained [6]-[7].

$$V_L = V_{dc}(2D_1 - 1) - V_g + (V_{dc} + V_g)\left\{1 - \frac{2Li_{avg}}{(V_{dc} - V_g)D_1 T_{sw}}\right\} \tag{5}$$

Then, the inverter circuit model in DCM is establish based on (5).

Fig. 4 illustrates the circuit model of the inverter operating in DCM which is based on (5). In CCM, the dash line part does not exist, because the average current i_{avg} equals to the half current peak $i_{peak}/2$. On the other words, this makes the zero-current interval D_3T_{sw} shown in Fig. 3 become zero. However, in DCM, the zero-current interval introduces the nonlinearities into the DCM transfer function. The design of the compensation part for the DCM nonlinearity is explained as follows. First, the circuit model in Fig. 4 is linearized at steady state.

Fig. 5 depicts the linearized circuit model. The duty-ratio-to-current transfer functions in CCM and DCM are derived from Fig. 5, and expressed as in (6) and (7) respectively,

$$G_{i\_CCM}(s) = \frac{\Delta i_{avg}(s)}{\Delta D_1(s)} = \frac{2V_{dc\_s}}{sL} \tag{6}$$

$$G_{i\_DCM}(s) = \frac{\Delta i_{avg}(s)}{\Delta D_1(s)} = \frac{4V_{dc\_s}}{sL + \dfrac{2L(V_{dc\_s} + V_{g\_s})}{D_{1\_s}T_{sw}(V_{dc\_s} - V_{g\_s})}} \tag{7}$$

Fig. 6 depicts the gain of the duty-ratio-to-current transfer function in CCM and DCM under different conditions of the steady-state duty ratio D_{1_s} and the grid voltage V_{g_s} based on (6)-(7). In most cases, the frequency corresponding to the pole of G_{i_DCM} is certainly much higher than the cutoff frequency of

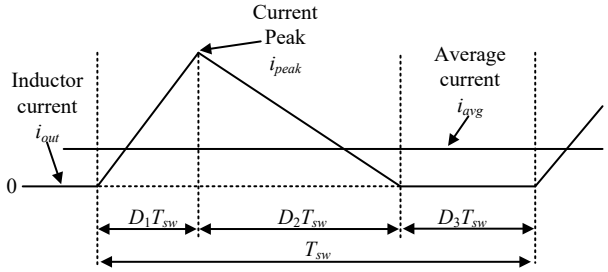


Fig. 3. Inductor current waveform in DCM. The zero-current interval introduces nonlinearities into the DCM operation.

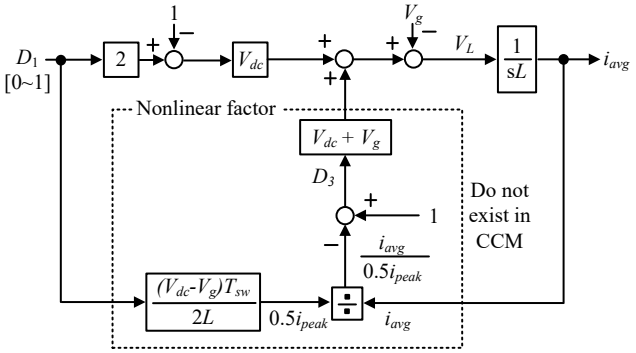


Fig. 4. Circuit model of inverter operated in DCM. In DCM, the current control depends greatly on the current value, i.e. the nonlinearities occurring in the duty-ratio-to-current transfer function and the disturbance-to-current transfer function.

the current control loop f_n. Consequently, the open loop gain in DCM is much lower than in CCM. This worsens the current response in DCM if the same PI controller as in CCM is employed in DCM. Therefore, the output of PI controller is necessary to be compensated when the circuit is operated in DCM in order to achieve the same current command response as in CCM. In order to eliminate the dash line part in Fig. 5, in the control system, the value of D_{1_s} is approximated as the duty ratio of SW_1 at the previous calculation period $D_{1[n\text{-}1]}$. As a result, the circuit model is necessary to be analyzed in the discrete model.

Fig. 7 depicts the discretized circuit model. In order to compensate the DCM nonlinearity at the output of the PI controller designed in CCM, the dash line part in Fig. 7 is necessary to be set as 1 when the circuit is operated in DCM. Therefore, in the control system, the inverse part of the dash line part in Fig. 7 is multiplied at the output of the PI controller in order to compensate for the DCM nonlinearity.

Fig. 8 illustrates the conventional CCM current control, and the proposed DCM current control. In CCM, the disturbance effect increases 10 times when L is reduced from 1 p.u. to 0.1 p.u., because the gain of the disturbance response inversely proportional to L [5]. On the other hand, in the proposed DCM current control, the PI controller is designed as same as in CCM, whereas the DCM nonlinearity compensation is calculated by using the duty ratio of SW_1 at the previous calculation period $D_{1[n\text{-}1]}$. The estimation of the duty ratio at steady state D_{1_s} as the duty ratio of SW_1 at the previous calculation period $D_{1[n\text{-}1]}$ provides the control system circuit-parameter-independence, and short computation time. The switches SW_1 and SW_2 are controlled separately depending on the polarity of the duty ratio D_1. The synchronous switching of SW_1 and SW_2 can be employed in order to further improve the inverter efficiency [7], [10]. Note that the absolute value of the grid voltage is calculated in order to use the same DCM nonlinearity compensation when the grid voltage becomes negative.

Fig. 9 shows the gain of the disturbance response in CCM and DCM under different conditions of the steady-state duty-ratio D_{1_s}. In CCM, the minimization of the inductor value L worsens the disturbance response. In general, when the typical dead-time error voltage compensation is applied with the high L, the current distortion is effectively reduced. However, when L is greatly reduced, only a small mismatch between the estimated and actual dead-time error voltage ($v_{deadtime\_est}$ and $v_{deadtime}$) which is caused by such as the current detection delay, results in a high current distortion due to the greatly-

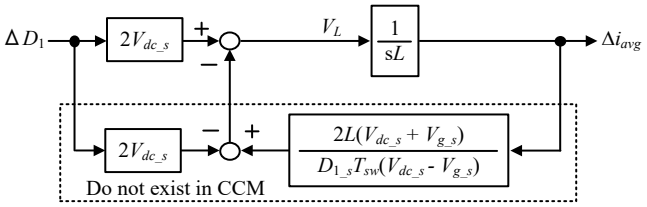


Fig. 5. Linearized circuit model. By estimating the duty ratio at steady states, the DCM nonlinearity can be compensated. Consequently, the controller in DCM can be designed as same as in the CCM operation, which has been researched and analyzed thoroughly.

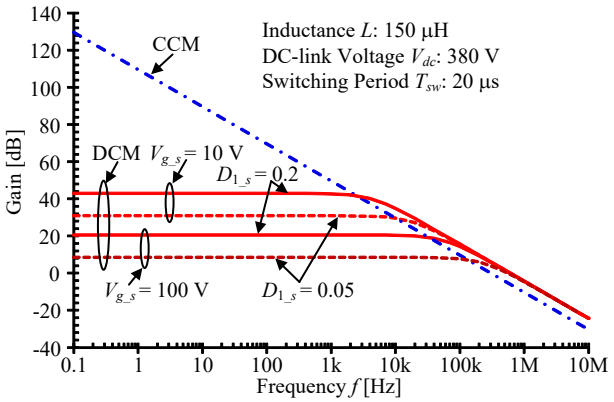


Fig. 6. Bode diagram of duty-ratio-to-current transfer function for CCM and DCM. The zero-current interval in DCM introduces the first nonlinearity into the duty-ratio-to-current transfer function, which greatly worsens the DCM current command response.

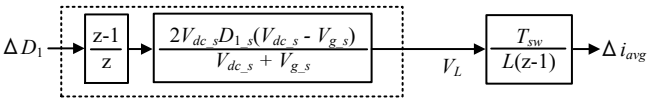
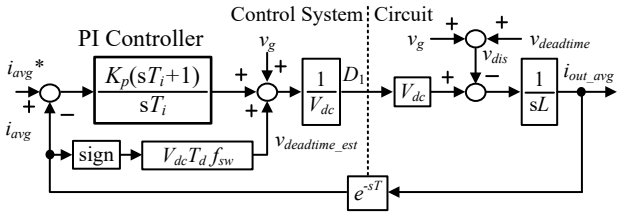
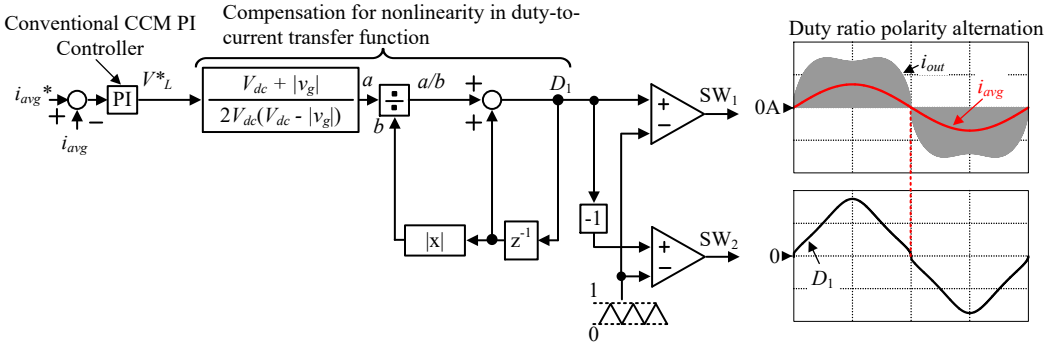


Fig. 7. Discretized circuit model. The original idea of the DCM nonlinearity compensation is to estimate the duty ratio at steady states by the duty ratio at the previous calculation. Consequently, the inductance is not required in the DCM nonlinearity compensation.



(a) Conventional CCM feedback current control block with typical dead-time error voltage compensation. When the inductors is minimized by reducing the inductance, the inverter become more vulnerable to the disturbances, i.e. the increase in the disturbance gain.



(b) Proposed DCM current control for inverter. In DCM, the switches SW_1 and SW_2 are controlled separately depending on the polarity of the duty ratio, i.e. the polarity of the grid voltage in unity power factor.

Fig. 8. Conventional CCM current control and proposed DCM current control for inverter.

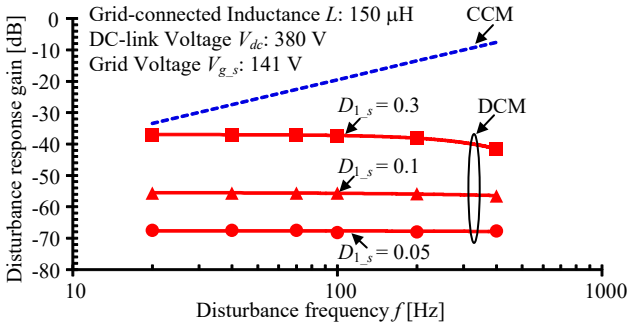


Fig. 9. Disturbance response in CCM and DCM. The DCM nonlinearity in the disturbance-to-current transfer function makes the DCM current more resistant to the disturbance than the CCM current. Therefore, the LCL filter can be further minimized in DCM.

increasing gain of the disturbance response. On the other hand, in DCM when the steady-state duty-ratio D_{1_s} becomes smaller, the disturbance response gain in DCM decreases. The reason is that the proposed DCM nonlinearity compensation for the current command response does not compensate for the DCM nonlinearity in the disturbance response. Consequently, the disturbance response depends on the steady-state duty-ratio D_{1_s}. Therefore, by utilizing this nonlinearity characteristic in which the disturbance gain decreases greatly with the small steady-state duty-ratio D_{1_s}, i.e. the interval near the current zero-crossing point or the light load, the current distortion can be reduced.

III. LCL Filter Design Procedure

Fig. 10 indicates the LCL filter design algorithm. The following parameters are needed for the filter design: the rated active power P_n, the dc-link voltage V_{dc}, the single-phase grid voltage v_g, and the grid frequency f_g. First, the base impedance of the inverter is defined by (8), [1]

$$Z_b = \frac{v_g^2}{P_n} \tag{8}$$

Next, in order to design the filter capacitor, the base capacitance is defined by (9),

$$C_b = \frac{1}{2\pi f_g Z_b} = \frac{1}{2\pi f_g}\frac{P_n}{v_g^2} \tag{9}$$

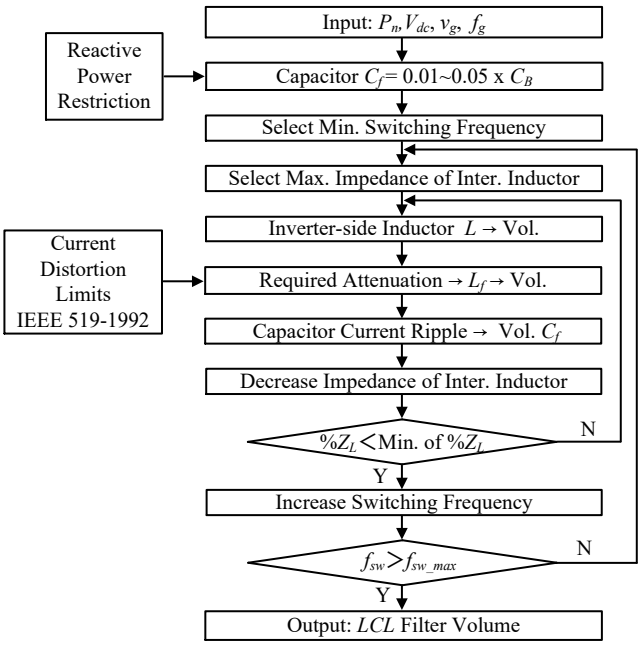


Fig. 10. LCL filter design algorithm. In DCM, the LCL filter can be optimized in aspect of volume or loss because the DCM disturbance gain is much smaller compared to CCM even with a small impedance of the LCL filter.

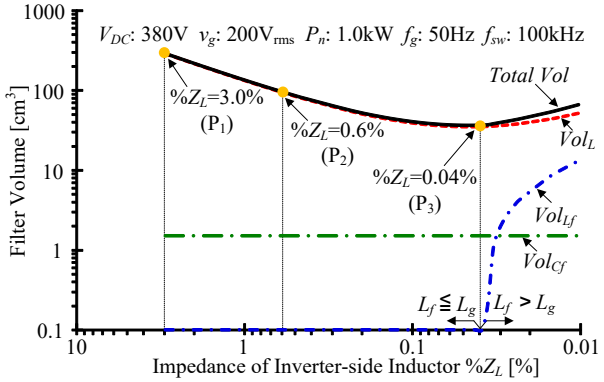


Fig. 11. Relationship between filter volume and inductor impedance at switching frequency of 100 kHz. The filter volume can be minimized greatly when reducing the impedance of the inverter-side inductor.

The filter capacitor value is limited by the decrease of the power factor at rated power (generally less than 5%), i.e. the reactive power restriction. Next, at the certain combination of the switching frequency f_{sw} and the impedance of the inverter-side inductor $\%Z_L$, the inductor value L is calculated. In the conventional CCM current control, the impedance of the inverter-side inductor L is necessary to be designed larger than several percentages of the base impedance of the inverter, because the disturbance response worsens with a small impedance of the inductor. This limits the minimization of the inductor. In the proposed DCM current control, the impedance of the inverter-side inductor L can be simply reduced in order to minimize the inductor volume, because the gain of the disturbance response is much smaller than that of the conventional CCM current control as shown in Fig. 9. This enables the optimization of the inductor volume in aspect of the inductor volume. Then, selecting a current ripple attenuation with respect to the ripple on the inverter side, the filter inductor value L_f is calculated. Minor inductor design loops are conducted in order to optimize the inductor volume and loss. After that, the volume of the filter capacitor is calculated based on the capacitor current ripple. Finally, the switching frequency and the impedance of the inverter-side inductor are varied in order to optimize the LCL filter [14]-[16].

Fig. 11 depicts the filter volume against the impedance of the inverter-side inductor. For the simplification, in this digest only the switching frequency of 100 kHz and the filter capacitor value of 0.2 μF are considered. When $\%Z_L$ decreases: the volume of the filter capacitor is almost unchanged; the filter inductor value L_f increases due to the increase in the required attenuation. However, the filter inductor volume stays at zero until the filter inductor value L_f becomes higher the minimum value of the grid

intrinsic inductor value L_g, which is 42 μH [3]-[4]. On the other hand, the inverter-side inductor volume Vol_L decreases due to the decrease in the inductance. The analysis of the current control performance and the volume evaluation of the inverter are carried out at three design points (P1-P3).

IV. Experimental Results

Table I depicts the experimental parameters. The operation frequency of the current controller is synchronized with the sampling frequency of 25 kHz despite of the high switching frequency of 100 kHz. This enables the use of low speed controllers.

Table II shows the specifications of the inductors in LCL filters, whereas Fig. 12 depicts the prototypes of the inverter-side inductors L under different conditions of the inductor impedance $\%Z_L$. Ferrite is chosen to be the core material in order to minimize the core loss at the switching frequency of 100 kHz, whereas Litz wire is used in order to minimize the winding loss coming from the proximity effect and the skin effect. By the application of DCM, the impedance of the inductor impedance $\%Z_L$ can be minimized without worsening the disturbance response as shown in Fig. 9. Consequently, by reducing the impedance of the inverter-side inductor $\%Z_L$ from 3.0% to 0.04%, the inductor volume is reduced by 77%.

Fig. 13 shows the grid voltage, grid current and inverter output current. The IEEE-519-1992 standards require the grid current THD below 5% at rated load, which can be accomplished simply with the high impedance of the inverter-side inductor $\%Z_L$ as shown in Fig. 13(a) [1]. However, as the inverter-

TABLE I
SYSTEM PARAMETERS.

Circuit Parameter		
V_{DC}	DC link Voltage	380 V
v_g	Grid Voltage	200 Vrms
P_n	Nominal Power	1 kW
Switching Device		sch2080ke
f_g	Grid Frequency	50 Hz
Z_b	Base Impedance	26.7 Ω
C_b	Base Capacitance	119 μF
C_f	Filter Capacitor	2 μF
f_{sw}	Switching Frequency	100 kHz
t_{dead}	Deadtime	400 ns

Current Controller Parameter		
f_{samp}	Sampling Frequency	25 kHz
ζ	Damping Factor	0.707
f_c	Cutoff Frequency	1 kHz
SiC Device Ratings		
V_{DSS}	Drain − Source Voltage	1200 V
I_D	Continuous Drain Cur.	40 A
R_{ds}	On-state Resistance	117 mΩ
t_r	Rise time	33 ns
t_f	Fall time	28 ns
V_{SD}	Forward Voltage	1.3 V

TABLE II
SPECIFICATIONS OF INDUCTORS IN LCL FILTERS.

X_{L1} / Z_b	**3% (P1)**	**0.6% (P2)**	**0.04% (P3)**
Max. Cur. i_{peak} [A]	7.2	7.6	15.5
Inv. side Ind. L [μH]	3800	770	50
Core Type	EE55	EE42	EE36
Core Material	Ferrite N87		
Wire	Litz Round 2UEWSTC 100 / ϕ0.1		
Air Gap [mm]	3	2	1.9
Number of Turns	115	59	16
Volume [cm^3]	119 (1 p.u.)	52 (0.43 p.u.)	25 (0.21 p.u.)
Filter Ind. L_f [μH]	1.9	7.6	31.3
Using grid-side inductor L_g as L_f because $L_f < L_g$			

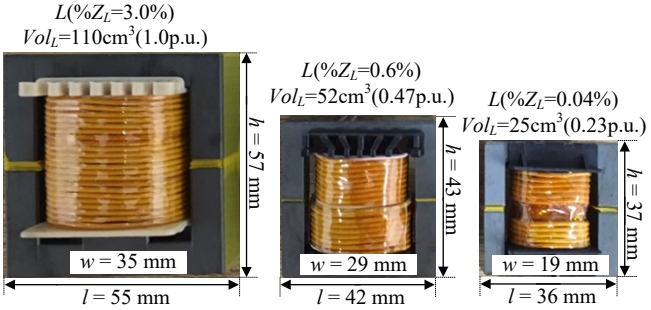
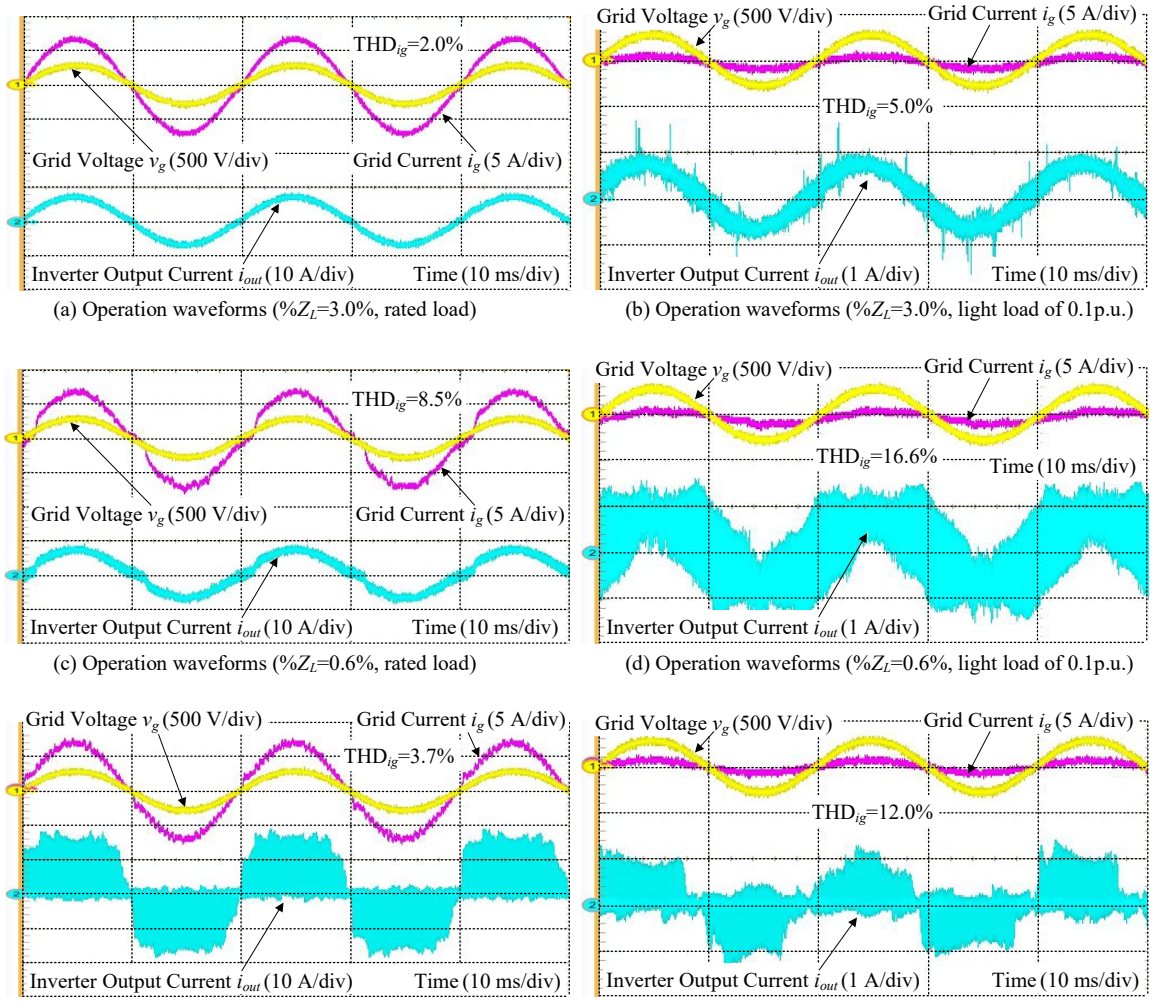


Fig. 12. Prototypes of inverter-side inductors under different condition of inductor impedance. By reducing the impedance of the inverter-side inductor $\%Z_L$ from 3.0% to 0.04%, the inductor volume is reduced by 77%.



(a) Operation waveforms (%Z_L=3.0%, rated load)

(b) Operation waveforms (%Z_L=3.0%, light load of 0.1p.u.)

(c) Operation waveforms (%Z_L=0.6%, rated load)

(d) Operation waveforms (%Z_L=0.6%, light load of 0.1p.u.)

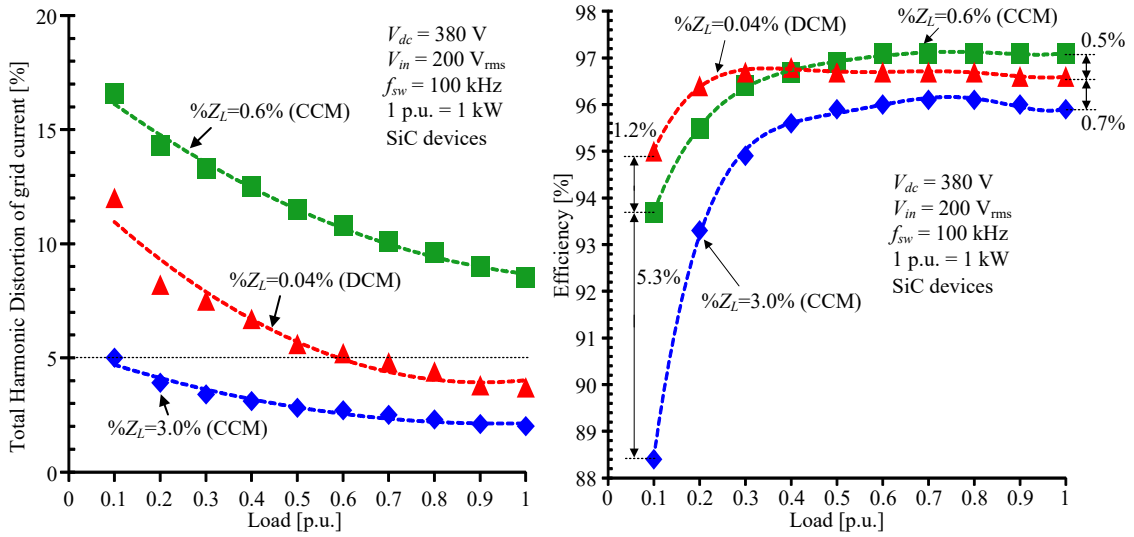
(e) Operation waveforms (%Z_L=0.04%, rated load)

(f) Operation waveforms (%Z_L=0.04%, light load of 0.1p.u.)

Fig. 13. Measured grid voltage, grid current and inverter output current. By the employment of the proposed DCM current control, the grid current THD below 5% at rated load is achieved even with a small inductor impedance of 0.04%.

side inductor value is reduced to minimize the LCL filter as shown in Fig. 11, the disturbance effects increase with the small Z_L. Consequently, the grid current THD rises from 2.0% to 8.5% when %Z_L is reduced from 3% to 0.6%. This problem can be overcome by increasing the control bandwidth of the current controller, which is difficult to employ with low speed controllers. On the other hand, when the inverter is operated in DCM, the disturbance effects naturally reduce at low duties as shown in Fig. 9, i.e. the zero-crossing intervals, due to the nonlinearity in the disturbance response. Therefore, the low grid-current THD of 3.7% is achieved with the proposed DCM current control even when %Z_L is reduced to 0.04%. Furthermore, at the light load of 0.1 p.u., the grid current THD reduction by the proposed DCM current control is also confirmed from 16.6% to 12.0% as shown in Fig. 13(d) and 13(f).

Fig. 14 shows the comparison of the grid current THD and the efficiency under different values of the inductor impedance. In CCM, the disturbance gain is constant against load, which results in the increase of the grid current THD at light load. On the other hand, by utilizing the DCM nonlinearity in the disturbance response, in which the disturbance gain decreases naturally at light load, the low grid current THD can be achieved. In particular, as shown in Fig. 14(a), even when the impedance of the grid-tied inductor %Z_L is minimized to 0.04% of the inverter total impedance, the grid current THD is maintained to be lower than 5% over wide load range from 0.6 p.u. to 1.0 p.u. by the proposed DCM current feedback control. Furthermore, as shown in Fig. 14(b), the efficiency at rated load with %Z_L = 0.04% is improved by 0.7% compared with %Z_L = 3.0% due to the decrease in the winding loss by reducing the inductor value. However, the efficiency at rated load with % Z_L = 0.04% is lower by 0.5% compared with %Z_L = 0.6% due to the increase in the current peak i_{pk}. At light load of 1.0 p.u., the efficiency %Z_L = 0.04% is improved by 1.2% and 5.3% compared with %Z_L = 0.6% and %Z_L = 3.0%,



(a) Grid current THD against load (b) Efficiency against load

Fig. 14. Comparison of grid current THD and efficiency under different values of inductor impedance. By the application of DCM, the low grid current THD and the efficiency improvement can be achieved.

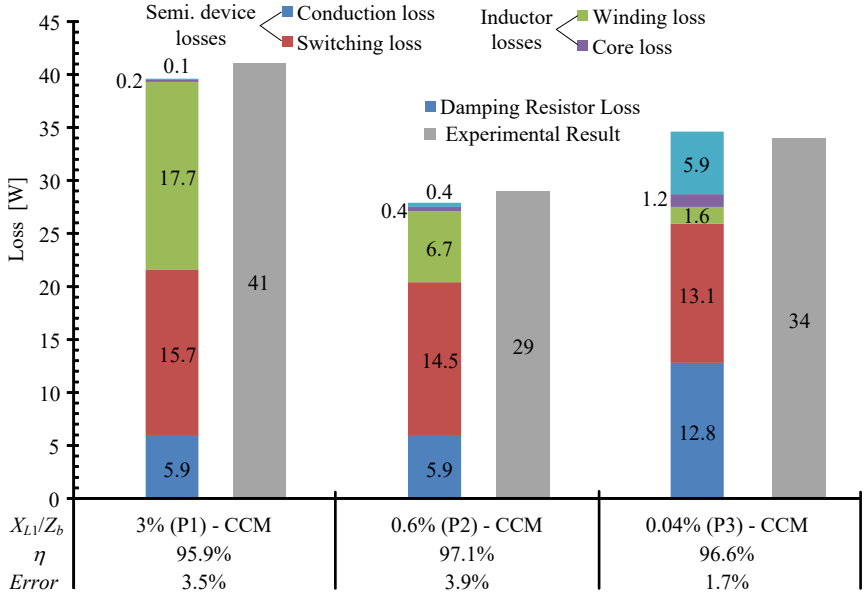


Fig. 15. Volume and loss distribution of at three design points (P1-P3).

respectively. The reason is because when the inverter is operated in DCM, the current ripple naturally decreases at light load, whereas the current ripple in CCM is constant against the load as shown in Fig. 13. The reduction in the current ripple at light load results in the decrease in the inductor loss and the switching device loss.

Fig. 15 depicts the loss distribution at three design points (P1-P3) and the measured inverter loss. The semiconductor device losses and the damping resistor loss are obtained from the simulator PLECS, whereas the inductor losses are obtained from the GECKO simulation. At the high %Z_L of 3% the winding loss dominates the total loss as shown in Table II due to the high number of turns to obtain the high inductance L. Note that the core loss at P1 is very small due to the small current ripple as shown in Fig. 13(a). On the other hand, when %Z_L is reduced to 0.04% to operate the inverter completely in DCM, the conduction loss of the semiconductor greatly increases due to the high current ripple as shown in Fig. 13(e). Nevertheless, the switching loss and the winding loss decrease due to the elimination of the recovery loss and the small numbers of winding turns. Furthermore, the maximum error between the calculated value and the experimental result is 3.9%. This small error enables the maximum power density of the gird-tied inverter with an acceptable efficiency to be achieved by the evaluation of the overall volume and loss [12].

V. Conclusion

When the grid-tied inductor was minimized by reducing the inductor impedance, the disturbance effects increased highly in the CCM operation, which distorted the grid current. On the other hand, in the DCM operation, the nonlinearity occurred in the disturbance response which resulted in the natural decrease in the disturbance gain at light load. By utilizing this DCM nonlinearity in the disturbance response, the grid current THD was maintained below 5% over wide load range even when the inductor impedance is minimized to 0.04%. However, another DCM nonlinearity occurred in the current command response, which made the open loop gain of DCM much lower than CCM. Therefore, the circuit-parameter-independent DCM nonlinearity compensation for the current command response was proposed by utilizing the duty ratio at the previous calculation period.

In the future work, the current control of the mixed-current-mode between CCM and DCM will be investigated in order to minimize the inductors without worsening the efficiency.

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