ZVRT Capability of Minimized-LCL-filter-based Single-phase Grid-tied Inverter with High-speed Gate-block

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***Abstract*— This paper proposes a Zero-Voltage Ride-Through (ZVRT) method and an LCL filter optimization design method to meet the Fault Ride Through (FRT) requirements for a single-phase grid-tied inverter with a minimized LCL filter. The inverter output current overshoots at a voltage sag when the small LCL filter is used. As a proposed method in this paper, the inverter output current overshoot is suppressed with the high-speed gate-block at the grid voltage drop and recovery. In order to suppress the overshoot current which is faster than switching period, this paper clarifies the design method of the minimized LCL filter to meet the FRT requirements. In particular, the designed LCL filter results that the interconnected inductor impedance is 1.0% of the inverter normalized impedance, whereas the filter inductor is %Z = 0.78%. Moreover, the inverter output current overshoot rate is suppressed to 37.2% by the high-speed gate-block and the designed LCL filter. Therefore, it is possible to meet the FRT requirements with the proposed ZVRT method and the designed LCL filter.**

Keywords—grid-tied inverter; FRT capability; minimized LCL filter; high-speed gate-block

I. INTRODUCTION

In recent years, photovoltaic systems (PV) have been actively studied for energy saving [1]-[3]. The PV system is applied with a grid-tied inverter in order to convert from DC power source to AC power. The inverter is required to have a small volume [4]-[5]. In particular, the interconnected inductor occupies a majority of the inverter size. Therefore, the interconnected inductor is highly required to reduce the size. Conventionally, an LC filter is employed due to its simplicity. The size of inductor is reduced by high switching frequency with SiC and GaN devices from the view point of the reduction of the current ripple. The filter capacitor is designed from the cutoff frequency of the inverter side LC filter. However, in order to effectively reduce the current ripple components of the inverter output current with an extremely minimized filter, the grid-side inductor is employed to form the LCL filter which has a high attenuation rate [6]-[7].

The grid-tied inverter is required to meet the Fault Ride Through (FRT) requirements, in order to continue the operation of the inverter during the voltage sag [8]-[13]. Moreover, it is necessary to suppress the inverter output current overshoot rate to less than 50% of the rated output current peak. Generally, an inductance of interconnected inductor is necessary to be designed in order to meet the FRT requirements. For instance, the interconnected inductor impedance is 2.1% of the inverter normalized impedance in order to carry out the FRT in [8]. This is because the reduction of the inductance for the interconnected inductor causes the decrease of the disturbance suppression performance. Furthermore, when the interconnected-inductor value is small, the inverter output current overshoot increases during the voltage sag. When the disturbance effects become large in the short grid failure, the Zero-Voltage Ride-Trough (ZVRT) operation and the reduction of the inverter output current overshoot are difficult to achieve in the small inductor because the inverter output current overshoot becomes high.

In [14], the ZVRT operation with the minimized interconnected inductor constructed by LC filter is developed by authors. In order to meet the FRT requirements, the grid-tied inverter is applied the momentary high-speed gate-block method. The gate-block operation is carried out when the inverter output current reaches the current threshold. By applying this method, the inverter output current overshoot rate is reduced to less than 50%. Thus, the grid-tied inverter with the minimized interconnected inductor meets the FRT requirements. However, when the LCL filter is applied as output filter or considering grid inductance with the LC filter, resonance occurs in the grid-side LC filter because of a voltage fluctuation. Thus, the inverter output current overshoot that is the sum of the resonance current and the steady-state current occurs in the LCL filter during the voltage sag. Therefore, in order to meet the FRT requirements, the ZVRT operation method and the LCL filter design method by considering the resonance current in the grid-side LC filter and the steady-state current are necessary.

In this paper, the ZVRT operation method meeting FRT requirements is proposed with a high-speed gate-block and the design method of the LCL filter. When the grid voltage fluctuation such as voltage drop and voltage recovery is detected, the gate-block operation is carried out. Thus, by using the proposed method, the grid-tied inverter with the minimized LCL filter is possible to continue the operation without disconnecting from the grid. In addition, in order to meet the FRT requirements, it is necessary to optimally design the LCL filter. The LCL filter is designed by deriving the equation of the inverter output current at the grid voltage recovery with the gate-block. This

ensures that the inverter output current overshoot rate which includes the resonance current of the grid-side LC filter is less than 50% of the rated output current peak at the voltage recovery. The ZVRT operation meeting FRT requirements is demonstrated with a 1-kW prototype.

II. Zero-voltage Ride-through Method for Minimized LCL Filter

A. *Conventional FRT Method*

Figure 1 shows a circuit configuration of a single-phase grid-tied inverter with an LCL filter. In this paper, an H-bridge single-phase two-level inverter is employed due to its simplicity. In order to minimize the LCL filter, the inductance and capacitance are reduced by increasing the switching frequency of the inverter. Due to the reduction of the inductance in the LCL filter, the inverter output current overshoots at the grid voltage drop and the grid voltage recovery. Consequently, the grid-tied inverter is stopped by the over current protection, and cannot continue the operation with the reduced inductance.

Figure 2 shows a reactive current control method for an FRT operation. The phase θ is locked by phase-locked-loop (PLL) based on the grid voltage detection value v_{acdet}. During the voltage sag, the detection signal v_{frt} becomes one, and the current phase θ' is the sum of the present voltage phase θ and $\pi/2$. The reactive current control is achieved by generating a current command value with the current phase θ'.

Figure 3 shows the control block diagram of the conventional FRT operation where V_{dc} is the input DC voltage, T_d is the dead-time period, i_{L1det} is the inductor current detection value, f_{sw} is the switching frequency and T_{delay} is the delay time of the inductor current detection. The current controller is implemented by digital signal processor (DSP). Moreover, a dead-time error voltage of the inverter output is compensated by using the dead-time error voltage compensation at a steady-state operation. When the inductance of the interconnected inductor becomes low, the grid current is distorted by the grid disturbance due to the increasing disturbance gain. Therefore, the inverter output current overshoot is caused due to the use of the conventional FRT method at the voltage sag.

Figure 4 shows the control block diagram of the conventional FRT operation with a disturbance observer [15]-[21]. The disturbance observer is implemented by digital hardware in field-programmable gate array (FPGA). Thus, the disturbances such as dead time error voltage and voltage drop of switching devices are compensated at high speed. The disturbance voltage $\hat{v}_{dis}$ is estimated from the output current and the voltage command as

$$\hat{v}_{dis} = \frac{\omega_c}{\omega_c + s} v_L^{*} - \frac{s\omega_c L_1}{\omega_c + s} i_{L1det} \quad (1),$$

where ω_c is the cutoff angular frequency of the disturbance observer, v_{conv}^{*} is the inverter output voltage command and s is the Laplace operator. Moreover, the current controller is added with the detected voltage of the filter capacitor v_{cdet} for a voltage-feedforward compensation. Consequently, the dead-time voltage error is compensated by the disturbance observer,

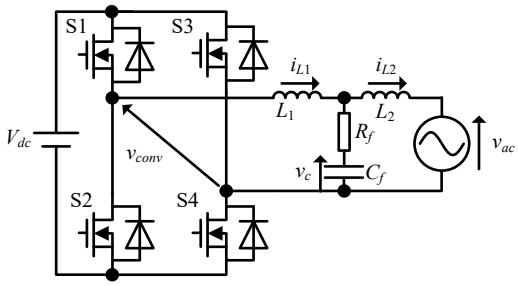
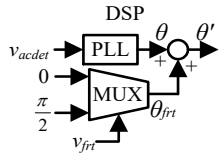


Fig. 1. Single phase inverter circuit with LCL filter. The interconnected inductor L_1 and the filter inductor L_2 are reduced by increasing the switching frequency.



	MUX	
	Normal operation	FRT
v_{frt}	0	1
θ_{frt}	0	$\pi/2$

Fig. 2. Reactive current control method for FRT operation. When voltage sag occurs, the phase θ' is advanced by $\pi/2$ from θ.

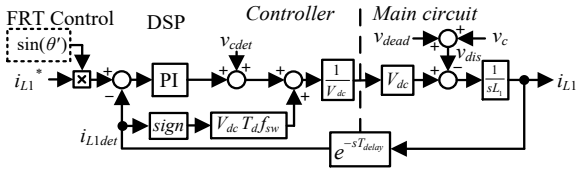


Fig. 3. Control block diagram of conventional FRT operation. In the conventional method, the current controller is implemented by DSP.

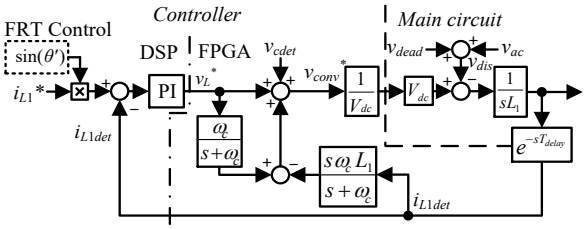


Fig. 4. Control block diagram of conventional FRT operation with disturbance observer. In this method, the disturbance observer is implemented by FPGA in order to compensate wideband disturbances.

whereas the grid voltage is compensated by the voltage feedforward. However, when the short grid failure occurs, the disturbance compensation with the voltage feedforward and the disturbance observer cannot detect the grid failure immediately due to the delay time of the detection and the sampling. Thus, the inverter output current overshoot rate becomes higher than 50% with the minimized LCL filter. Therefore, the high-speed control is necessary in order to suppress the overshoot of the inverter output current i_{L2} during the voltage sag.

B. *Proposed ZVRT Method*

Figure 5 shows the control block diagram of the high-speed gate-block with the disturbance observer for the ZVRT operation. In order to suppress the inverter output current overshoot, a gate-block is carried out by the detection of the grid voltage fluctuation. By filtering the grid voltage by a high-pass-

filter (HPF), the gate-block operation is carried out when the HPF output gets over the threshold V_{ac_GB}. Furthermore, in order to achieve the ZVRT operation at high speed response, the gate-block control is implemented by digital hardware in FPGA, whereas the HPF and the detection circuit are constructed by analog circuit. Therefore, the detection delay time until the gate-block operation is minimized, i.e. one of the main factors to reduce the overshoot.

III. Optimized Design for Minimizing LCL Filter

A. *Derivation of Output Current at Grid Voltage Recovery*

When a grid voltage sag occurs, a resonance occurs in the grid-side LC filter. The inverter output current overshoots due to the combination of the resonance current and the steady-state current. The gate-block operation in H-bridge inverter is impossible to suppress resonances in the grid-side LC filter. Thus, it is necessary to design the parameters of the LCL filter with the grid-side LC filter resonance in order to meet the FRT requirements. The equation of the inverter output current at the voltage recovery is derived in order to design the LCL filter.

Figure 6 shows the transient phenomenon of the inverter output current with the LCL filter at the grid voltage recovery. Area (i) of Fig. 6 shows the time from the voltage recovery to when the gate-block is carried out ($0 \leqq t \leqq t_{bd}$). Area (ii) shows the time after the gate-block operation ($t \geqq t_{bd}$). Note that t_{bd} is the delay time from the voltage sag to when the gate-block is carried out. In the area (i), the delay time t_{bd} is the sum of the delay time of the gate-block such as the detection delay time of the analog circuit and the control delay time of the gate-block operation in the FPGA. The inverter-output-current maximum value i_{L2_max} and the time reaching the maximum current t_{imax} are calculated in area (ii). In addition, the LCL filter is designed in order that the inverter output current maximum value is less than the inverter output current overshoot rate of 50% i_{th} according to the FRT requirements.

Figure 7 shows the circuit model with the LCL filter after the gate-block ($t \geqq t_{bd}$) in the area (ii) of Fig. 6. The equation of the inverter output current during the transient interval is derived by considering the LCL filter circuit from the viewpoints of the inverter and the grid separately. After the gate-block, the inverter output voltage V_{conv} is applied to the inverter-side LC filter in order to inject the current of the reverse vector to the inverter output current. The inverter output voltage is equal to the input DC voltage V_{dc}. When considering the inverter output side, the rated inverter output current peak $-I_{L2}$ flows until the gate-block is carried out. Thus, the positive inverter output voltage V_{conv} is applied after the gate-block in order to flow the current with the positive direction. In Fig. 7, the circuit equations are derived as shown in (2)-(4)

$$\frac{V_{conv}}{s}e^{-st_{bd}} = sL_1 I_{L1}(s) + sL_2 I_{L2}(s) + \frac{V_{ac}}{s} \tag{2}$$

$$\frac{I_{Cf}(s)}{sC_f} = sL_2 I_{L2}(s) + \frac{V_{ac}}{s} \tag{3}$$

$$I_{L1}(s) = I_{L2}(s) + I_{Cf}(s) \tag{4},$$

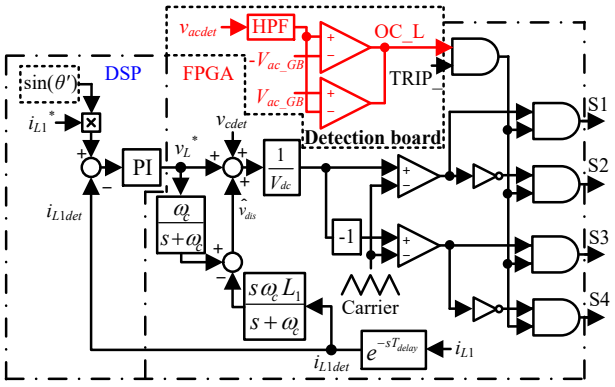


Fig. 5. Control block diagram of ZVRT operation with gate-block. By using gate-block, the inverter output current overshoot is suppressed at the grid voltage drop and the grid voltage recovery.

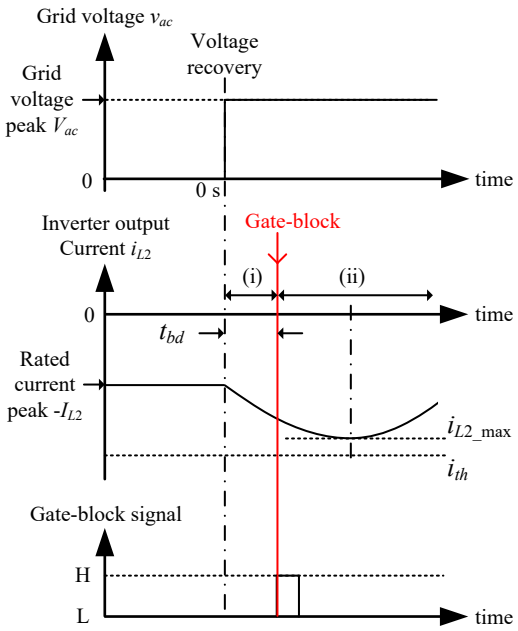


Fig. 6. Transient phenomenon of inverter output current i_{L2} with LCL filter during voltage recovery. The LCL filter has to be designed in order that the maximum current i_{L2_max} is less than the limitation i_{th} of the current overshoot according to FRT requirements.

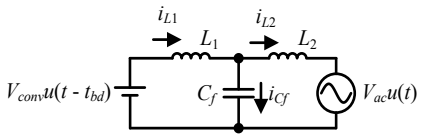


Fig. 7. Circuit model with LCL filter after gate-block. The transient phenomenon of Inverter output voltage and grid voltage are considered.

where $I_{L1}(s)$ is Laplace transform of the interconnected inductor current i_{L1}, I_{L2} (s) is Laplace transform of the filter inductor current i_{L2}, I_{cf} (s) is Laplace transform of the filter capacitor current i_{cf}, and V_{ac} is the grid voltage peak. By using (2)-(4) and the rated inverter output current peak I_{L2}, the filter inductor current i_{L2} is expressed as

$$i_{L2} = -I_{L2} + \frac{V_{conv}(t-t_{bd}) - V_{ac}t}{L_1 + L_2} - \frac{1}{L_1 + L_2}\sqrt{\frac{L_1 C_f L_2}{L_1 + L_2}}\left\{\frac{L_1}{L_2}V_{ac}\sin\left(\sqrt{\frac{L_1 + L_2}{L_1 C_f L_2}}t\right) + V_{conv}\sin\left(\sqrt{\frac{L_1 + L_2}{L_1 C_f L_2}}(t-t_{bd})\right)\right\} \quad (5).$$

In order to design the LCL filter meeting FRT requirements, the period until the inverter output current reaches maximum entitled $t_{i\max}$ as shown in Fig. 6 is derived as follows. First, considering (6) as the filter inductor resonance voltage component $v_{L2\_res}(t)$,

$$v_{L2\_res}(t) = \frac{L_1}{L_2}V_{ac}\sin\left(\sqrt{\frac{L_1 + L_2}{L_1 C_f L_2}}t\right) + V_{conv}\sin\left(\sqrt{\frac{L_1 + L_2}{L_1 C_f L_2}}(t-t_{bd})\right) \quad (6).$$

When the differentiate equation for (6) becomes zero, the time reaching the maximum inverter output current $t_{i\max}$ is derived as

$$t_{i\max} \approx \frac{t_{bd}}{\left(\frac{L_1}{L_2}\frac{V_{ac}}{V_{conv}} + 1\right)} + \frac{\sqrt{\left(\frac{L_1}{L_2}\frac{V_{ac}}{V_{conv}} + 1\right)\left(\frac{2L_1 C_f L_2}{L_1 + L_2} + \frac{2L_1{}^2 C_f}{L_1 + L_2}\frac{V_{ac}}{V_{conv}}\right) - \frac{L_1}{L_2}\frac{V_{ac}}{V_{conv}}t_{bd}{}^2}}{\left(\frac{L_1}{L_2}\frac{V_{ac}}{V_{conv}} + 1\right)} \quad (7),$$

where the approximation of $\sin(x) \approx x - x^3/6$ is applied to (6) in order to derive (7). By substituting $t_{i\max}$ in (7) to t in (5), the maximum inverter output current after the gate-block $i_{L2\_\max}$ is derived.

B. *Flowchart of LCL filter design*

Figure 8 shows the flowchart of the LCL filter design method. First, the inverter side LC filter is designed from the specification of the inverter. For example, the interconnected inductor L_1 is designed from the current ripple, the switching frequency or %Z for the output impedance of the inverter. The inductance of the interconnected inductor L_1 is derived as shown in (8) or (9)

$$L_1 = \frac{V_{ac}}{\Delta I_{L1} f_{sw}}\frac{V_{dc} - V_{ac}}{V_{dc}} \quad (8)$$

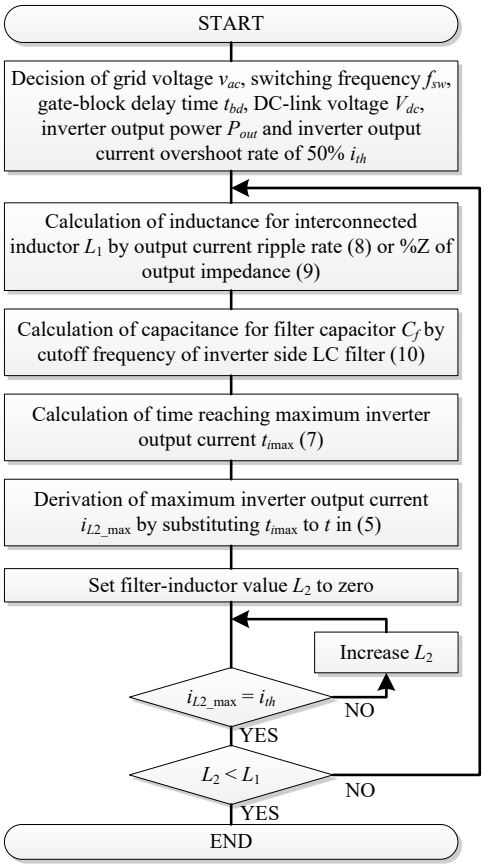


Fig. 8. Flowchart of LCL filter optimized design for grid-tied inverter. The LCL filter is designed to meet FRT requirements.

$$L_1 = \frac{2\pi f_{grid}}{\%Z_{L1}}\frac{P_{out}}{v_{ac}{}^2} \quad (9),$$

where ΔI_{L1} is the current ripple of the interconnected inductor, $\%Z_{L1}$ is %Z of the interconnected inductor, f_{grid} is frequency of the grid, v_{ac} is rms value of the grid voltage and P_{out} is inverter output power. The filter capacitor C_f is determined from the cutoff frequency of the inverter-side LC filter f_{LC_cut}. The filter capacitor C_f is expressed as

$$C_f = \frac{1}{\left(2\pi f_{LC\_cut}\right)^2 L_1} \quad (10).$$

After that, the filter inductor L_2 is determined to meet the FRT requirements according to (5) and (7). When determining the filter inductor, if the interconnected inductor L_1 is less than the filter inductor L_2, the inverter side LC filter should be redesigned. Table I shows the calculation result of the LCL filter design based on the flowchart of Fig. 8. The interconnected inductor impedance is 1.0% of the inverter normalized impedance, whereas the filter inductor is 0.78%. The filter capacitor is determined to let the cutoff frequency of inverter side LC filter be 10 kHz (one eighth of switching frequency). In the calculation result with the designed LCL filter, the output current overshoot rate is suppressed less than 50%. Moreover, in order to reduce the resonance current in the LCL filter, a damping resistor R_f is

TABLE I. INITIAL CONDITION AND CALCULATION RESULT OF LCL FILTER DESIGN.

Initial condition	
Grid voltage V_{ac}	283 V
DC-link voltage V_{dc}	380 V
Output power P_{out}	1 kW
Rated inverter output current I_{L2}	±7.07 A
Inverter output voltage V_{inv}	380 V
Switching frequency f_{sw}	80 kHz
Gate-block delay time t_{bd}	3.0 μs
Inverter output current limit by FRT requirement i_{th}	$\pm I_{L2} \times 1.5$
Calculation result	
Interconnected inductor L_1	1.29 mH
Filter capacitor C_f	0.2 μF
Filter inductor L_2	0.99 mH
Maximum inverter output current at recovery voltage i_{L2_max}	-10.3 A (45.2%)

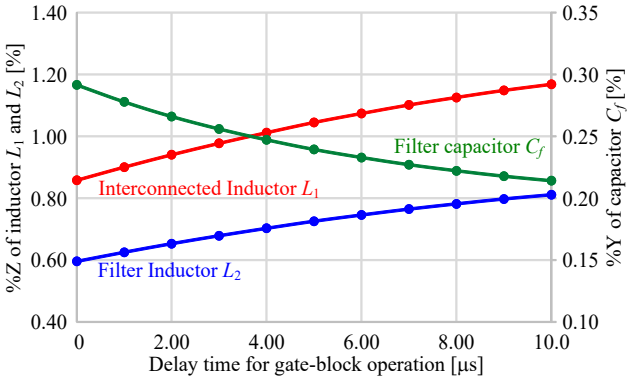
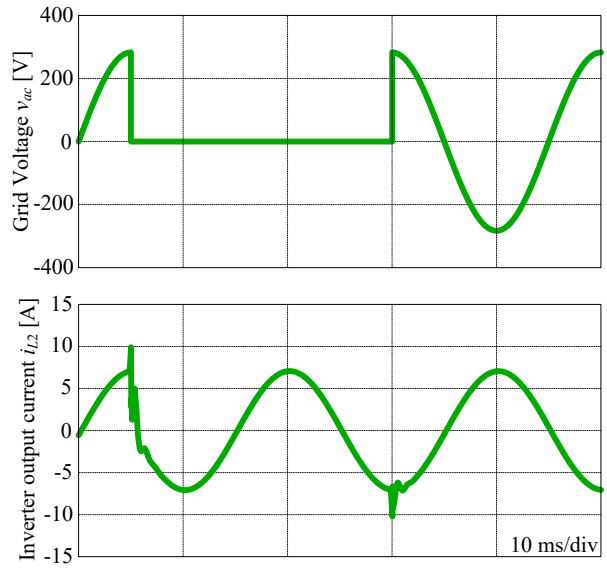


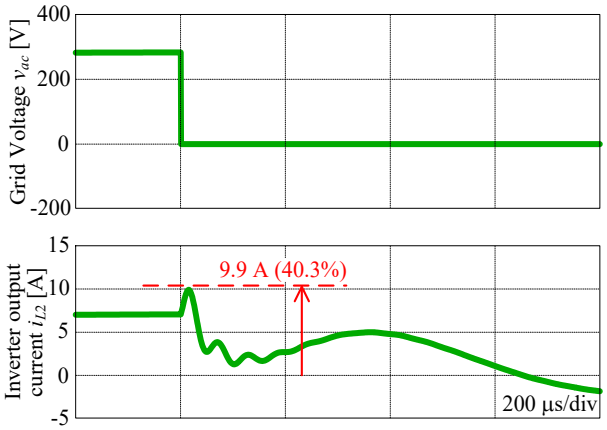
Fig. 9. Relationship between delay time of gate-block operation and design parameters of minimized LCL filter in 1-kW system. The LCL filter parameter is designed in order that the inverter output current overshoot rate is 50%.

connected to the filter capacitor in series. The resistance of the damping resistor is selected in order to consume below 0.1% of the inverter output power. Therefore, the voltage drop of the damping resistor is ignored.

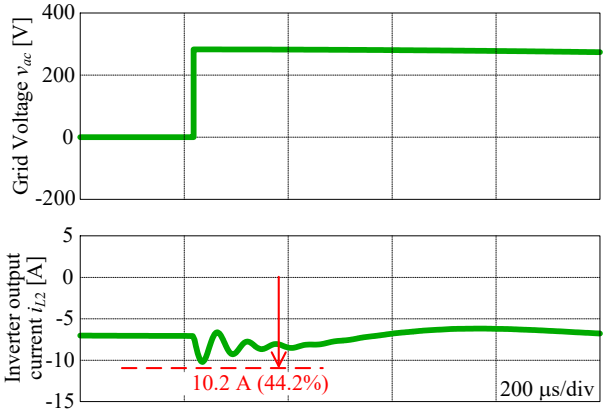
Figure 9 shows the characteristics of the delay time for the gate-block operation and the minimized LCL filter parameter when the maximum inverter output current overshoot rate is 50%. In this design, the LCL filter is designed as follows; the cutoff frequency of the inverter side LC filter is 10 kHz, the cutoff frequency of the grid-side LC filter is 12 kHz, and the maximum inverter output current overshoot rate becomes 50% at the voltage recovery. In Fig. 9, when the delay time for the gate-block operation is short, the interconnected inductor and the filter inductor are possible to minimize. This is because when the delay time for the gate-block operation is short, the effect of the inverter output current overshoot caused by the short grid failure is small. On the other words, the interconnected-inductor value and the filter-inductor value are limited by the delay time for gate-block operation.



(a) Waveform of ZVRT operation.



(b) Voltage drop operation.



(c) Voltage recovery operation.

Fig. 10. Simulation result of grid failure with minimized LCL filter by using proposed design method. The inverter output current overshoot rate is suppressed to become less than 50%.

C. *Simulation of ZVRT with designed LCL filter*

In order to confirm validity of the designed LCL filter in Table I, the ZVRT operation with the designed LCL filter is evaluated in simulation. Figure 10 shows the simulation results of the ZVRT with the proposed high-speed gate-block method.

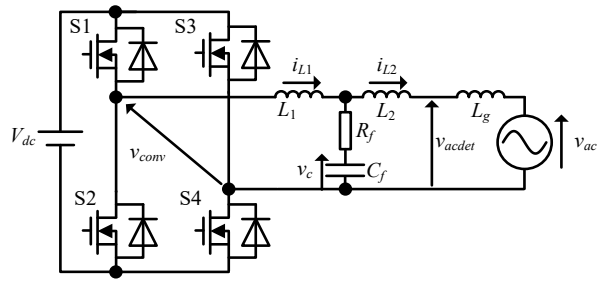


Fig. 11. Circuit configuration with grid impedance L_g. In actual grid connection, there is grid impedance between the inverter output and the grid voltage.

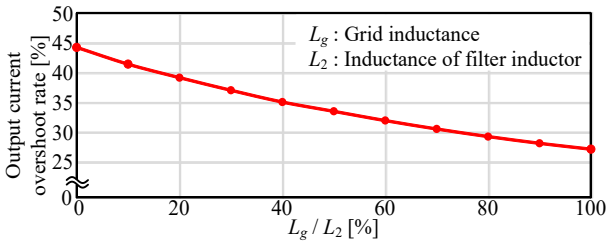


Fig. 12. Simulation results of inverter output current overshoot rate at grid voltage recovery and ratio between grid inductance L_g and filter inductance L_2. When the grid impedance is low, the output current overshoot rate becomes high.

By using the proposed high-speed gate-block method, the inverter output current is suppressed to 9.9 A at the grid voltage drop as shown in Fig. 10 (b) (Overshoot rate: 40.3%). Moreover, at the grid voltage recovery, the inverter output current overshoot is suppressed to 10.2 A as shown in Fig. 10 (c) (Overshoot rate: 44.2%). Thus, the grid-tied inverter with the minimized LCL filer meets the FRT requirements by using the proposed high-speed gate-block method. Comparing the inverter output current overshoot between the calculation value and the simulation value at the voltage recovery, the error rate is 2.2%. Thus, the validity of the LCL filter design method meeting the FRT requirements is confirmed. Moreover, the error between the calculation value and the simulation value occurs due to the damping resistor, the precision of approximation and the steady-state current at the grid voltage recovery is constant value in the calculation. Therefore, by using the high-speed gate-block method and the optimized LCL filter design method, it is possible to minimize the LCL filter and still meet the FRT requirements.

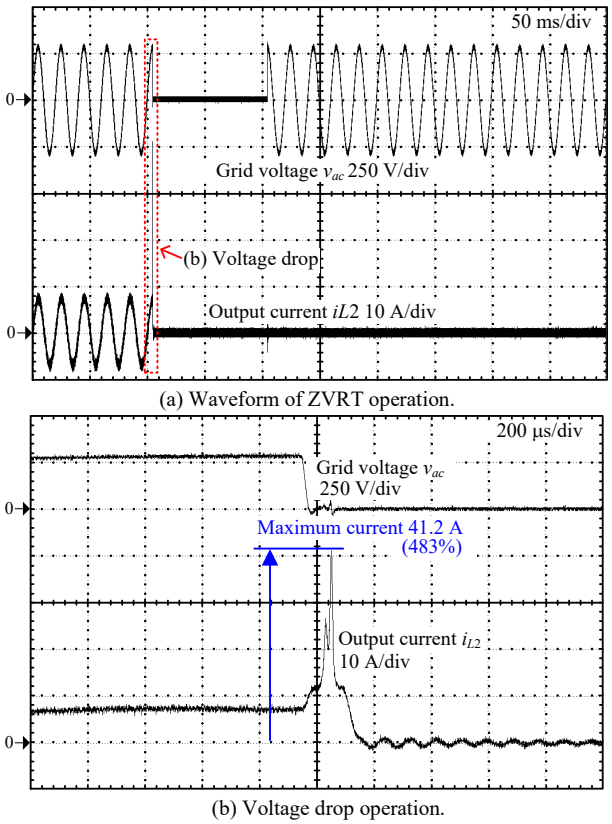
D. *Consideration of inverter output current overshoot rate with grid impedance*

Figure 11 shows the circuit diagram considering a grid inductor connected to the LCL filter at the grid-side. The effect of the grid impedance for the FRT capability by using the proposed high-speed gate-block method is confirmed under the condition that there is grid impedance in the actual grid. As shown in Fig. 11, it is impossible to directly detect the grid voltage v_{ac}, because the detection point of the grid voltage is between the grid inductor L_g and the filter inductor L_2.

Figure 12 shows the simulation results of the relationship between the inverter output current overshoot rate at the grid voltage recovery and the ratio between grid impedance and filter inductance L_g/L_2. Note that the filter-inductor value L_2 is 0.99 mH (%Z of 0.78%) which is designed in Table I. The grid impedance L_g is changed from zero to the filter-inductor value L_2. As shown in Fig. 12, the inverter output current overshoot rate is reduced by increasing the grid impedance L_g. The reason is because the inverter output current variation is reduced by increasing the grid impedance L_g.

TABLE II. EXPERIMENTAL CONDITION.

Output power	P_{out}	1 kW	Filter cap.	C_f	0.2 μF
DC link vol.	V_{dc}	380 V	Carrier fre.	f_{cry}	80 kHz
Grid voltage	v_{ac}	200 V_{rms}	Ang. fre. of ACR	ω_n	6000 rad/s
Inter. Induc. (%Z)	L_1	1.29 mH (1.0%)	Samp. fre. of ACR	f_{samp}	20 kHz
			Samp. fre. of DOB	f_{so}	80 kHz
Filter Induc. (%Z)	L_2	0.99 mH (0.78%)	Cutoff fre. of DOB	f_c	2 kHz
			GB delay time	t_{delay}	< 3 μs



(a) Waveform of ZVRT operation.

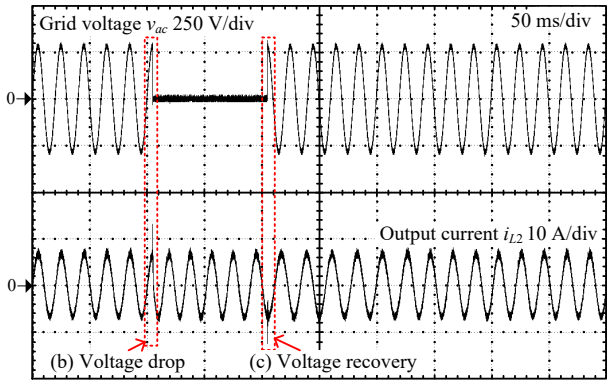
(b) Voltage drop operation.

Fig. 13. Experimental results of grid failure with conventional FRT method. The inverter output current overshoot is large due to the detection delay and the sampling delay at the voltage drop.

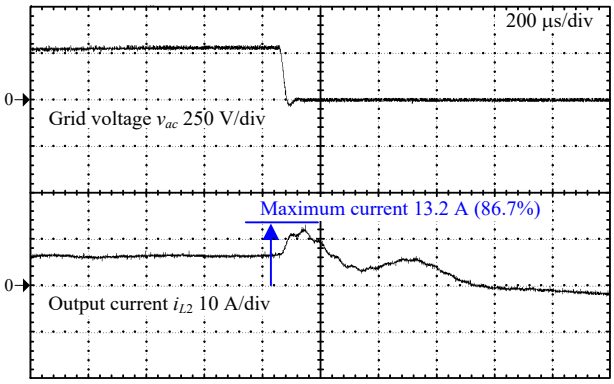
IV. EXPERIMENTAL RESULT

Table II shows the experimental condition. The LCL filter that designed in Table I is used. Note that in the experiment, in order to consider the worst case of the grid, the ZVRT operation is confirmed without the grid inductor.

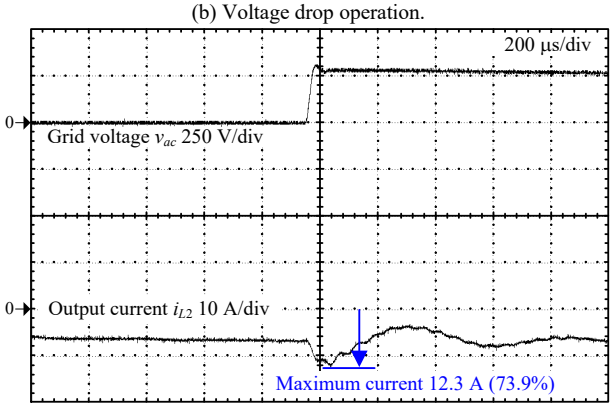
Figure 13 shows the experimental result of the ZVRT operation with the conventional FRT method without the high-performance disturbance observer. After the grid voltage drop, the inverter output current overshoots to 41.2 A (Overshoot rate:



(a) Waveform of ZVRT operation.

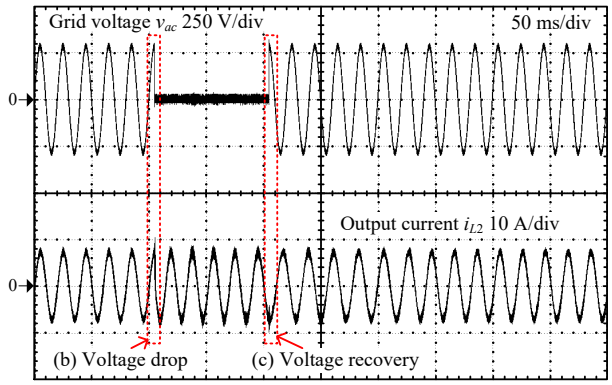


(b) Voltage drop operation.

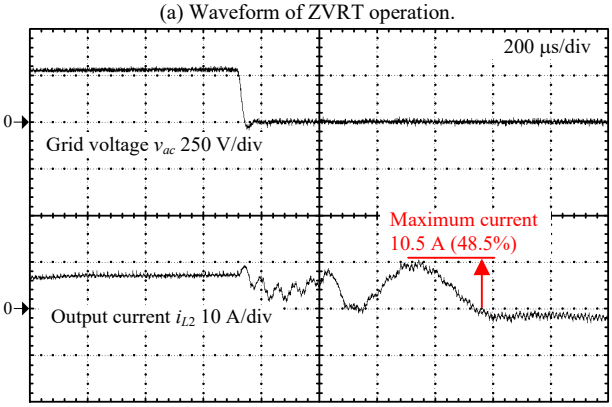


(c) Voltage recovery operation.

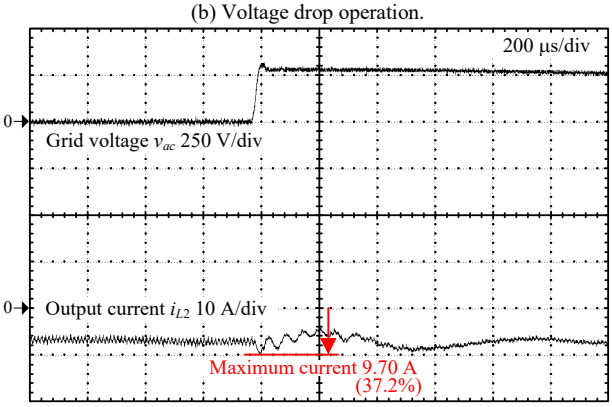
Fig. 14. Experimental results of grid failure with conventional FRT method by applying disturbance observer. The inverter output current overshoot rate exceeds 50% due to the delay for disturbance compensation caused by the detection delay and sampling delay.



(a) Waveform of ZVRT operation.



(b) Voltage drop operation.



(c) Voltage recovery operation.

Fig. 15. Experimental results of grid failure with proposed ZVRT method. By applying the proposed method, it is possible to continue the operation of the inverter, and satisfy the FRT requirements.

483%). After that, the inverter stops operation by the over current protection. Due to the detection delay and the sampling delay, the inverter output current overshoot with the minimized LCL filter is large. As a result, the inverter output current reaches the over current threshold. Therefore, in order to meet the FRT requirements, a high speed control method that is faster than the conventional method is necessary.

Figure 14 shows the experimental result for the ZVRT operation of the conventional FRT method with the high-performance disturbance observer. In Fig. 14 (a), it is possible to continue the operation during the grid failure. However, in Fig. 14 (b), the inverter output current maximum value is 13.2 A at the voltage drop (Overshoot rate: 86.7%). Moreover, in Fig. 14 (c), the inverter output current maximum value at the voltage recovery is 12.3 A (Overshoot rate: 73.9%). Thus, it is impossible to reduce the inverter output current overshoot rate less than 50% at the voltage recovery. If the sampling frequency for the disturbance compensation increases, it is possible to suppress the inverter output current overshoot less than the threshold value of over current protection with the high-performance disturbance observer. However, due to the delay time of the detection and the sampling, the inverter output current overshoot rate exceeds 50% with the minimized LCL filter that is composed by the minimized interconnected inductor (%Z of 1.0%) and filter inductor (%Z of 0.78%). As a conclusion, it is necessary to reduce the detection delay time in order to meet the FRT requirements with the minimized LCL filter.

Figure 15 shows the experimental result of the ZVRT operation with the proposed high-speed gate-block method. The inverter output current overshoot at the grid voltage drop is 10.5 A (Overshoot rate: 48.5%), whereas the inverter output current overshoot at the grid voltage recovery is 9.70 A (Overshoot rate: 37.2%). From the experimental result, the FRT requirements are satisfied by the proposed high-speed gate-block method. Therefore, it is confirmed that the grid-tied inverter with the minimized LCL filter meets the FRT requirements by the proposed high-speed gate-block method and the designed LCL filter. There is error of 5.6% between the overshoot current of calculation result and experimental result at the grid voltage recovery. The error is caused by the approximation when deriving the equation, and the inconsideration of the damping resistor.

V. CONCLUSION

In this paper, the ZVRT operation of the single-phase grid-tied inverter with the minimized LCL filter was verified. It was confirmed that the inverter output current overshoot rate during the voltage sag was suppressed to become less than 50% by the proposed high-speed gate-block method and the design of the LCL filter. In particular, the interconnected inductor was minimized to 1.0% of %Z and the filter inductor is minimized to 0.78% of %Z in the 1-kW prototype. Therefore, by applying the proposed method, it is possible to reduce the size of LCL filter and to meet the FRT requirements.

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