Wide-Load-Range Efficiency Improvement for High-Frequency SiC-Based Boost Converter with Hybrid Discontinuous Current Mode

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***Abstract*--This paper proposes a hybrid current mode between triangular current mode (TCM) and discontinuous current mode (DCM) in order to improve a wide-load-range efficiency for a high-frequency SiC-based boost converter. At rated load, TCM where the zero-voltage switching (ZVS) is achieved, is used in order to increase the switching frequency and minimize the boost converter. At light load, the hybrid current mode (HDCM) where the TCM current is flown during the zero-current interval of DCM, is applied in order to achieve both ZVS and a reduction of a current ripple. This maintains a high efficiency over a wide load range. A 1-kW prototype is realized to compare HDCM over continuous current mode (CCM), DCM and TCM. Compared to TCM, the root-mean-square current is reduced up to 56.6% with HDCM. Consequently, the efficiency of HDCM at light load of 0.1 p.u. is improved by 3.1%. Compared to DCM, the average-current ripple in HDCM is reduced by 82.3%, whereas the efficiency of HDCM at light load of 0.1 p.u. is improved by 1.5%. Finally, when the current ripple of CCM is designed to be half of TCM, the efficiency of HDCM at rated load is improved by 0.9% compared to CCM.**

***Index Terms*--DC-DC power converters, Discontinuous current mode, Triangular current mode, Zero-voltage switching.**

I. Introduction

OVER the past decades, the increase of the power density has been one of the most important design criteria in power electronics due to limited space requirements or weight reductions [1]-[3]. A typical boost DC-DC converter is widely applied in many power conversion systems, e.g. power conditioning system in photovoltaic systems. Magnetic component, i.e. a boost inductor in the boost converter, accounts for the major volume of the converter [4]. By increasing the switching frequency, the volume of the boost inductor can be reduced. However, higher switching frequency leads to an increase of switching loss, which requires larger cooling system. Therefore, a reduction of the switching loss is crucial to high power density design.

In recent years, SiC devices have emerged as promising devices for high efficiency and high density power conversion. The switching frequency of SiC devices has been push up to several hundreds of kHz in order to reduce the size of the magnetic component. The following important switching characteristic occurs in the SiC devices; turn-on switching loss is dominant due to reverse recovery charge or junction capacitor charge of free-wheeling device at hard-switching condition. Soft switching techniques can greatly reduce the turn-on switching loss, in which resonance between a inductor and a capacitor is utilized in order to achieve zero-voltage switching (ZVS) [5]-[7]. However, in order to satisfy conditions for ZVS, these methods suffer many drawbacks such as, e.g. a requirement of additional components, or a restriction of controllable duty ratio. The additional components not only restricts the minimization of the converter but also complicates the control method, whereas the limitation of the duty ratio restricts the applicable range of ZVS. Therefore, the achievement of ZVS without additional components or the limited controllable duty ratio is desired.

On the other hand, triangular current mode (TCM) operation is the most simple and effective way to achieve ZVS, and is recently introduced in the “Little Box Challenge”, i.e. a worldwide competition in order to push the forefront of power density in today’s converter systems further [8]-[11]. In TCM, turn-off switching loss can be decreased greatly by connecting a snubber capacitor in parallel with the switching devices, whereas the turn-on switching loss is eliminated by ZVS. Consequently, the switching frequency can be pushed to hundreds of kHz or several MHz. One of the main drawbacks in TCM applied with pulse-width modulation (PWM) is that the high current ripple is constant over entire load range. Consequently, it is difficult to achieve high efficiency at light load when the load current is relatively low. Therefore, it is desired to reduce the current ripple at light load in order to avoid a sharp decrease in the efficiency [8].

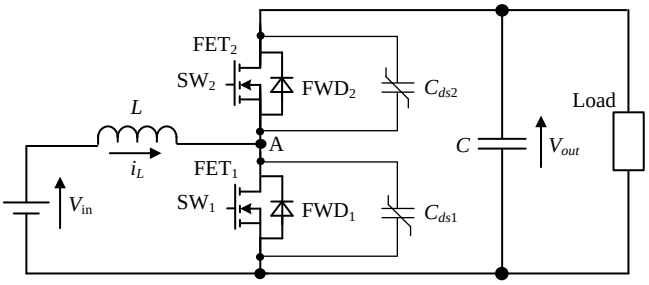


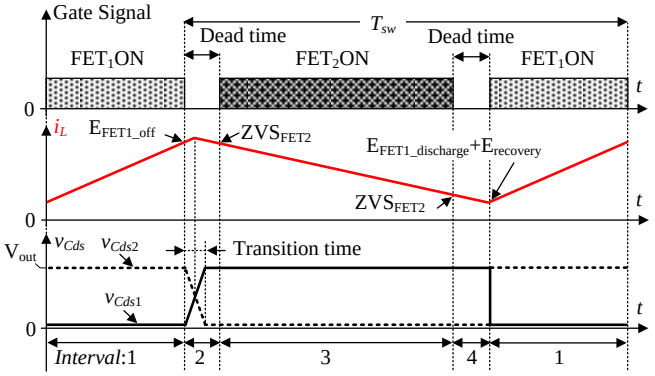
Fig. 1. Typical non-isolated boost DC-DC converter. The switching loss reduction is crucial to the high frequency design. In general, there are three current modes to operate the converter: CCM, DCM and TCM.

This paper proposes a novel concept of a hybrid current mode between TCM and discontinuous current mode (DCM), which is entitled hybrid discontinuous current mode (HDCM). The proposed current mode can achieve a high efficiency over a wide load range for a high-frequency SiC-based boost converter. In HDCM, TCM is applied during zero-current interval of DCM in order to satisfy the conditions for ZVS. Consequently, the switching frequency can be increased by HDCM in order to minimize the converter. Meanwhile, the current ripple is also reduced at light load, which results in the wide-load-range high efficiency. The remainder of this paper is organized as follows; in section II, HDCM is proposed in order to solve the problems of the conventional current modes, then in section III the design and the control of the boost converter operated in HDCM are explained. After that, experimental HDCM operations are presented in section IV. In addition, a comparison of the efficiencies among four current modes, i.e. TCM, DCM, continuous current mode (CCM) and HDCM, over a wide load range is carried out. Finally, the advantages of HDCM over other current modes are clarified based on these results.

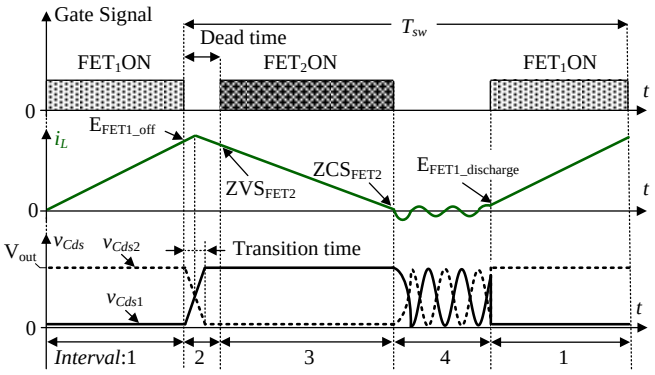
II. Hybrid Current Mode Between Discontinuous Current Mode And Triangle Current Mode

This section presents the basic principle of the switching loss occurrence in the boost converter and points out the difference between the hard switching and the proposed hybrid current mode which allows for ZVS during the complete switching period.

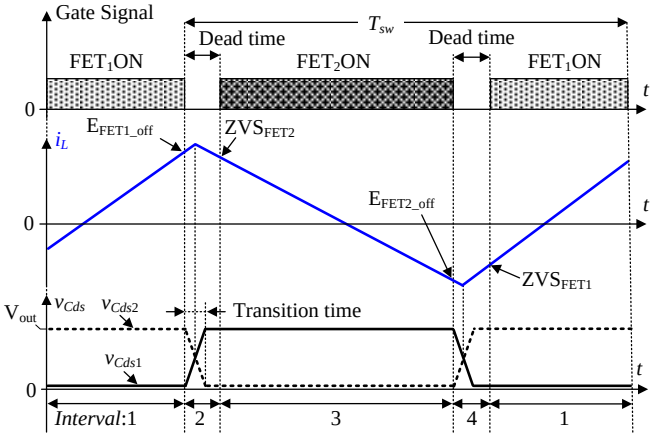
Figure 1 depicts a typical non-isolated boost converter, where the junction capacitor of the semiconductor devices are shown as C_{ds1} and C_{ds2}. In order to minimize the magnetic component, i.e. the boost inductor L, the switching frequency is required to be pushed to hundreds of kHz or even several MHz. Hence, the switching loss reduction is crucial to the high power density design. There are three conventional current modes to operate the boost converter: CCM, DCM and TCM. Note that critical current mode (CRM) can be analyzed as same as DCM without the occurrence of the zero-current interval.



(a) Switching losses in CCM. In CCM, the free-wheeling diode suffers from the significant reverse recovery loss.



(b) Switching losses in DCM. The reverse recovery issues can be alleviated by DCM. Nevertheless, in DCM, two kinds of switching loss still occur; the high turn-off loss because the switching devices is turned off at least twice of the average current, and the turn-on loss due to the junction capacitor charge.



(c) Switching losses in TCM.

Fig. 2. Switching losses in CCM, DCM and TCM. In TCM, the turn-off loss can be reduced simply by connecting a snubber capacitor in parallel with the switching devices, whereas the turn-on loss is eliminated by using the boost inductor to resonate out the junction capacitor charge before the turn-on, i.e. ZVS. However, the high current ripple is constant over entire load range with the application of PWM, which decreases the efficiency at light load.

Figure 2 depicts the pattern of the switching losses in each current mode. The switching period in CCM as depicted in Fig. 2(a) is split into two main intervals and two short resonant transitions.

Interval 1 (CCM): During interval 1, the switch SW_1 is closed, the input voltage V_{in} is applied to the inductor L, and the inductor current i_L increases linearly. At the end of the interval 1, SW_1 is turned off. Consequently, the turn-off loss occurs on SW_1.

Interval 2 (CCM): During interval 2, a switching transition takes place where the junction capacitor C_{ds1} is charged and C_{ds2}

is discharged. When C_{ds1} is fully charged to the output voltage V_{out}, the free-wheeling diode FWD_2 starts to conduct the inductor current i_L. At the end of the interval 2, SW_2 is turned on at the forward voltage of FWD_2, which is considered as ZVS.

Interval 3 (CCM): During interval 3, the voltage applied to L is negative and i_L decreases linearly. At the end of the interval 2, SW_2 is turned off and the inductor current commutates from FET_2 to FWD_2. This current commutation clamps the voltage of SW_2 to the forward voltage of FWD_2. As a result, the turn-off of SW_2 is considered as ZVS.

Interval 4 (CCM): During interval 4, i_L continues to decrease. As soon as the dead time has passed, SW_1 is turned on. The inductor current i_L commutates from FWD_2 to FET_1 which leads to the forceful turn-off of FWD_2. This results in the high reverse recovery current and the high reverse recovery loss [12]. Note that FET_1 is turned on when C_{ds1} is fully charged at the output voltage V_{out}. Consequently, additional loss coming from the discharge of C_{ds1} occurs.

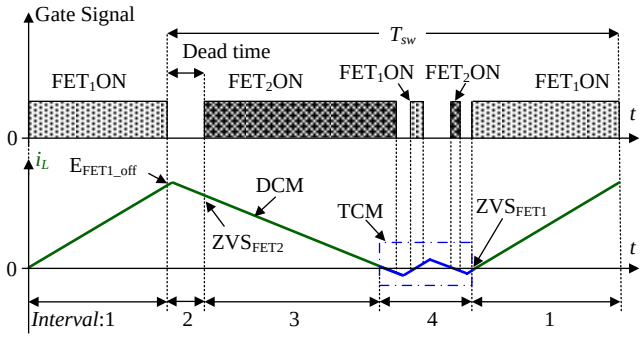


Fig. 3. Hybrid discontinuous current mode between DCM and TCM. By applying TCM during the zero-current interval of DCM, the condition for ZVS is achieved, whereas the current ripple can still be reduced at light load.

On the other hand, the switching period in DCM as depicted in Fig. 2(b) is split into two main intervals and two resonant transitions.

Interval 1 and *Interval* 2 (DCM): these intervals are similar to the intervals in CCM.

Interval 3 (DCM): At the end of interval 3, i_L reaches zero and SW_2 is turned off. Therefore, zero-current switching (ZCS) is achieved.

Interval 4 (DCM): During interval 4, L, C_{ds1}, and C_{ds2} form a resonant circuit which starts to oscillate. The behavior of the oscillation depends on the input to output voltage ratio V_{in}/V_{out} [9]. Due to this oscillation, at the moment when SW_1 is turned on at the end of interval 4, the voltage of C_{ds1} varies from 0V to V_{out} depending on the circuit condition. On the other words, SW_1 can still be turned on under the condition that C_{ds1} is charged and the loss coming from the discharge of C_{ds1} still occurs. Hence, the hard switching still occurs in DCM.

In order to allow for ZVS over entire period, TCM has been proposed [8]-[11]. The switching period in TCM as depicted in Fig. 2(c) is split into two main intervals and two resonant transitions.

Interval 1 and *Interval* 2 (TCM): these intervals are similar to the intervals in CCM.

Interval 3 (TCM): Different from DCM, instead of turning off SW_2 when i_L reaches zero, SW_2 is still kept on in order to let i_L become negative. At the end of interval 3, SW_2 is finally turned off. Consequently, the turn-off loss occurs on SW_2.

Interval 4 (TCM): During interval 4, a switching transition takes place in which C_{ds2} is charged and C_{ds1} is discharged. When C_{ds2} is fully charged, FWD_1 starts to conduct i_L. At the end of the interval 4, SW_1 is turned on at the forward voltage of FWD_1, which is considered as ZVS. Note that TCM is basically similar to CCM but the current ripple in TCM is intentionally designed high enough to let the current become negative in one switching period (cf., Section III) [11].

To conclude, the principle of the ZVS achievement in TCM is to flow a current through the free-wheeling diode before the turn-on of the switches in order to discharge the junction capacitor. Besides, it should be noted that the turn-off loss can be reduced simply by connecting a snubber capacitor in parallel with the switches. A drawback of TCM, however, is a large current ripple which decreases notably the efficiency at light load [8]. Therefore, the current ripple reduction of TCM at light load is desired. In order to reduce the current ripple, one of the conventional methods is to increase the switching frequency at light load, i.e. the Pulse Frequency Modulation (PFM) [9]-[10]. However, PFM is undesirable in many power electronic systems because it is difficult to design a filter circuit for the operation across a wide range of frequencies [13]-[14]. On the other hand, in DCM, because the current ripple becomes smaller at light load, the high efficiency can be maintained [15]. As mentioned above, because DCM still suffers the high turn-on loss, the method to achieve ZVS in DCM is desired. Therefore, this paper proposes the novel concept where TCM and DCM are combined in order to utilize the advantages of these current modes, i.e. ZVS in TCM and the current ripple reduction at light load in DCM.

Figure 3 illustrates the concept of the hybrid discontinuous current mode (HDCM) between DCM and TCM. During the zero-current interval in DCM, i.e. the interval 4 as depicted in Fig. 2(b), instead of letting the current return to zero, the switches are modulated in order to flow the TCM current. Consequently, the condition in order to achieve ZVS in DCM can be satisfied by the TCM current during the interval 4 as shown in Fig. 3. Note that the switching losses during the TCM interval are negligibly small as explained above. Furthermore, because the total charge during the TCM interval can be controlled to become negligibly small, the TCM interval has no effects on the average current which is generated by the DCM interval. On the other words, the current ripple at light load can still be reduced by the DCM operation. As a result, both ZVS and the current ripple reduction at light load are achieved without additional components or the limitation of the duty ratio.

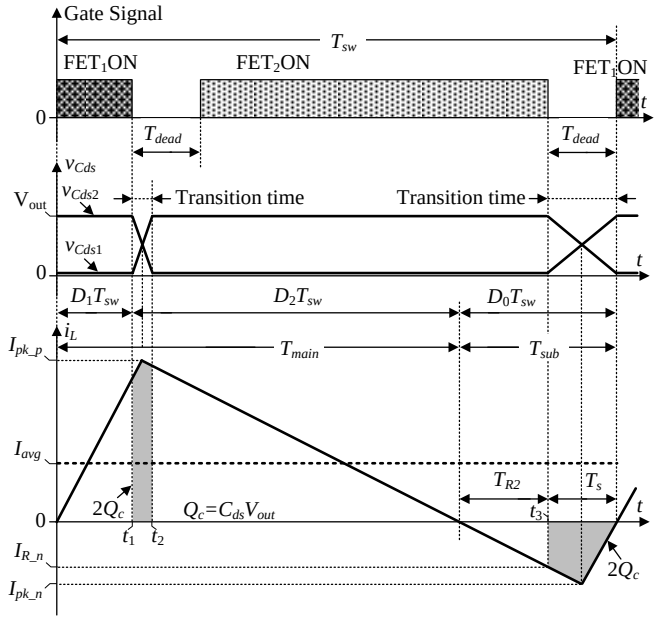


Fig. 4. HDCM operation waveforms of gate signal, junction capacitor voltage and inductor current at rated load in case of $V_{in}>V_{out}/2$. The design of the boost inductance L and the dead time T_{dead} is carried out in TCM which allows for ZVS at rated load.

III. Basic Operation Of Hybrid Discontinuous Current Mode

Based on the mechanism of the switching loss occurrence discussed in Section II, the design and control of the boost converter for HDCM is described in this section. The derivation of the ZVS condition has to be carried out for two cases: $V_{in}>V_{out}/2$ and $V_{in}<V_{out}/2$. However, for the sake of brevity, only the case of $V_{in}>V_{out}/2$ is discussed in the following, whereas the case of $V_{in}<V_{out}/2$ is derived analogously [9].

A. Converter design

Figure 4 depicts the HDCM operation waveforms of the gate signal, the junction capacitor voltage and the inductor current at rated load in case of $V_{in}>V_{out}/2$. HDCM is utilized in order to reduce the current ripple at light load and to allow for ZVS during the complete period. Hence, HDCM basically becomes TCM at rated load.

During the positive-current interval T_{main}, when SW_1 is turned off at t_1, due to the high current peak at rated load, the current is higher than the required positive current I_{R_p} which is the current value satisfying the condition for the ZVS achievement of SW_2. Similarly, the required negative current I_{R_n} stands for the current value which discharges completely C_{ds1}, i.e. one of the conditions for the ZVS achievement of SW_1. Considering the negative-current interval T_{sub}, as soon as FET_2 is turned off at t_3, C_{ds1} and C_{ds2} are connected in parallel. In order to discharge C_{ds1}, the charge Q_c has to be removed and, assuming identical switches, the same charge Q_c is required to charge C_{ds2} to V_{out}. The larger the negative inductor current is, the shorter the transition time becomes. However, this negative current should be minimized in order not to increase the current ripple, which causes excessive conduction loss and decreases the efficiency at rated load. The required negative current I_{R_n} is independent of the output power but only depends on V_{in}, V_{out}, L and the selected switch which defines C_{ds} [9]-[10],

$$I_{R\_n}=\sqrt{\frac{2C_{ds}V_{out}(2V_{in}-V_{out})}{L}} \quad \text{.....(1)}$$

When FET_2 is precisely turned off at the moment i_L reaches I_{R_n}, the resonance between L and C_{ds} continues to flow i_L until it reaches the negative current peak I_{pk_n},

$$I_{pk\_n}=\sqrt{\frac{2C_{ds}V_{out}V_{in}}{L}} \quad \text{.....(2)}$$

Assuming that at rated load, the boost converter transmits the average current I_{avg} to the load over a switching period T_{sw} and also generates the negative current I_{pk_n} for the ZVS achievement, the boost inductance L *and* the dead time T_{dead} which achieve the minimum current ripple are derived as following. First, the positive-curent interval T_{main} and the negative-current interval T_{sub} are geometrically derived from the corresponding peak current I_{pk_p} and I_{pk_n},

$$T_{main}=I_{pk\_p}L\left(\frac{1}{V_{out}-V_{in}}+\frac{1}{V_{in}}\right) \quad \text{.....(3)}$$

$$T_{sub}=I_{pk\_n}L\left(\frac{1}{V_{out}-V_{in}}+\frac{1}{V_{in}}\right) \quad \text{.....(4)}$$

In the boost converter applied with PWM, T_{sw} is constant, whereas I_{avg} is the total charge over T_{sw},

$$T_{sw}=T_{main}+T_{sub} \quad \text{.....(5)}$$

$$I_{avg}=f_{sw}\left(\frac{1}{2}I_{pk\_p}T_{main}-\frac{1}{2}I_{pk\_n}T_{sub}\right) \quad \text{.....(6)}$$

Substituting (3) and (4) into (5) and (6) and solving for the boost inductance L, (7) is obtained.

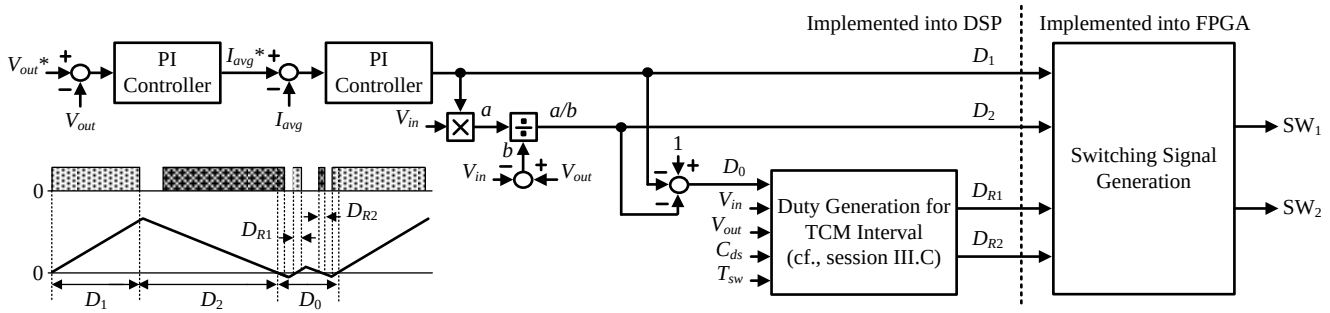


Fig. 5. Control system of boost converter operating in HDCM. A FPGA-based DSP is employed in order to control the boost converter operating in HDCM. Owing to the online calculation of the duty ratios, a real-time closed-loop control of HDCM can be realized.

$$L = \frac{1}{f_{sw}^2\left(\frac{1}{V_{out}-V_{in}}+\frac{1}{V_{in}}\right)^2}\cdot \frac{1}{\left[\sqrt{2C_{ds}V_{out}V_{in}}+\sqrt{2C_{ds}V_{out}V_{in}+\frac{2I_{avg}}{f_{sw}\left(\frac{1}{V_{out}-V_{in}}+\frac{1}{V_{in}}\right)}}\right]^2} \quad (7)$$

Then, the dead time T_{dead} is designed longer than the transition time T_s in order to resonate out completely the charge in the junction capacitor before the switches are turned on,

$$T_s = L\left(\frac{I_{pk\_n}-I_{R\_n}}{V_{out}-V_{in}}+\frac{I_{R\_n}}{V_{in}}\right) \quad \text{.....(8)}$$

To conclude, when the boost converter transmits I_{avg} to the load over T_{sw} at rated load, the condition to achieve ZVS is that L and T_{dead} have to satisfy (7) and (8), respectively.

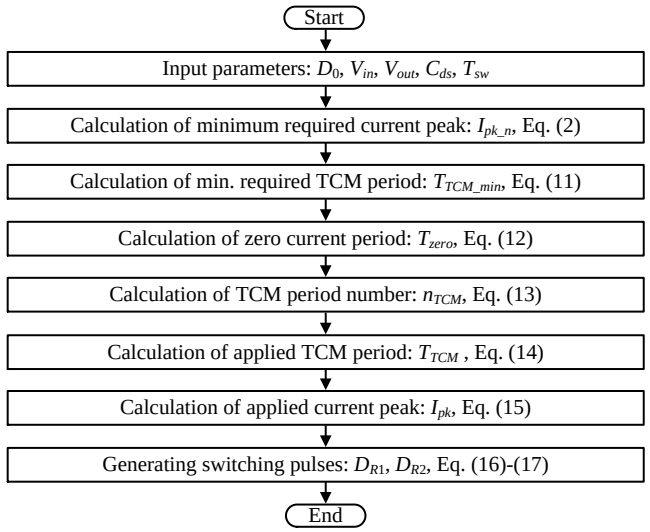


Fig. 6. Flowchart of switching signal generation during TCM interval. Because the TCM current is flown in order to achieve the ZVS condition for DCM, the losses and the charge from the additional TCM current is required to be minimized. Furthermore, it is also necessary to achieve ZVS during the TCM interval.

B. Control system of hybrid discontinuous current mode

Figure 5 depicts the control system of the boost converter operating in HDCM. The voltage and current regulators and the calculation for the duty ratios are implemented into a digital signal processor (DSP), whereas the switching signals are generated by a field-programmable gate array (FPGA) based on the duty ratios received from the DSP. In order to regulate the output voltage V_{out} in response to the line, the load, and the parameter variations, a PI controller is employed into the voltage regulator as a major control loop. The output of the voltage regulator, i.e. the average inductor current I_{avg}*, is then used as a command for the current regulator. Note that the current regulator which is designed in order to deal with the nonlinearity in DCM has been researched thoroughly in [16]-[19]. The current regulator outputs the duty ratio D_1 of the positive-current interval T_{main} as shown in Fig. 4. Based on the relationship between the current slopes during T_{main} [16], the duty ratio D_2 of SW_2 and the duty ratio D_0 of the zero-current interval, i.e. the TCM interval, are estimated as follows,

$$D_2 = D_1\frac{V_{in}}{V_{out}-V_{in}} \quad \text{.....(9)}$$

$$D_0 = 1-D_1-D_2 \quad \text{.....(10)}$$

Then, the following parameters are used to generate the duty ratios D_{R1} and D_{R2} for the TCM interval (cf., Section III.C): the duty ratio D_0, the input voltage V_{in}, the output voltage V_{out}, the junction capacitor value C_{ds}, and the switching period T_{sw}. Finally, the switching signals are generated in the FPGA by comparing the duty ratios D_1, D_2, D_{R1} and D_{R2} with multiple counters. Owing to the online calculation of the duty ratios, a real-time closed-loop control of the proposed current mode (HDCM) can be realized.

C. Duty generation for TCM interval

At light load, the negative current in TCM increases due to the constant switching frequency, which increases the ratio between the current ripple and the average current. Consequently, the efficiency at light load decreases sharply [8], [15]. Therefore, HDCM is applied at light load in order to reduce the current ripple load and to achieve ZVS.

Figure 6 depicts the flowchart of the switching signal generation during the TCM interval in HDCM. It is necessary to control the turn-on period of the switches during the TCM interval as depicted in Fig. 3 so that the following conditions are satisfied;

(i) the TCM interval has no influence on the DCM operation, which implies that the total charge during the TCM interval is required to be negligibly small,

(ii) the ZVS condition for the next DCM period is satisfied, which implies that the current value at the end of the TCM interval is required to be adjusted according to the zero-current interval of DCM by controlling the TCM current peak and the TCM period,

(iii) the losses from the TCM interval such as the conduction loss are minimized, which implies that the TCM current peak is large just enough to achieve ZVS over the TCM interval.

Figure 7 depicts the HDCM operation waveforms of the gate signal, the junction capacitor voltage and the inductor current at light load. Note that only the zero-current interval in which TCM is applied is shown. First, the minimum current peak I_{pk_n} which achieves the condition of ZVS for SW_1 is calculated from the total charge stored Q_c in the junction capacitor C_{ds} as in (2). In order to let the inductor current reach the peak I_{pk_n}, the required TCM period T_{TCM_min} is calculated by (11),

$$T_{TCM\_\min} = I_{pk\_n} L\left(\frac{1}{V_{out}-V_{in}}+\frac{1}{V_{in}}\right) \quad \text{.....(11)}$$

Next, the number of the TCM period n_{TCM} is calculated from the zero-current period T_{zero} as shown in Fig. 6. The zero-current period T_{zero} is calculated from the duty ratio D_0 [16],

$$T_{zero} = D_0 T_{sw} \quad \text{.....(12)}$$

In order to minimize the losses from the TCM interval, the current peak I_{pk} of the TCM current is required to be minimal. Consequently, it is necessary to choose the number of the TCM period n_{TCM} as a maximum odd number,

$$n_{TCM} \le \frac{T_{zero}}{T_{TCM\_\min}}; n_{TCM} \text{ is an odd number.} \quad \text{.....(13)}$$

Next, the applied TCM period T_{TCM} is calculated from the zero-current period T_{zero} and the number of the TCM period n_{TCM},

$$T_{TCM} = \frac{T_{zero}}{n_{TCM}} \quad \text{.....(14)}$$

Then, the applied current peak I_{pk} of the TCM current is calculated as in (15),

$$I_{pk} = \frac{T_{TCM}}{L\left(\frac{1}{V_{out}-V_{in}}+\frac{1}{V_{in}}\right)} \quad \text{.....(15)}$$

Finally, the duty ratios D_{R1} and D_{R2} of SW_1 and SW_2 in order to achieve the TCM current peak I_{pk} is calculated as in (16) and (17), respectively [9],

$$D_{R1} = \frac{L}{f_{sw} V_{in}} \sqrt{I_{pk}^2 - \frac{2C_{ds} V_{out} V_{in}}{L}} \quad \text{.....(16)}$$

$$D_{R2} = \frac{L}{f_{sw}(V_{out}-V_{in})} \sqrt{I_{pk}^2 - \frac{2C_{ds} V_{out}(V_{out}-V_{in})}{L}} \quad \text{..(17)}$$

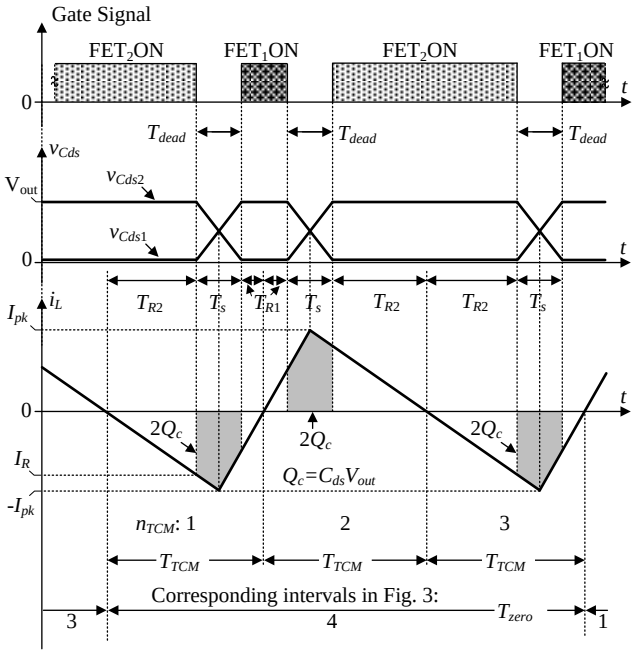


Fig. 7. HDCM operation waveforms of gate signal, junction capacitor voltage and inductor current at light load. In order to achieve ZVS for the DCM operation, the TCM period T_{TCM} is adjusted according to the zero-current period T_{zero}. Furthermore, in order to minimize the losses from the additional TCM current, the current peak I_{pk} is designed to be just large enough to achieve ZVS for both switches SW_1 and SW_2 during the TCM interval. Finally, in order to make the TCM interval has no influence on the DCM operation, which implies the total charge from the additional TCM current is negligibly small, the positive and negative values of the current peak I_{pk} are controlled to become equal.

TABLE I
PARAMETERS OF CIRCUIT AND CONTROLLERS IN EXPERIMENTS.

Symbol	Quantity	Value
V_{in}	Input Voltage	200 V
V_{out}	Output Voltage	350 V
P	Rated Output Power	1 kW
	Experiments for Efficiency Comparison	
	Switching Device	SCH2080KE(ROHM)
L	Boost Inductor Value	70 μH
Δi_H	Current Ripple at Rated Load in TCM, DCM and HDCM	100%
f_{sw1}	Switching Freq. at Rated Load in TCM, DCM and HDCM	100 kHz
f_{sw2}	Maximum Switching Freq. at Light Load in HDCM	300 kHz
Δi_L	Current Ripple at Rated Load in CCM	50%
f_{sw3}	Switching Freq. in CCM	200 kHz
	Experiment for Load Step Response	
C	Output Capacitor Value	360 μF
f_{samp}	Sampling Frequency	25 kHz
f_c	Cutoff frequency (Current Regulator)	500 Hz
ζ_c	Damping factor (Current Regulator)	0.707
f_v	Cutoff frequency (Voltage Regulator)	10 Hz
ζ_v	Damping factor (Voltage Regulator)	0.707

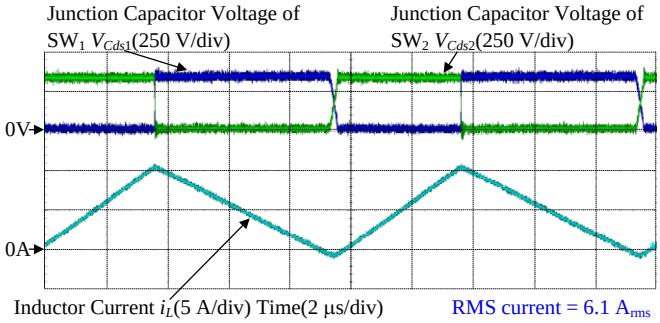
As depicted in Fig. 6, the positive and negative values of the current peak I_{pk} are controlled to be the same, which makes the total charge from the additional TCM current negligibly small. Consequently, the TCM interval has almost no influence on the DCM operation, which implies that the current ripple can be reduced at light load by DCM. Hence, by controlling the TCM current peak during the TCM interval, the proposed current mode (HDCM) both reduces the current ripple load and achieves ZVS.

IV. LABORATORY SETUP

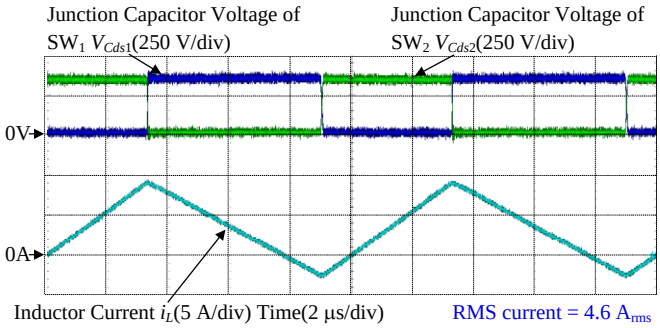
Table I shows the experimental parameters of the circuit and the controllers. A 1-kW prototype is realized with the SiC devices and ferrite core N87. At rated load of 1 kW and the switching frequency of 100 kHz, the inductor value is designed by (7) in order to operate the boost converter in TCM. Consequently, three current modes TCM, DCM, and HDCM share the same operation at rated load. On the other hand, in order to operate the boost converter by CCM under the same condition of the boost inductor, the switching frequency is increased to 200 kHz. As a result, the inductor current ripple of CCM at rated load is reduced by half compared to HDCM. On the other words, in order to achieve the same size of the boost inductor by using CCM with the small inductor current ripple compared to HDCM with the high inductor current ripple, the switching frequency has to be increased.

A. Basic operations of TCM, DCM, HDCM and CCM

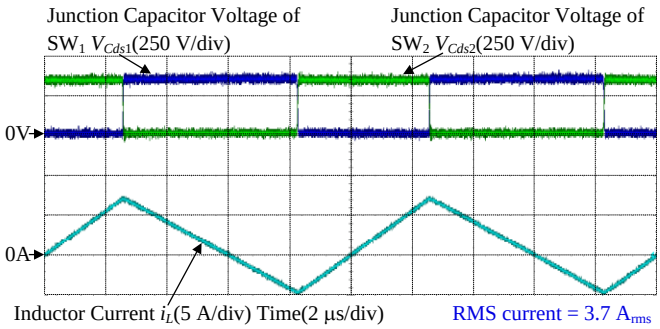
Figure 8-10 depict the waveforms of the TCM, DCM, HDCM and CCM currents, and the junction capacitor voltages under different conditions of load. At rated load, the current waveforms are same for TCM, DCM and HDCM. The current ripple of TCM in Fig. 8 is constant against load. On the other hand, at light load, compared to TCM, the current ripple is greatly reduced by DCM or HDCM. In particular, at light load of 0.2 p.u., the root-mean-square (RMS) current is reduced from 3.7 A_{rms} (TCM) to 1.8 A_{rms} (DCM) or to 2.1 A_{rms} (HDCM). The RMS current of HDCM is slightly higher than that of DCM due to the employment of the TCM current during the zero-current interval. Furthermore, as shown in Fig. 9(c)-(d), the positive and negative values of the TCM current are controlled to be almost the same. Consequently, the addition TCM current has no effects on the DCM operation. This allows the conventional DCM current control to be applied simply to HDCM [16]-[19]. As shown in Fig. 10, by increasing the switching frequency from 100 kHz to 200 kHz, the boost converter is operated in CCM at rated load. Compared to TCM, the smaller RMS current is achieved in CCM owing to the increase in the switching frequency.



(a) TCM current and junction capacitor voltages at rated load.

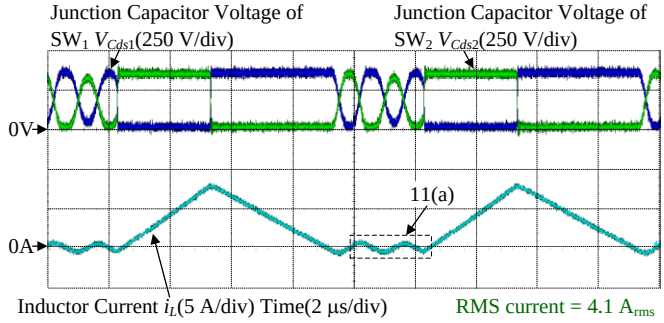


(b) TCM current and junction capacitor voltages at light load of 0.6 p.u.

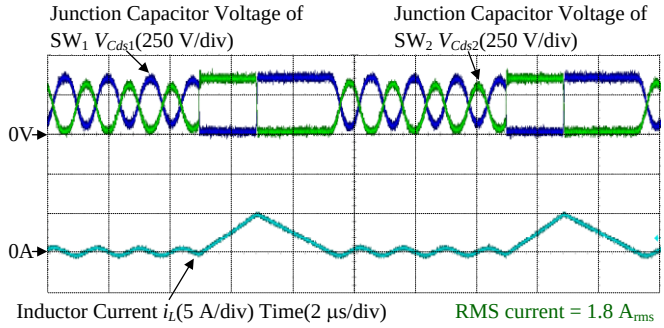


(c) TCM current and junction capacitor voltages at light load of 0.2 p.u..

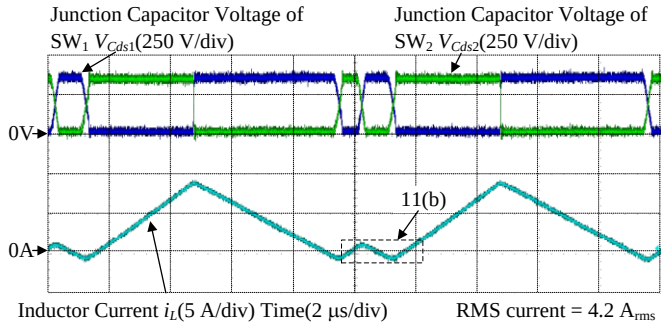
Fig. 8. Waveforms of TCM current and junction capacitor voltages under different conditions of load.



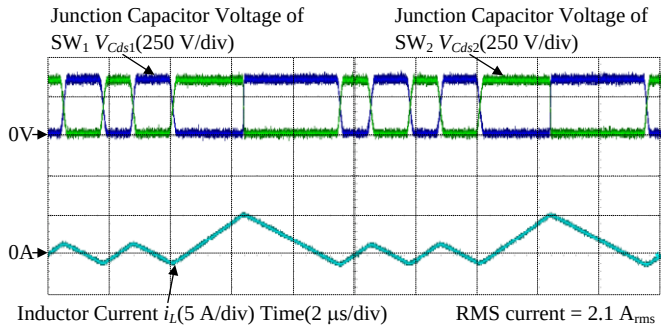
(a) DCM current and junction capacitor voltages at light load of 0.6 p.u.



(b) DCM current and junction capacitor voltages at light load of 0.2 p.u.



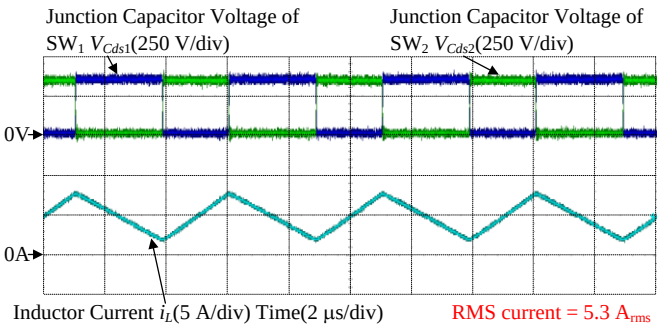
(c) HDCM current and junction capacitor voltages at light load of 0.6 p.u.



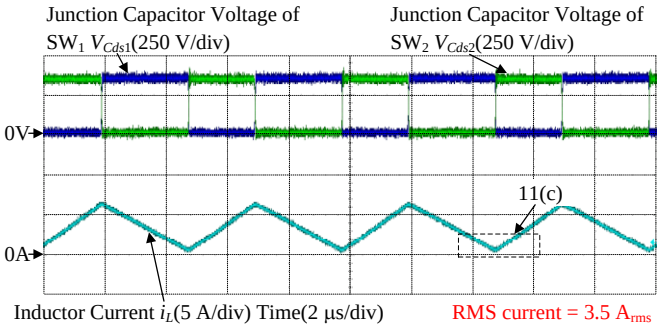
(d) HDCM current and junction capacitor voltages at light load of 0.2 p.u.

Fig. 9. Waveforms of DCM and HDCM currents, and junction capacitor voltages under different conditions of load.

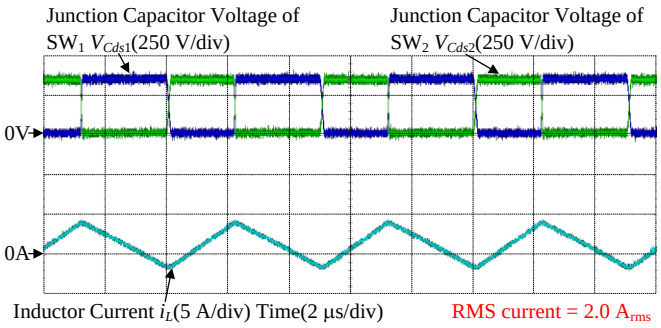
Figure 11 illustrates the waveforms of the gate signal and the junction capacitor voltage, which is the magnified waveforms from Fig. 9(a), 9(c), and 10(b). As explained in Fig. 2(b), the hard switching can still occur in DCM. The switching behavior and the switching loss of DCM depends on the resonance between the boost inductor and the junction capacitors during the zero-current interval. On the other hand, it is confirmed in Fig. 11(b) that both the switches SW_1 and SW_2 are turned on at the zero voltage, i.e. ZVS. Furthermore, the turn-off losses can be simply reduced by connecting a snubber capacitor parallel to the switch in order to delay the rise of the junction voltage. Consequently, low switching loss can be accomplished in order to further increase the switching frequency and to achieve the high power density. In Fig. 11(c), the occurrence of the hard switching is confirmed in CCM similarly to DCM. The hard switching in DCM and CCM not only generates high switching loss but also distorts the gate signal due to the high di/dt of the discharge current from the junction capacitor. The gate signal distortion can lead to the occurrence of the false triggering in CCM and DCM. In order to avoid the occurrence of the false triggering during hard switching in CCM and DCM, the main circuit and the gate driver circuit are required to be customized for the high di/dt of the current, which is undesirable due to the increase in cost. On the other words, the soft switching in HDCM not only reduces the switching loss but also benefits the design cost of the main circuit and the gate driver circuit.



(a) CCM current and junction capacitor voltages at rated load.

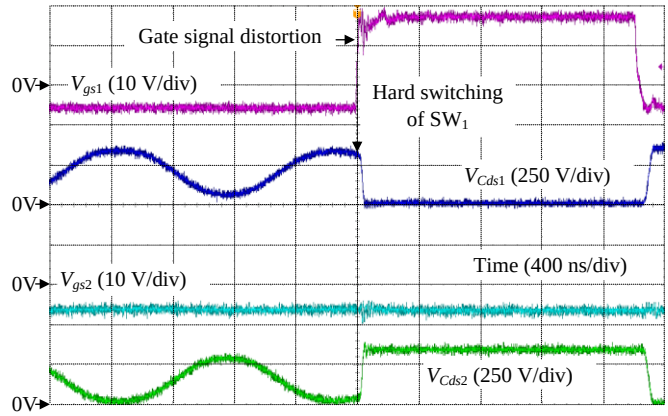


(b) CCM current and junction capacitor voltages at light load of 0.6 p.u.

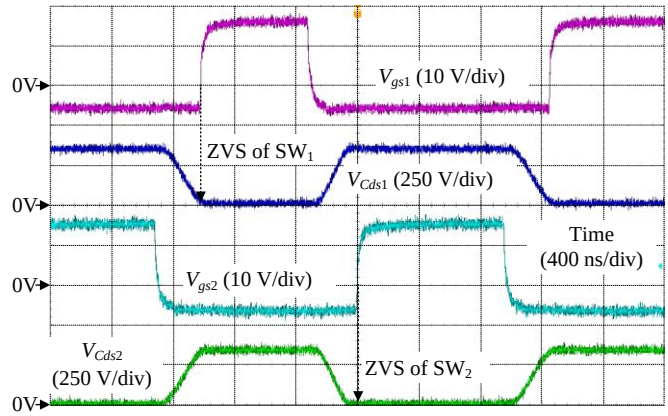


(c) CCM current and junction capacitor voltages at light load of 0.2 p.u..

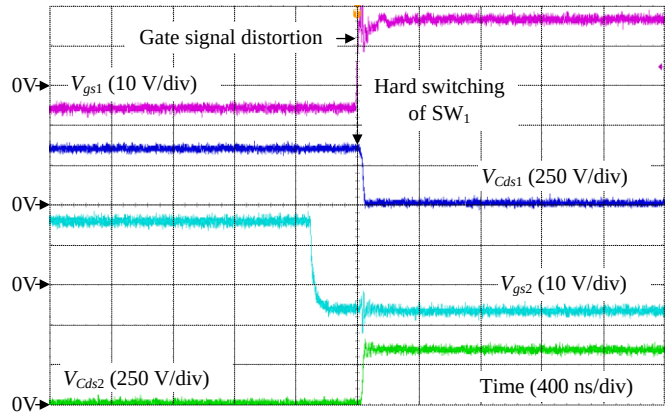
Fig. 10. Waveforms of CCM current and junction capacitor voltages under different conditions of load.



(a) Hard switching in DCM.



(b) Soft switching in HDCM.



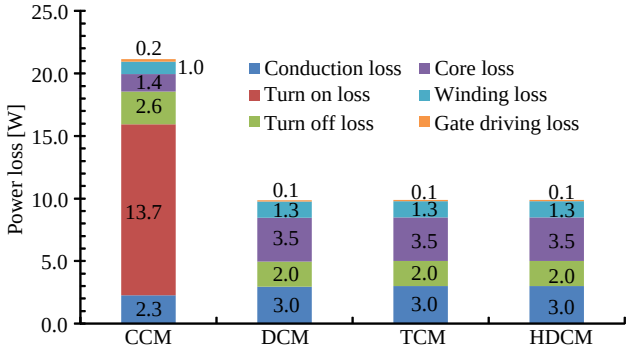
(c) Hard switching in CCM.

Fig. 11. Waveforms of gate signal and junction capacitor voltage in DCM, HDCM and CCM which is the magnified waveforms from Fig. 9(a), 9(c), and 10(b).

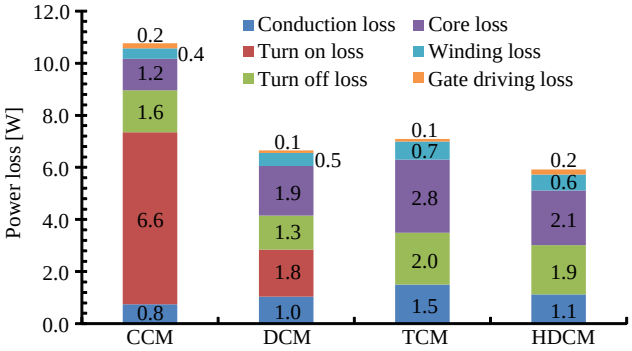
B. Comparisons of RMS current and efficiency among four current modes

Figure 12 shows the comparisons of RMS current and efficiency among TCM, DCM, HDCM and CCM. Note that the same boost inductor is used to conduct the experiments of the efficiency comparison. First, as shown in the results of the ratio between the RMS current I_{L_rms} and the average current I_{avg}, by utilizing the variable current-ripple characteristic of DCM, the RMS current in HDCM is reduced greatly compared to TCM. In particular, at light load of 0.1 p.u., the RMS current of HDCM is reduced by 56.6%. Besides, the RMS current of HDCM at rated load is as same as that in TCM, because the converter is designed to be operated with TCM at rated load. This design minimizes the required current ripple in order to achieve ZVS at rated load. Consequently, the efficiency of HDCM at rated load is as same as that in TCM, whereas at light load, the efficiency is improved up to 3.1% with HDCM. On the other hand, the RMS current of HDCM is slightly higher than that of DCM due to the employment of the TCM current during the zero-current interval. However, the efficiency of HDCM is higher than that of DCM over entire load range because the hard switching still occurs in DCM. Note that the variation of the DCM efficiency is quite large because the turn-on loss of the hard switching in DCM depends on the zero-current interval which changes according to load. Finally, the efficiency of CCM shows a sharp decline around load of 0.5 p.u. because the boost converter changes the current mode from TCM to CCM as shown in Fig. 10 (b)-(c). By applying HDCM, the efficiency at rated load is improved by 0.9% compared to CCM.

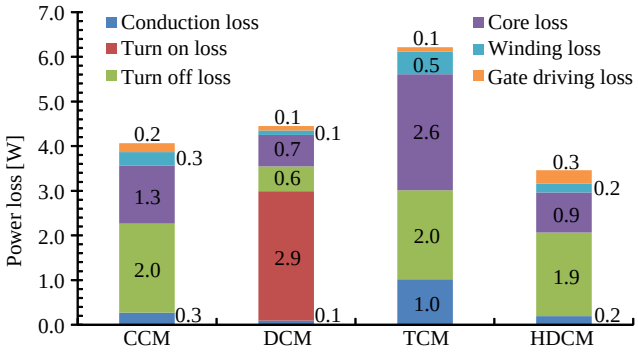
Figure 13 shows the loss distribution of four current modes under different conditions of load. The conduction losses and the switching losses are obtained from the simulator, i.e. PLECS, whereas the core losses and the winding losses are obtained from the inductor modeling software entitled GeckoMAGNETICS. As shown in Fig. 13(a), the turn-on loss in CCM is dominant and this greatly reduces the efficiency at rated load. The turn-on loss in DCM varies largely depending on the zero-current interval which changes according to load and the other conditions of the circuit such as the input and output voltage. On the other hand, as shown in Fig. 13 (c), the high conduction loss and inductor loss still occur in TCM even at light load due to the constant current ripple. The losses from the high current ripple in TCM at light load can be reduced by applying HDCM. This efficiency improvement at light load is specially desired in the photovoltaic system, where the most frequent operating range locates at light load. Note that the increase in the gate driving loss when applying HDCM is negligibly small compared to the reduction of the other losses.



(a) Loss distribution at rated load.

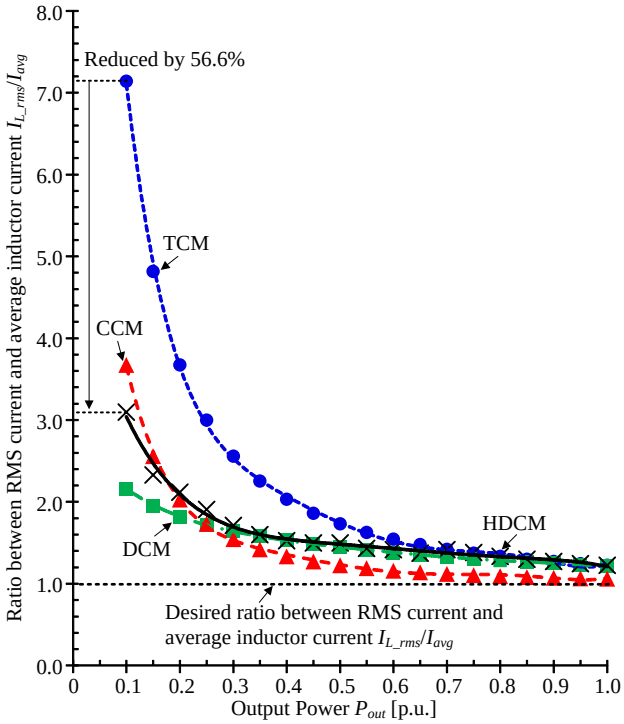


(b) Loss distribution at load of 0.5 p.u..

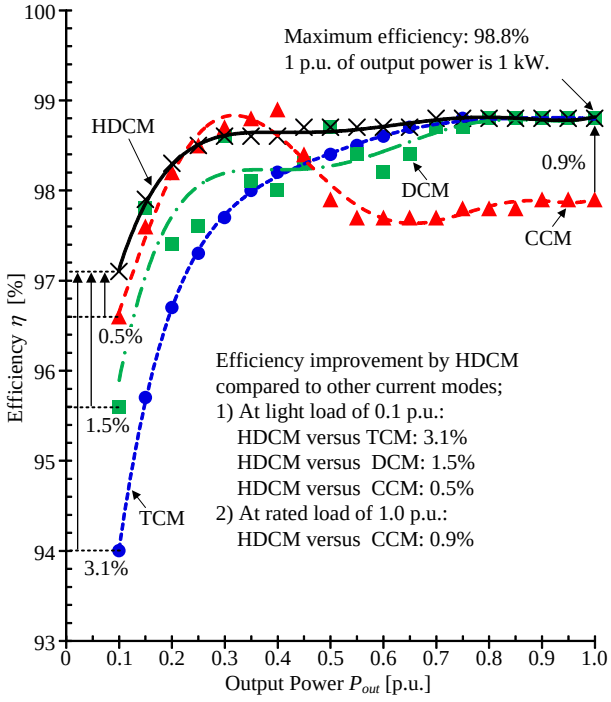


(c) Loss distribution at load of 0.1 p.u..

Fig. 13. Loss distribution of four current modes under different conditions of load. In the SiC device, the turn-on switching loss is dominant due to the reverse recovery charge or the junction capacitor charge of the free-wheeling device at hard-switching condition. Therefore, it is crucial to eliminate the turn-on switching loss in order to increase the switching frequency and still maintain the high efficiency.



(a) Ratio between RMS current and average current.



(b) Efficiency characteristic.

Fig. 12. Comparison of RMS current and efficiency among TCM, DCM, HDCM and CCM.

C. Average current ripple reduction and Output voltage regulation

Figure 14 describes the theoretical and actual DCM currents. At t_1, when both the switches SW_1 and SW_2 are turned off, the theoretical DCM current remains zero until t_2. However, due to the resonance between the boost inductor and the junction capacitors, a current flows during the interval from t_1 to t_2. At t_2,

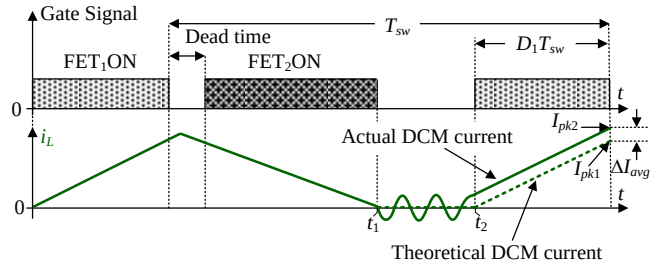
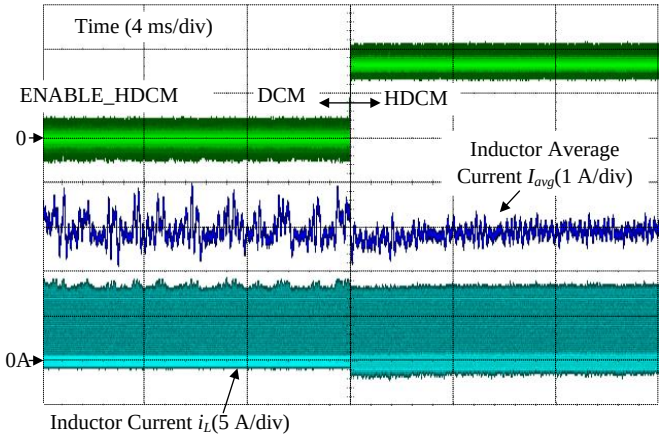
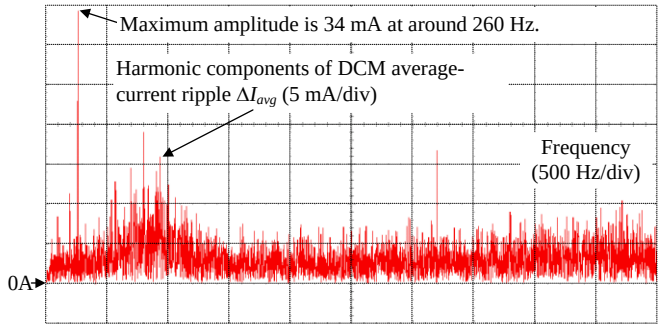


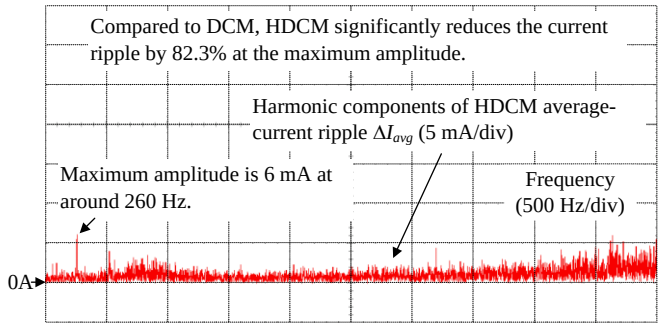
Fig. 14. Theoretical and actual DCM currents. Due to the resonance between the boost inductor and the junction capacitors, the high average-current ripple occurs in DCM. Consequently, the minimization of the boost inductor in DCM suffers this high average-current ripple.



(a) Average current when the current mode is changed from DCM to HDCM at load of 0.6 p.u..



(b) Harmonic analysis results of DCM average-current ripple.

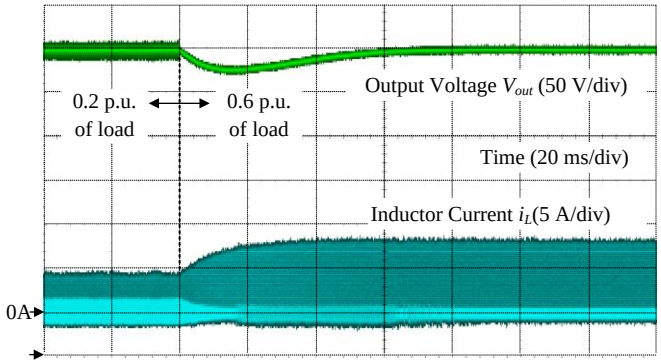


(c) Harmonic analysis results of HDCM average-current ripple.

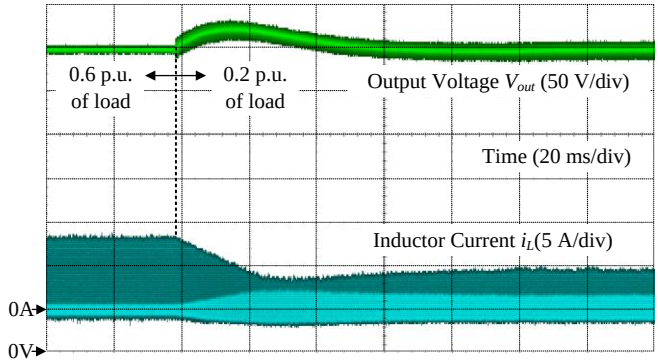
Fig. 15. Average-current ripple reduction by applying HDCM. The high average-current ripple occurring in DCM worsens the maximum power point tracking in the photovoltaic system. By applying HDCM, the average-current ripple can be reduced greatly. This enables the minimization of the boost inductor.

the theoretical DCM current starts to rise from 0A and reaches the current peak I_{pk1} after the turn-on interval D_1T_{sw} of SW_1, whereas the actual DCM current reaches the current peak I_{pk2}. The difference between I_{pk1} and I_{pk2} results in the average-current ripple ΔI_{avg}. On the other words, the current flowing during t_1 and t_2 acts as a disturbance to the current regulator. Furthermore, the amplitude of the current flowing during t_1 and t_2 is inversely proportional to the boost inductor value. This relationship has been researched thoroughly in [20]. Consequently, the minimization of the boost inductor in DCM suffers the high average-current ripple. On the other hand, the TCM current in HDCM is controlled in order to let the current return to zero before the next switching period (cf., Section III). Therefore, the average-current ripple can be reduced by the employment of HDCM.

Figure 15 depicts the experimental results of the average-current ripple reduction by applying HDCM. When the signal of ENABLE_HDCM becomes high, the current mode changes from DCM to HDCM. The reduction of the average-current ripple by applying HDCM can be observed from Fig. 15(a). Then, the harmonic analysis of the average-current ripple in DCM and HDCM is conducted and the results are shown in Fig. 15(b)-(c), respectively. As observed from Fig. 15(b), the average-current ripple in DCM consists of many low-frequency harmonic components, one of which has the maximum amplitude of 34 mA around 260 Hz. The average-current ripple in DCM decreases the efficiency of the photovoltaic system, because the maximum power point tracking is decayed with this average-current ripple. Furthermore, a large input filter which has a low cut-off frequency is required if the average-current ripple in DCM has to be filtered out, because the harmonic components of the average current ripple in DCM occur in the low frequencies. This problem restricts the minimization of the boost inductor by DCM. The average-current ripple in DCM can also be reduced by damping the resonance between the boost inductor and the junction capacitors. This can be accomplished by employing a snubber circuit connected parallel to the switching devices. However, the snubber circuit not only increases the switching loss as shown in Table I in [20], but also restricts the minimization of the boost converter. On the other hand, as observed from Fig. 15(c), the harmonic components of the average-current ripple are greatly reduced by applying HDCM. In particular, compared to DCM, the maximum amplitude of the harmonic components is reduced by 82.3%. Note that the small average-current ripple still occurs in HDCM due to the limited resolution of the counter in the FPGA which is generated by a clock frequency of 200 MHz. This causes the TCM current cannot exactly return to zero before the next switching period. This problem can be alleviated by increasing the clock frequency of the FPGA.



(a) Load step change: 0.2 p.u. to 0.6 p.u..



(b) Load step change: 0.6 p.u. to 0.2 p.u..

Fig. 16. Load transient response by output voltage control with 10 Hz cutoff frequency. The overshoot voltage and the settling time are 28 V and 56 ms, the errors of which compared to the designed values are 3.6% and 1.8%, respectively [18].

Figure 16 shows the load transient response obtained in experiment by the output voltage control with 10-Hz cutoff frequency. The test is conducted with a load current step from 0.2 p.u. to 0.6 p.u. and vice versa. The overshoot voltage and the settling time are 28 V and 56 ms, the errors of which compared to the designed values are 3.6% and 1.8%, respectively. The stability of the voltage control in HDCM is similar to that in DCM because the online calculation of the duty ratios is employed and the TCM current is controlled to have no influence on the DCM operation. Consequently, this confirms that the real-time closed-loop control of HDCM can be realized as same as DCM. Furthermore, the duty generation for the TCM interval can be carried out with a margin considering the element tolerances, whereas the feedback control ensures the stable operation of HDCM.

V. Conclusion

This paper presented a hybrid current mode between TCM and DCM in order to improve the wide-load-range efficiency for the high-frequency SiC-based boost converter. In the proposed current mode entitled HDCM, ZVS was achieved without any additional components as same as the conventional TCM. Consequently, the high power density design was accomplished by using the SiC devices at high switching frequency. The advantages of HDCM were compared to the other current modes; i.e. TCM, CCM, DCM.

First, in TCM, the constant current ripple decreased significantly the efficiency at light load. Therefore, HDCM in which TCM was applied during the zero-current interval of DCM, was introduced in order to reduce the current ripple and to allow for

ZVS over entire switching period. As a result, under the condition of the same boost inductor, the efficiency of HDCM at light load of 0.1 p.u. was improved by 3.1% compared to TCM.

Second, in order to operate the boost converter by CCM under the same condition of the boost inductor, the switching frequency was increased from 100 kHz to 200 kHz. As a result, the inductor current ripple of CCM at rated load was reduced by half compared to HDCM. In CCM, the hard switching occurred due to the discharge of the reverse recovery charge and the junction capacitor charge. Therefore, the efficiency of CCM at rated load was lower by 0.9% compared to HDCM. Furthermore, the hard switching in CCM not only generated high switching loss but also distorted the gate signal due to the high di/dt of the discharge current from the junction capacitor. The gate signal distortion can lead to the occurrence of the false triggering in CCM. In order to avoid the occurrence of the false triggering during hard switching in CCM, the main circuit and the gate driver circuit are required to be customized for the high di/dt of the current, which is undesirable due to the increase in cost. On the other words, the soft switching in HDCM not only reduced the switching loss but also benefitted the design cost of the main circuit and the gate driver circuit.

Finally, the hard switching in DCM can still occur depending on load. Therefore, the efficiency of HDCM was improved by 1.5% at most compared to DCM. Furthermore, due to the resonance between the boost inductor and the junction capacitors, a current flew during the interval when both the switches are turned off. This current was the reason of the difference between the theoretical and actual DCM currents, which generated the average-current ripple. The average-current ripple in DCM decreased the efficiency of the photovoltaic system, because the maximum power point tracking was decayed with this average-current ripple. On the other hand, the TCM current in HDCM was controlled in order to let the current return to zero before the next switching period. Therefore, the average-current ripple could be reduced by the employment of HDCM. As a result, compared to DCM, the maximum amplitude of the harmonic components in the HDCM average-current ripple was reduced up to 82.3%.

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