High Power Density Design for a Modular Multilevel Converter with an H-bridge Cell based on a Volume Evaluation of Each Component

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***Abstract*— This paper presents a high power density design for a step-down rectifier incorporating a modular multilevel converter (MMC) in a power system connected to a 6.6 kV AC grid. In particular, the relationship among the number of cells, the output voltage of the MMC and the overall volume is clarified. A proposed design flowchart focuses on minimizing volumes of cell capacitors, heat sinks and arm inductors by using optimal number of cells. Moreover, the commercial electrolytic capacitors are used as the cell capacitor. Besides, the formulae used to determine the ripple currents in the electrolytic capacitor and the arm inductor are presented, along with that for the semiconductor loss. Each of these formulae were verified experimentally using a miniature model and theoretical values from all formulae agree with the measured values within minimal deviations that are discussed with regard to the design of a practical converter for a 6.6 kV system. Finally, the conditions necessary to achieve high power density in an MMC are provided, based on volume evaluations of the electrolytic capacitor, the arm inductor and the heat sink. Using this optimization process, an MMC design achieved a volume reduction of approximately 90% compared to a conventional system.**

***Index Terms*— Modular multilevel converter, Pareto front, High power density design, H-bridge cell, Step-down rectifier**

I. Introduction

Recently, DC micro-grids have been actively researched as next generation power distribution system [1]-[6]. In DC micro-grids which have been considered so far, a power system which is connected to an AC power grid has the isolation transformer in order to convert 6.6 kV to several hundred volts [5]. However, the isolation transformer operating at a commercial frequency is bulky. In addition, bulky static capacitors for power factor correction as well as series reactors for reduction of the harmonic distortion of the grid current are also requires in the above system [7].

In order to avoid the utilization of the bulky transformer, the neutral-point-clamped (NPC) converter or the diode-clamped converter has been researched [8]. In the three-level diode-clamped converter, the high voltage IGBTs with the voltage rating more than 6.5 kV are required. However, it is generally difficult to employ the IGBTs with the voltage rating more than 6.5 kV due to their specifications. Moreover, if the five-level diode-clamped converter is applied to solve the problem with the switching devices, the voltage balancing circuit is required as the auxiliary circuit in order to correct the unbalanced voltage among four capacitors in the DC link. Besides, the switching frequency cannot be set more than several kilohertz because the switching loss is large in the high voltage switching device which is applied to the three-level or the five-level diode-clamped converter. As a result, the volume of the interconnected inductor is bulky. In addition, the both converters cannot achieve step-down rectification. Thus, the specification of the NPC converter are different from the requirements of the proposed system.

On the other hand, a modular multilevel converter (MMC) has been actively researched as next generation high voltage power converters that does not require a bulky transformer [9]-[16]. In particular, an H-bridge cell type MMC is suitable for use as the front-end converter in a DC micro-grid in terms of volume reduction and step-down rectification from 6.6 kV AC voltage to several hundred volts of DC voltage [17]-[18].

In many AC-DC converters incorporating MMC topology, high power density is obtained by careful consideration of the volume and by setting specific design criteria [19]-[25]. However, the criteria necessary to reduce the overall volumes of (i) capacitors, (ii) heat sinks and (iii) arm inductors in the design of a step-down rectifier with an H-bridge cell type MMC have not yet been reported in detail.

Firstly, evaluations of the correlations between capacitor volume, the capacitance and electrostatic energy of the device have been reported [26]-[28]. Volumes of various capacitors such as customized film or ceramic with a fixed number of cells have been also shown [28]-[29]. However, the relationship between the number of cells and the capacitor volume has not been thoroughly considered. Additionally, it is difficult to compare the volumes of the above capacitors in a practical manner because film or ceramic capacitors are customized with varying numbers of cells according to desired performance parameters. On the other hand, an electrolytic capacitor has the useful feature such as high capacitance per unit volume or the voltage rating of several hundred volts. In addition, it is easy to consider and design the capacitor volume when electrolytic capacitors are applied to the MMC because cell capacitors can be designed based on data of commercial electrolytic capacitors.

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In contrast, the lifetime of the electrolytic capacitor is short compared to film or ceramic capacitors as the drawback. However, electrolytic capacitors are widely applied to many power converters such as grid-tied inverters or PWM rectifiers after the lifetime of the electrolytic capacitors is considered carefully. Besides, in the prototype of the MMC for the medium voltage grid or the miniature model, electrolytic capacitors are also applied [30]-[36]. These examples show the usability of electrolytic capacitors. Thus, it is very important to consider the use of electrolytic capacitors including the lifespan in order to promote the discussion for the cell capacitor design. However, not only the design method of electrolytic capacitors in the MMC but also volume comparisons of electrolytic capacitors, film capacitors or ceramic capacitors have not been discussed.

Secondly, as the heat sink design, the calculation of the semiconductor loss have been reported [37]-[40]. In addition, heat sink volumes have been evaluated when insulated gate bipolar transistors (IGBTs) with voltage rating from 600 V to 6.5 kV were applied [41]. Despite this, the relationship among the number of cells, the output voltage of the MMC and the heat sink volume has not been considered. As the output voltage is varied, both the capacitor voltage and the circulating current will change, even at a same power rating. Moreover, the capacitor voltage is also changed by varying the number of cells. Thus, the semiconductor loss varies drastically because the voltage rating and the rated current of the switching device are modified by the capacitor voltage and circulating current. Besides, the switching loss changes based on the number of cells because the switching frequency is determined by the equivalent frequency which is affected by the number of cells. Hence, the relationship among the number of cells, the output voltage of the MMC and the heat sink volume has to be clarified in order to achieve minimization of the heat sink volume.

Thirdly, with regard to the arm inductor volume, the inductance has been determined to be several percent of the impedance rating of the MMC [42]-[44]. In addition, design criteria that focus on the harmonic components of the circulating current and the resonance phenomenon between the arm inductor and the capacitors in cells have also been discussed [45]-[46]. In the case of the inductor in a general power converter, the inductance is determined based on the ripple factor of the inductor current [47]-[49]. In an MMC, the magnitude and the frequency of the ripple current will change in response to the switching frequency and the number of cells because these factors vary the equivalent switching frequency. As well, the inductor current includes the circulating current, which changes based on the output voltage of the MMC. Thus, the ripple current factor varies even when the magnitude and the frequency of the ripple current are constant. However, the relationship among the number of cells, the output voltage of the MMC and the arm inductor volume has not been considered. In particular, the total volume of the heat sink and the arm inductor has to be considered because the semiconductor loss also changes when the number of cells or the output voltage varies.

As a problem of the conventional design method for the MMC, the relationship among the number of cells, the output voltage of the MMC and the overall volume has not been considered, although the design criteria for each component have been assessed independently. However, it is required to clarify the above relationship in order to obtain high power density. In particular, the parameters that are significantly affected by the number of cells and the output voltage of the MMC are: (i) the voltage rating, the current rating and the switching frequency of the switching device, (ii) the voltage rating and the rated ripple current of the electrolytic capacitor and (iii) the inductance of the arm inductor. Hence, the volume of the MMC is changed by variations in the required parameters of these components.

This paper proposes the design criteria in order to obtain high power density in the H-bridge cell type MMC. In particular, the main aim of this paper is to clarify the conditions based on the number of cells and the output voltage of the MMC for achieving the volume reduction of the cell capacitor, the heat sink and the arm inductor. The original contribution of this paper is to determine the number of cells associated with the smallest possible overall MMC volume based on the evaluation of the relationship among each component volume, the number of cells and the output voltage. Moreover, the validity of formulae for the design are verified by the experiment.

As a first step, a design flowchart was proposed to achieve the highest possible power density. Secondly, in the design of the electrolytic capacitor focusing on lifespan and the voltage rating, the number of parallel connection and the number of series connection are determined for the volume reduction. Besides, the relationship between the electrolytic capacitor volume, the rated ripple current and the voltage rating are evaluated. In addition, the relationship between the number of cells and the electrolytic capacitor volume was also clarified. Thirdly, the heat sink volume was evaluated by calculating the conduction and the switching losses of the switching devices. Fourthly, as the arm inductor design, a formula of the ripple current was derived in order to determine the inductance based on the ripple current factor. Finally, the relationship among the number of cells, the output voltage of the MMC and the volume of the electrolytic capacitor was clarified. In addition, the relationship between the number of cells, the output voltage of the MMC and the total volume of the arm inductor and the heat sink was evaluated by Pareto front optimization [50]. The above evaluations generates design criteria that reduce the overall volume of the MMC. As a result, the overall volume of the capacitors, heat sinks and arm inductors in an H-bridge cell type MMC equals to equal 10% of the overall volume of a conventional power system including an isolated transformer, static capacitors and a series reactor.

II. Circuit Configuration and Control Strategy

A. Conventional Power System Connected to a Utility Grid

Fig. 1 shows the structure of a conventional 200 kVA power system connected to a 6.6 kV AC power grid [7]. This conventional system has isolated transformers to convert the grid voltage of 6.6 kV into an AC distribution voltage of 200 or

100 V. The power system also includes static capacitors to correct the input power factor and a series reactor to reduce the harmonic distortion of the grid current. The component volume, defined as the total volume of the transformers, static capacitors and the series reactor, is 1605 dm^3, i.e. the main factors that increase the system volume.

B. Front-end Converter with MMC and Isolated DC-DC Converter

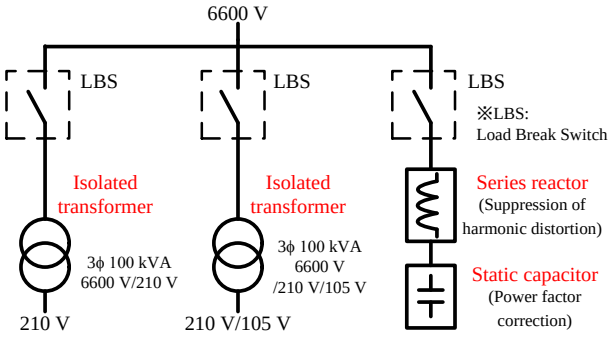
Fig. 2 presents the configuration of the front-end converter using an H-bridge cell type MMC. Each arm of the MMC that operates as the step-down rectifier consists of an arm inductor, L_a, and H-bridge cells [17]. Because the MMC is able to reduce the voltage rating of the devices on each cell due to the cascade cell connections. Therefore, lower voltage switching devices can be utilized with the MMC. The output DC voltage of the MMC, V_{mmc}, depends on the sum of the output average voltages of cells per leg, meaning that the cell output voltage includes both AC and DC components to control the input current and the output voltage. Besides, the arm current such as i_{Ar} or i_{Br} also includes both AC and DC components. The MMC first converts a high AC voltage to a DC voltage of several hundred volts, then 400 V DC is supplied to the DC bus of the DC distribution by the isolated DC-DC converter, which also provides the isolation between the AC power grid and the DC micro-grid. Hence, the high step-down from 6.6 kV to several hundred volts is accomplished by the operations of both the MMC and the isolated DC-DC converter. Thus, the output voltage rating of the MMC can be designed with a high degree of freedom. Moreover, the DC component of the arm current which flows from each leg to the output side of the MMC can be changed based on the output voltage of the MMC, V_{mmc} even at a same power rating. The ripple current of the cell capacitor or the semiconductor loss changes according to the variation of the DC component. Thus, it is necessary to employ a variety of combinations of the output voltage and the circulating current to reduce volumes of the MMC and the isolated DC-DC converter.

C. Control Strategy for the Step-Down MMC

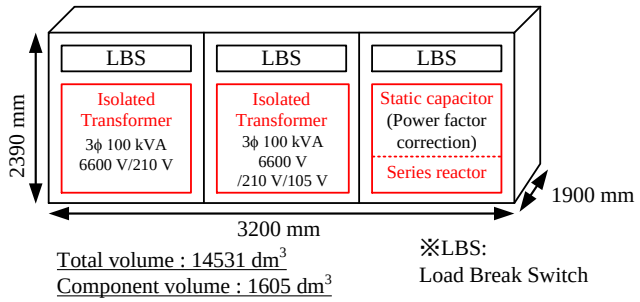
Fig. 3 shows a control block diagram of the step-down rectifier with an H-bridge cell type MMC [18]. The control block is constructed by an averaging voltage control, an arm current control, an output voltage control and a voltage balancing control. In the proposed voltage balancing control, the output DC voltage of each cell is varied depending on the capacitor voltage [36]. The advantage of the proposed voltage balancing control system is that it is not necessary to design control parameters because the dividing ratio is adjusted automatically depending on the capacitor voltage.

III. Design Flowchart for a Step-down Rectifier with MMC Topology

Fig. 4 presents a flowchart summarizing the design of the step-down rectifier with MMC. The flowchart is divided into three parts: the capacitor, the arm inductor and the heat sink. The efficiency and power density of the converter are shown as



(a) Circuit configuration of conventional system



(b) Volume of conventional system

Fig. 1. Conventional power system of 200 kVA connected to utility gird of 6.6 kV. The conventional power system is constructed of several bulky transformers, a high capacity static capacitor and a series reactor.

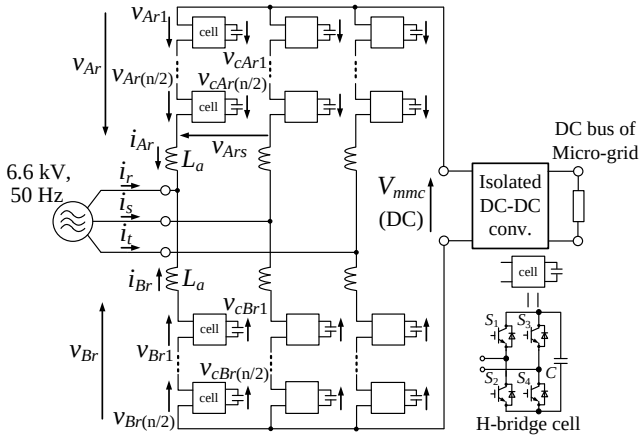


Fig. 2. Circuit configuration of front-end converter with H-bridge cell type MMC and isolated DC-DC converter.

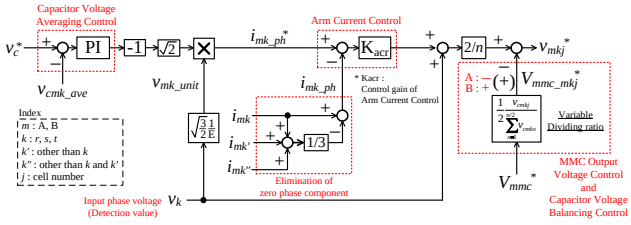


Fig. 3. Control block diagram for each arm in H-bridge cell type MMC. Note that *m* is the index of the arm group A or B, *k*, *k´* or *k´´* is the index of the phase such as *r*, *s* and *t*, and *j* is the index of the cell number.

outputs. The purpose of this work is to miniaturize the converter, and so it is necessary to determine the design parameters associated with obtaining high power density. In

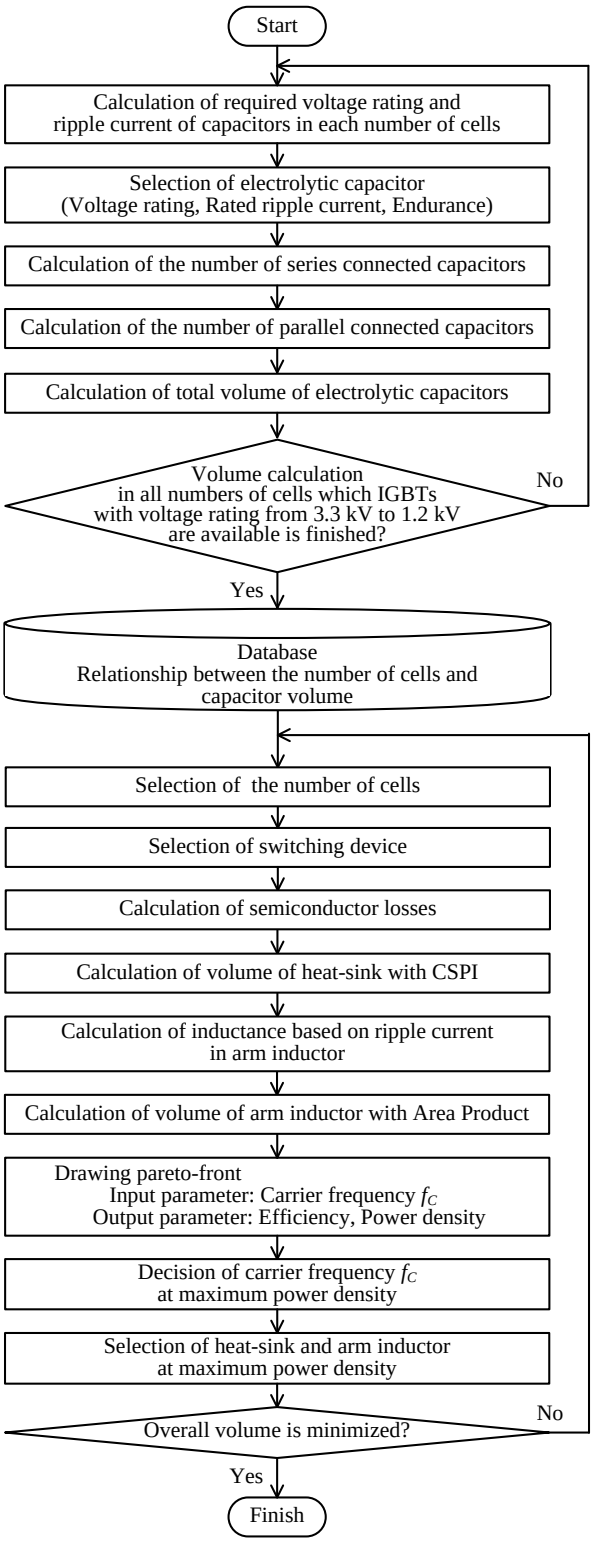


Fig. 4. Design flowchart for a step-down rectifier with MMC.

particular, the carrier frequency and the number of cells at which the overall volume of the capacitor, the heat sink and the inductor are minimized is determined.

In the capacitor design, the ripple current and the voltage rating are calculated from the MMC output voltage and the power rating. A capacitor having a low rated ripple current is advisable in order to reduce the capacitor volume. The number of parallel connected capacitors increases when a capacitor with a low rated ripple current is employed. However, when a low rated ripple current capacitor is selected, the capacitor volume is small compared to that of device with a high rated ripple current. When considering the voltage rating, a capacitor for which the voltage rating per single capacitor is over 400 V should be selected. The number of series connected capacitors varies from two to three when a 1.7 or 1.2 kV IGBT is applied to the converter. When the number of series connected capacitors is greater than this, a balancing resistance is required for each capacitor and so the volume increases. From the above, the quantity of series connected capacitors is optimized based on the desired voltage rating, while the number of parallel capacitors is chosen by considering the ripple current and the lifespan of the device. The capacitor volume is calculated from the number of series connections, the number of parallel connections and the cell quantity. The capacitor volume associated with each cell quantity is stored in database. In the case of high power converter, IGBTs with voltage rating from 1.2 to 3.3 kV are generally applied, and so it is particularly important to store the relationship between the volume and the number of cells when using IGBTs with voltage ratings in this range. It is possible to reduce the capacitor volume by varying the number of cells when the voltage rating ratio is high. This is defined as the ratio of the required voltage rating to the voltage rating with the series connected capacitors, and is calculated using equation (1). A high ratio implies that the capacitor is utilized without any waste.

In the heat sink design, based on two goals of reducing the heat sink volume and obtaining high efficiency, it is desirable to select 1.7 or 1.2 kV IGBTs with low loss characteristics. Following this, the number of cells for the available device is calculated. After the calculation of the semiconductor loss, the heat sink volume is calculated based on the concept of the cooling system performance index (CSPI), defined as the inverse of the thermal resistance per unit volume, such that a high CSPI indicates the high cooling performance per unit volume [51].

In the case of the arm inductor design, the inductance is designed by considering the relationship between the ripple current and the arm current. Additionally, the volume of the arm inductor is designed by Area Product. Area product is the evaluation method for the volume of a core, which can be quantitatively calculated from the effective cross section and the window section.

Following the design of the heat sink and the arm inductor, the carrier frequency that minimizes the total volume of the heat sink and the arm inductor is determined by the Pareto front optimization. In addition, the available heat sink and the inductor are selected at the point of maximum power density.

Finally, in order to determine the number of cells for which

$$Voltage\ rating\ ratio = \frac{Required\ voltage\ rating\ in\ each\ number\ of\ cells}{Voltage\ rating\ \ per\ one\ capacitor \times The\ number\ of\ \ series\ \ connected\ capacitors} \quad (1)$$

the overall volume of the capacitor, the heat sink and the arm inductor is at a minimum, the above calculations and design process are repeated. In the volume calculation, the relationship between the number of cells and the capacitor volume is obtained from the database. As a result, it is not necessary to redesign the capacitor and recalculate the capacitor volume. When the number of cells is selected, several points are taken into account. Firstly, when designing the capacitor, the number of cells for which the voltage rating ratio is at its maximum is selected. Secondly, during the design of the heat sink and the arm inductor, the minimum number of cells for which the selected switching device is available is employed. The design principles and the volume evaluation process are explained in the following chapter.

IV. Evaluation of the Volume of the Electrolytic Capacitor

In the case of the cell capacitor of the MMC, high capacitance is required to reduce the ripple voltage of the capacitor, because the ripple voltage disturbs the voltage control of the cell capacitor. Therefore, the use of an electrolytic capacitor should be considered because it has the high capacitance per unit volume. On the other hand, the ripple current that flows to the electrolytic capacitor affects the lifespan of the capacitor. Thus, the ripple current of the capacitor is one of the most important factors in the design of the MMC when electrolytic capacitors are applied. In this work, the relationship between the capacitor volume and the ripple current is examined, using a database of commonly-marketed electrolytic capacitors that are often included in various devices. Moreover, the relationship between the number of cells and the capacitor volume is also considered because the voltage rating of the capacitor drastically changes according to the number of cells.

A. Determination of the Charge Voltage Command

In the MMC, an output DC voltage, V_{mmc}, is applied to each cell of leg because each leg is connected to the load in parallel. In addition, the maximum value of the input phase voltage is applied to each arm. Thus, the capacitor voltage depends on the input voltage and the output voltage. A capacitor voltage command, v_c^*, is given by equation (2) [18].

$$v_C^* \geq \frac{1}{n\lambda}\left(2\sqrt{\frac{2}{3}}E + V_{mmc}\right) \tag{2}$$

where E is the effective input line-to-line voltage, V_{mmc} is the output DC voltage of the MMC and n is the number of cells in each leg. Note that the modulation index, λ, which is set to 0.95 or less and the voltage drop of the arm inductor is ignored because its value is negligible compared to the input phase voltage and the output voltage of the MMC.

B. Relationship between the Ripple Voltage and the Input Phase Difference

As a first step in the design of the lifespan of the electrolytic capacitor, the relationship between the ripple voltage and the input phase difference is clarified in order to determine the worst case when the ripple voltage is maximum. The capacitor voltage, $v_c(t)$, is given by equation (3) [36].

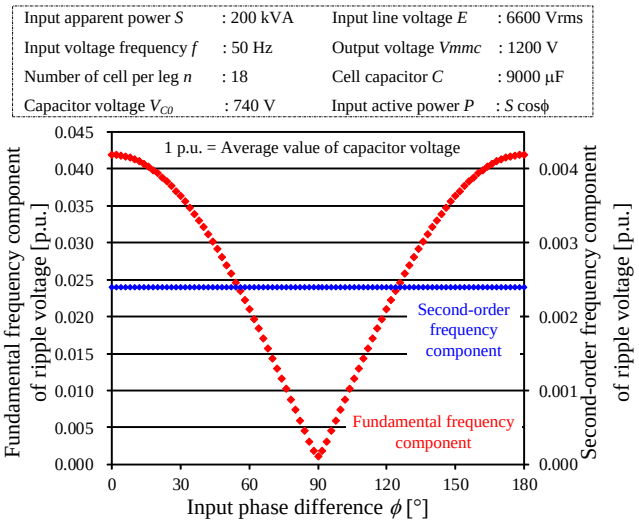


Fig. 5. Relationship between input phase difference ϕ and ripple voltage. The fundamental frequency component is maximum when ϕ is 0 or π.

$$v_c(t) = V_{C0} - \frac{1}{2}\sqrt{\frac{2}{3}}\frac{V_{mmc}\,S}{n\omega C E\,V_{C0}}\sin\omega t + \frac{2}{3}\sqrt{\frac{2}{3}}\frac{EP}{n\omega C\,V_{mmc}V_{C0}}\sin(\omega t+\phi) - \frac{S}{6n\omega C V_{C0}}\sin(2\omega t+\phi) \tag{3}$$

Here, V_{C0} is the average value of the capacitor voltage, S is the input apparent power, ϕ is the input phase difference.

The ripple voltage includes a fundamental frequency component, whose frequency is the same as that of the input voltage, and a second-order frequency component with twice the frequency of the input frequency.

Fig. 5 shows the relationship between the input phase difference, ϕ, and the ripple voltage based on equation (3). The second-order frequency component does not change, even when the input phase difference varies because S is constant. In contrast, the fundamental frequency component reaches its maximum when ϕ is either 0 or π. Thus, it is necessary to design the capacitance considering the ripple voltage when ϕ is 0 as the worst case.

C. Clarification of Ripple Current

The ripple current values of commercially-available capacitors are normally readily obtained from the manufacturer's specifications. The capacitor should be selected such that the ripple current value that flows to each capacitor is sufficiently small compared with the specified value so as to improve the device lifetime. Additionally, the number of capacitors connected in parallel in each cell should be increased so as to obtain the specified ripple current, a process that can dramatically change the capacitor volume. Hence, it is necessary to clarify the relationship between the ripple current and the capacitor volume before the relationship between the number of cells and the capacitor volume is evaluated. The relationship between the capacitor current, i_c, and the capacitor voltage, v_c, is given by equation (4).

$$i_C = C\frac{dv_C}{dt} \tag{4}$$

From equations (3) and (4), it can be seen that the relationship between ϕ and the maximum value of the amplitude is not changed by the differential of the ripple voltage. Therefore, the ripple current reaches its maximum when ϕ is 0, and the maximum effective value of the fundamental frequency component in the ripple current, I_{C_1}, is given by equation (5). Note that V_{C0} is calculated by equation (2).

$$I_{C\_1} = \sqrt{\frac{1}{3}}\frac{\lambda P}{\left(2\sqrt{\frac{2}{3}}E + V_{mmc}\right)}\left(\frac{2}{3}\frac{E}{V_{mmc}} - \frac{1}{2}\frac{V_{mmc}}{E}\right) \tag{5}$$

This equation shows that the maximum effective value of the ripple current will not change as the number of cells or the capacitance are varied.

D. Conditions for Evaluation of the Capacitor Volume

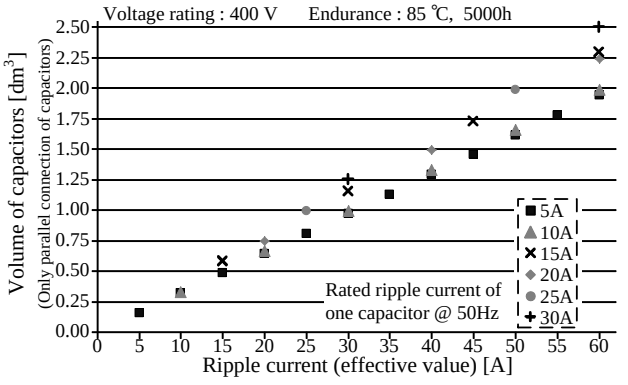
The overall volume of the capacitors is evaluated by using a database of commonly-used commercial electrolytic capacitors. This database is composed of capacitors whose manufacturers (Nippon Chemi-Con, Nichicon and Rubycon) are recommended as suppliers for inverters and high power applications and for which the voltage ratings are from 100 to 600 V [36]. In this database, each capacitor volume is the average of all capacitors with different ripple current values, rounded to the nearest one.

E. Relationship between Ripple Current and Capacitor Volume

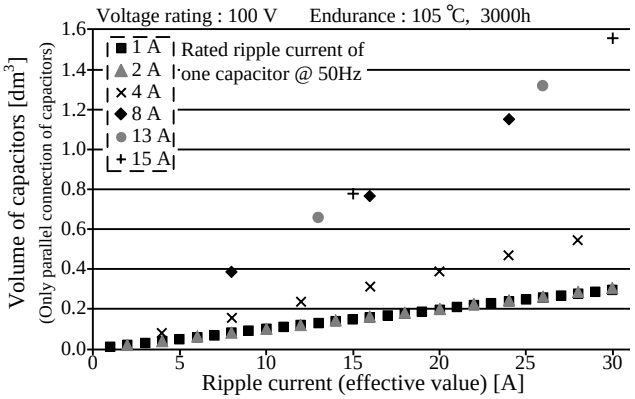
Fig. 6 shows the relationship between the ripple current and the capacitor volume using values from the database as an example. In this graph, the amperages indicate the ripple current of a single capacitor, and the number of capacitors connected in parallel in one cell will increase with the required ripple current values. As well, the starting point of each line indicates the ripple current and the volume of the single capacitor. These data demonstrate that the overall volume of the capacitors is reduced by connecting capacitors with small rated ripple currents in parallel, compared to using only one capacitor with a large rated ripple current and so the parallel connection scenario is preferable. Moreover, the ripple current does not change with variations in the capacitance or the number of cells. Thus, the minimum value of capacitor volume against the number of cells is equivalent to the minimum overall volume.

F. Relationship between the Number of Cells and Capacitor Volume

Fig. 7 plots the relationship among the number of cells, the overall volume of the capacitor and the voltage rating ratio. Note that the number of series connected capacitors increases as the required voltage rating increases above the voltage rating of a single capacitor, making it necessary to use a series connection of capacitors. The required voltage rating in this case is designed to be 30% more than the value calculated by equation (2). The capacitor volume is determined by the



(a) Voltage rating: 400 V, Endurance: 85 °C, 5000h



(b) Voltage rating: 100 V, Endurance: 105 °C, 3000h

Fig. 6. Relationship between ripple current and capacitor volume. The parallel connection of capacitors with small rated ripple currents rather than only one capacitor with a large rated ripple current results in size reduction.

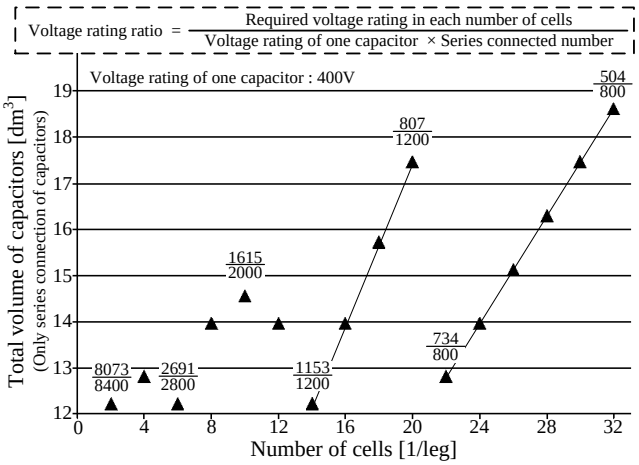


Fig. 7. Relationship between the number of cells and the capacitor volume. The capacitor volume becomes small when the voltage rating ratio is close to 1.0.

quantity of series connected capacitors multiplied by the number of cells under the same ripple current conditions. The voltage rating ratio is defined as the ratio between the required voltage rating and the actual voltage rating when the capacitors are connected in series. As depicted in Fig. 7, the capacitor volume becomes small when the voltage rating ratio at each point is close to 1.0. Hence, it is possible to achieve the desired volume minimization by designing a device for which the

voltage rating ratio is close to 1.0. In conclusion, it is necessary to meet several conditions in order to achieve volume minimization of the capacitors. Firstly, capacitors with low rated ripple currents must be connected, and secondly, the voltage rating ratio should be close to its maximum value of 1.0.

V. Clarification of the Semiconductor Losses for the Heat Sink Design

In this chapter, the equations for semiconductor losses in the H-bridge cell are determined to allow for the design of the heat sink. Following this, the theoretical formulae and simulation results are compared.

A. Calculation of Conduction Losses

Fig. 8 presents a circuit model for the H-bridge cell that allows analysis of the semiconductor losses. The capacitor is replaced with an ideal voltage source to remove the effect of the ripple voltage and the inductor is replaced with an ideal current source to remove the effects of the ripple current and the harmonic distortion.

The cell output voltage and the arm current include DC and AC components. Thus, the magnitudes and the periods of the currents which flow to each switching device in the H-bridge cell are different. The differences of the switching device currents have been considered by defining the duty of the switching device and analyzing the arm current [18].

Fig. 9 shows the relationship between the cell output voltage and the arm current. Each offset of the cell output voltage and the arm current varies according to the input voltage, the output voltage and the output power. Besides, the output power varies according to the input phase difference. Moreover, the angle, θ_a, is the period when the direction of the arm current is positive, whereas the angle, θ_b, is the period when the direction of the arm current is negative. Note that the current direction was defined as shown in Fig. 2. In the definition of each duty, the offset by the DC component in the cell output voltage should be considered. In addition, the angle, θ_0, indicating the direction in which the arm current changes is defined by equation (6) when the arm current is AC [18].

$$\theta_0 = \cos^{-1}\left(\frac{2}{3}\sqrt{\frac{3}{2}}\frac{E}{V_{mmc}}\cos\phi\right) \tag{6}$$

On the other hand, adding or subtracting the offset by the DC component is required depending on the switching device such as S_1, or S_2. In addition, it is also possible to calculate the duty of the free wheeling diode (FWD) such as D_1 or D_2 based on the duty of the switching device. Besides, in the H-bridge cell, S_1 and S_4, which are shown in Fig. 8, operate as a pair, as so do S_2 and S_3. Thus, the semiconductor losses are the same in these paired switching devices [18]. Therefore, in this paper, the formulae of the semiconductor losses in only one leg of the H-bridge cell are shown.

The conduction losses of S_1, S_2, D_1 and D_2 are calculated using equations (7), (8), (9) and (10), respectively [18].

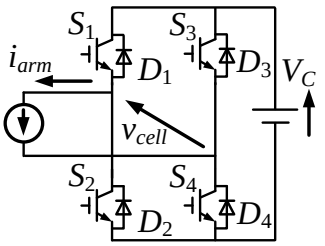


Fig. 8. Circuit model of the H-bridge cell for loss analysis.

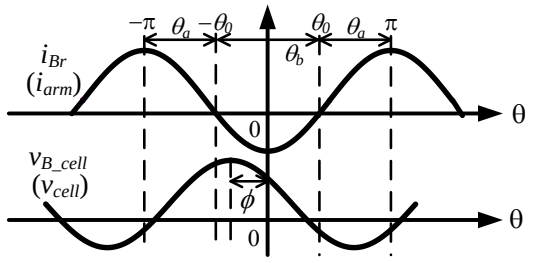


Fig. 9. Relationship between the cell output voltage and the arm current in the lower side of the MMC.

$$\begin{aligned}
P_{B_S1_Con} &= \frac{V_{0_SW}}{4\pi}\left[\left(1+\frac{V_{mmc}}{nV_C}\right)\left\{\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0+\frac{2}{3}\frac{P}{V_{mmc}}(\pi-\theta_0)\right\}\right.\\
&\left.+\frac{1}{nV_C}\left\{-\frac{P}{3}(2(\pi-\theta_0)-\sin 2\theta_0)-\frac{4}{3}\sqrt{\frac{2}{3}}\frac{PE}{V_{mmc}}\cos\phi\sin\theta_0\right\}\right]\\
&+\frac{R_{SW}}{4\pi}\left[\left(1+\frac{V_{mmc}}{nV_C}\right)\left\{\frac{1}{12}\frac{S^2}{E^2}(2(\pi-\theta_0)-\sin 2\theta_0)\right.\right.\\
&\left.+\frac{2}{3}\sqrt{\frac{2}{3}}\frac{PS}{EV_{mmc}}\sin\theta_0+\frac{2}{9}\frac{P^2}{V_{mmc}^2}(\pi-\theta_0)\right\}\\
&+\frac{1}{nV_C}\left\{-\frac{1}{6}\sqrt{\frac{2}{3}}\frac{PS}{E}\left(3\sin\theta_0+\frac{1}{3}\sin 3\theta_0\right)\right.\\
&\left.\left.-\frac{4}{9}\frac{P^2}{V_{mmc}}\left((\pi-\theta_0)-\frac{1}{2}\sin 2\theta_0\right)-\frac{4}{9}\sqrt{\frac{2}{3}}\frac{P^2E}{V_{mmc}^2}\cos\phi\sin\theta_0\right\}\right]
\end{aligned} \tag{7}$$

$$\begin{aligned}
P_{B_S2_Con} &= \frac{V_{0_SW}}{4\pi}\left[\left(1-\frac{V_{mmc}}{nV_C}\right)\left\{\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0-\frac{2}{3}\frac{P}{V_{mmc}}\theta_0\right\}\right.\\
&\left.-\frac{1}{nV_C}\left\{\frac{P}{3}(2\theta_0+\sin 2\theta_0)-\frac{4}{3}\sqrt{\frac{2}{3}}\frac{PE}{V_{mmc}}\cos\phi\sin\theta_0\right\}\right]\\
&+\frac{R_{SW}}{4\pi}\left[\left(1-\frac{V_{mmc}}{nV_C}\right)\left\{\frac{1}{12}\frac{S^2}{E^2}(2\theta_0+\sin 2\theta_0)-\frac{2}{3}\sqrt{\frac{2}{3}}\frac{PS}{EV_{mmc}}\sin\theta_0\right.\right.\\
&\left.+\frac{2}{9}\frac{P^2}{V_{mmc}^2}\theta_0\right\}-\frac{1}{nV_C}\left\{\frac{1}{6}\sqrt{\frac{2}{3}}\frac{PS}{E}\left(3\sin\theta_0+\frac{1}{3}\sin 3\theta_0\right)\right.\\
&\left.\left.-\frac{4}{9}\frac{P^2}{V_{mmc}}\left(\theta_0+\frac{1}{2}\sin 2\theta_0\right)+\frac{4}{9}\sqrt{\frac{2}{3}}\frac{P^2E}{V_{mmc}^2}\cos\phi\sin\theta_0\right\}\right]
\end{aligned} \tag{8}$$

$$P_{B\_D1\_Con} = \frac{V_{0\_FWD}}{4\pi}\left[\left(1+\frac{V_{mmc}}{nV_C}\right)\left\{\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0 - \frac{2}{3}\frac{P}{V_{mmc}}\theta_0\right\}\right.$$
$$\left. + \frac{1}{nV_C}\left\{\frac{P}{3}\left(2\theta_0+\sin 2\theta_0\right) - \frac{4}{3}\sqrt{\frac{2}{3}}\frac{PE}{V_{mmc}}\cos\phi\sin\theta_0\right\}\right]$$
$$+ \frac{R_{FWD}}{4\pi}\left[\left(1+\frac{V_{mmc}}{nV_C}\right)\left\{\frac{1}{12}\frac{S^2}{E^2}\left(2\theta_0+\sin 2\theta_0\right)\right.\right.$$
$$\left. - \frac{2}{3}\sqrt{\frac{2}{3}}\frac{PS}{EV_{mmc}}\sin\theta_0 + \frac{2}{9}\frac{P^2}{{V_{mmc}}^2}\theta_0\right\}$$
$$+ \frac{1}{nV_C}\left\{\frac{1}{6}\sqrt{\frac{2}{3}}\frac{PS}{E}\left(3\sin\theta_0+\frac{1}{3}\sin 3\theta_0\right)\right.$$
$$\left.\left. - \frac{4}{9}\frac{P^2}{V_{mmc}}\left(\theta_0+\frac{1}{2}\sin 2\theta_0\right) + \frac{4}{9}\sqrt{\frac{2}{3}}\frac{P^2E}{{V_{mmc}}^2}\cos\phi\sin\theta_0\right\}\right] \quad (9)$$

$$P_{B\_D2\_Con} = \frac{V_{0\_FWD}}{4\pi}\left[\left(1-\frac{V_{mmc}}{nV_C}\right)\left\{\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0 + \frac{2}{3}\frac{P}{V_{mmc}}\left(\pi-\theta_0\right)\right\}\right.$$
$$\left. - \frac{1}{nV_C}\left\{-\frac{P}{3}\left(2\left(\pi-\theta_0\right)-\sin 2\theta_0\right) - \frac{4}{3}\sqrt{\frac{2}{3}}\frac{PE}{V_{mmc}}\cos\phi\sin\theta_0\right\}\right]$$
$$+ \frac{R_{FWD}}{4\pi}\left[\left(1-\frac{V_{mmc}}{nV_C}\right)\left\{\frac{1}{12}\frac{S^2}{E^2}\left(2\left(\pi-\theta_0\right)-\sin 2\theta_0\right)\right.\right.$$
$$\left. + \frac{2}{3}\sqrt{\frac{2}{3}}\frac{PS}{EV_{mmc}}\sin\theta_0 + \frac{2}{9}\frac{P^2}{{V_{mmc}}^2}\left(\pi-\theta_0\right)\right\}$$
$$- \frac{1}{nV_C}\left\{-\frac{1}{6}\sqrt{\frac{2}{3}}\frac{PS}{E}\left(3\sin\theta_0+\frac{1}{3}\sin 3\theta_0\right)\right.$$
$$\left.\left. - \frac{4}{9}\frac{P^2}{V_{mmc}}\left(\left(\pi-\theta_0\right)-\frac{1}{2}\sin 2\theta_0\right) - \frac{4}{9}\sqrt{\frac{2}{3}}\frac{P^2E}{{V_{mmc}}^2}\cos\phi\sin\theta_0\right\}\right] \quad (10)$$

Here V_0 is the voltage drop at zero current, R is the on-resistance of the switching device, V_C is the capacitor voltage. Both V_0 and R are calculated from values in the datasheets of switching devices.

B. Calculation of Switching and Recovery Losses

The switching losses from S_1 and S_2 are calculated using equations (11) and (12), respectively. Similarly, the recovery losses from D_1 and D_2 are given by equations (13) and (14), respectively [18].

$$P_{B\_S1\_SW} = \frac{V_C}{\pi}\left\{\frac{1}{2}\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0 + \frac{P}{3V_{mmc}}\left(\pi-\theta_0\right)\right\}\frac{w_{on}+w_{off}}{V_{dcd}I_{md}}f_c \quad (11)$$

$$P_{B\_S2\_SW} = \frac{V_C}{\pi}\left\{\frac{1}{2}\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0 - \frac{P}{3V_{mmc}}\theta_0\right\}\frac{w_{on}+w_{off}}{V_{dcd}I_{md}}f_c \quad (12)$$

$$P_{B\_D1\_Rec} = \frac{V_C}{\pi}\left\{\frac{1}{2}\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0 - \frac{P}{3V_{mmc}}\theta_0\right\}\frac{w_{rr}}{V_{dcd}I_{md}}f_c \quad (13)$$

$$P_{B\_D2\_Rec} = \frac{V_C}{\pi}\left\{\frac{1}{2}\sqrt{\frac{2}{3}}\frac{S}{E}\sin\theta_0 + \frac{P}{3V_{mmc}}\left(\pi-\theta_0\right)\right\}\frac{w_{rr}}{V_{dcd}I_{md}}f_c \quad (14)$$

where w is the loss energy value provided in the datasheet, V_{dcd} and I_{md} are the voltage and the current at which w is measured, and f_c is the carrier frequency.

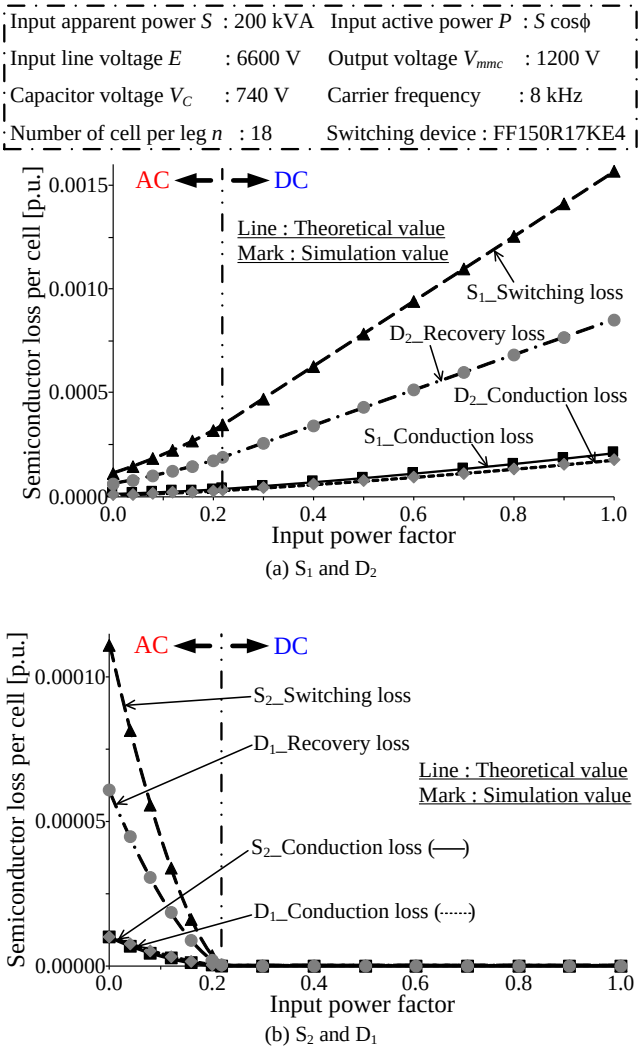


Fig. 10. Comparison result of theoretical formula of semiconductor loss and simulation.

C. Relationship between Input Power Factor and Semiconductor Losses

Here, the relationship between the input power factor and the total loss of the H-bridge cell is clarified in order to design a heat sink according to the worst-case scenario.

Fig. 10 presents a comparison of the results of theoretical calculations of the semiconductor losses and those from the simulation. The theoretical values agree with the simulation values within a maximum error of 1.0% or less, even though the arm current changes from AC to DC at an input power factor of 0.22. Moreover, the losses of S_1 and D_2 increase as the input power factor is raised. In contrast, the losses of S_2 and D_1 decrease. The semiconductor losses change because the DC component in the arm current is varied according to the input power factor. When the input power factor is zero, the semiconductor loss is generated by only the AC component because the active input power (the output power) is zero. The semiconductor loss generated by the DC component increases gradually as the input power factor approaches 1.0. Thus, the losses of S_1 and D_2 increase with increases in the DC

component. In contrast, the losses of S_2 and D_1 decrease to zero because the arm current does not flow to S_2 and D_1.

From the results in Fig. 10, the total loss is at its maximum when the input power factor is 1.0. Thus, it is necessary to design the heat sink for the worst-case semiconductor losses at this input power factor.

VI. Determination of the Ripple Current Formula for the Arm Inductor Design

In this chapter, the formula for the ripple current in the arm inductor is determined to allow for the design of the arm inductor, which is based on the ripple factor of the inductor current. The ripple current varies drastically in association with the multilevel converter when the number of cells or the switching frequency changes. Hence, it is necessary to clarify the relationship between the number of cells, the switching frequency and the ripple current.

A. Analysis of the Ripple Current on Each Arm Inductor by the Equivalent Circuit Model

As a first step in the arm inductor design, it is necessary to clarify the relationship between the ripple current and the number of cells.

Fig. 11 shows the equivalent circuit model of the single phase circuit in the MMC. The circuit operation and the changes in the ripple current are readily determined from the single phase circuit. In the equivalent circuit, the cell capacitor is replaced by an ideal voltage source to remove voltage control of the capacitor voltage. In addition, the output voltage of the cell is determined by equation (15) [18].

$$v_{cell}(t)=\frac{1}{n}\left(2\sqrt{\frac{2}{3}}E\cos(\omega t+\phi)+V_{mmc}\right) \tag{15}$$

From equation (15), the total output voltage of the cells in the arm is equal to the summation of the input voltage and half the value of the MMC output voltage. Hence, only the ripple component is extracted.

Fig. 12 presents a frequency analysis of the ripple current, with the carrier frequency of the cell set to 1.5 kHz. As shown here, the fundamental component is 12 kHz, whereas the frequencies of the second and the third-order components are 24 and 36 kHz.

In the H-bridge cell, employing unipolar modulation gives an output voltage with twice the frequency of the carrier frequency. Additionally, the equivalent switching frequency of the cell total output voltage, v_{Ar}, in each arm, f_{tc_eq}, is given by equation (16).

$$f_{tc\_eq}=\frac{n}{2}*2f_c=nf_c \tag{16}$$

This equation indicates that using eight cells and a carrier frequency of 1.5 kHz gives an f_{tc_eq} value of 12 kHz. It is confirmed that the theoretical value given by equation (16) is equal to the result of the frequency analysis. Moreover, the above result implies that the frequency of the ripple current in each arm inductor is determined by the equivalent switching frequency, f_{tc_eq}. As a result, when assessing the ripple current, only the lower arm in Fig. 11 is considered.

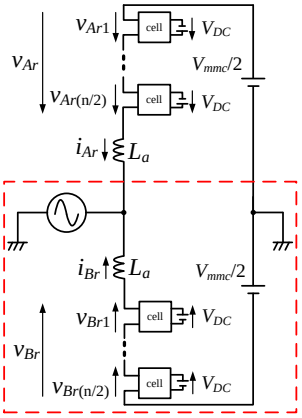


Fig. 11. Equivalent circuit model of the single phase circuit in the MMC. The cell capacitor is replaced by an ideal voltage source.

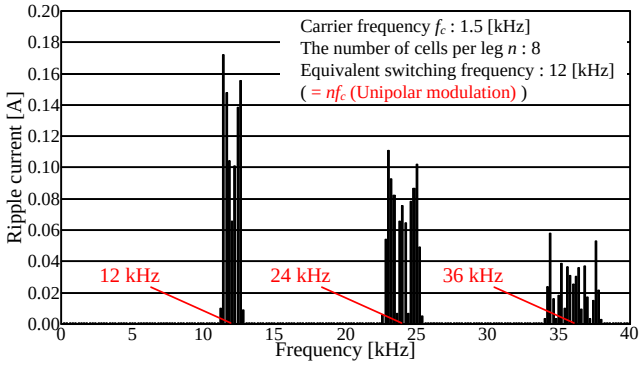


Fig. 12. Frequency analysis of the ripple current. The frequency of the ripple current on each arm inductor is determined by the equivalent switching frequency $f_{tc\_eq} = nf_c$.

B. Relationship between the Duty of the Switching Device and the Ripple Current in the Chopper Circuit

In a general power converter, the ripple current of the inductor is varied by the duty. As an example, in the chopper circuit, the maximum value, Δi_{Lm_ch}, is given via equations (17) [53].

$$\Delta i_{Lm\_ch}=\frac{\Delta i_{Lpp\_ch}}{2}=\frac{V_{out\_ch}}{2L}TD_{on}(1-D_{on}) \tag{17}$$

where V_{in_ch} is the input voltage in the chopper circuit, V_{out_ch} is the output voltage, L is the inductance, T is the switching cycle, D_{on} is the duty of the lower switching device in the chopper circuit. Note that the average value of the ripple current is set to zero in order to calculate only the ripple component.

C. Definition of Duty in Each Multilevel-voltage Step for Clarification of the Ripple Current Formula

Equation (17) determines the relationship between the duty of the switching device and the ripple current of the inductor in the chopper circuit. In the same way, it is possible to determine the equation for the ripple current in the MMC based on the duty of the multilevel voltage. However, the general duties cannot express the variation of the pulse width in each step of the multilevel voltage.

As discussed above, the ripple current is varied by changes in the pulse width, and so it is necessary to define a duty based on

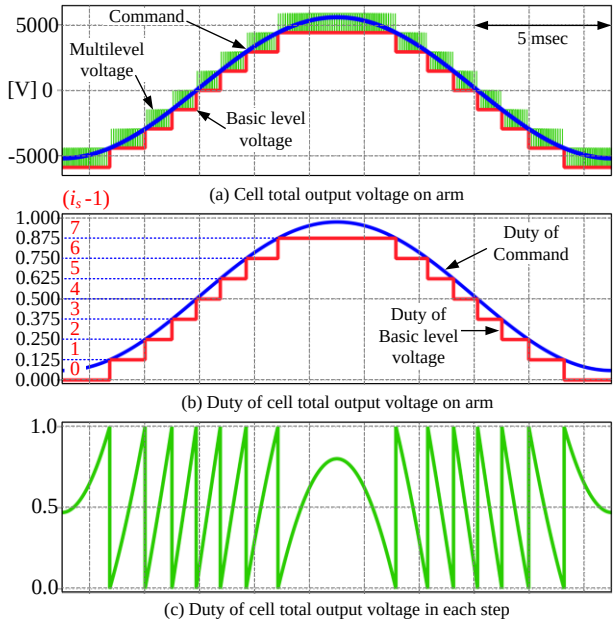


Fig. 13. Command for the cell total output voltage, the multilevel waveform for the total output voltage and the basic level voltage. Each duty of the cell total output voltage and basic level are also shown, as are the duty of the cell total output voltage in each step, d_{mlvs}.

variations in the pulse width in each step of the multilevel voltage waveform. Initially, the basic level in each step of the multilevel voltage is applied in order to consider the variation of the pulse width in each of these steps.

Fig. 13(a) shows the multilevel waveform for the cell total output voltage, v_{Br}, the command waveform for the cell total output voltage and the basic level voltage. First, the multilevel waveform is obtained by the command, while the basic level of the multilevel voltage in each step is obtained as the lower limit of each step. In other words, in each step, the MMC outputs the pulse voltage based on the basic level.

Fig. 13(b) shows the command duty of v_{Br} as well as the duty of the basic level voltage. It is also possible to calculate the duty of the basic level voltage, d_{mlbl}, by equation (18).

$$d_{mlbl} = \frac{1}{n}(i_S - 1) \qquad i_S = 1,2,3\cdots n \tag{18}$$

Here i_s is an index that is varied from 1 to n.

As an example, at n = 8, the step of the multilevel voltage varies periodically when d_{mlbl} is 0.125, 0.250 or 0.375. From equation (18) and Fig. 13, it is apparent that the variation of the duty in each step, such as at 0.125 and 0.250, is determined solely by the number of cells, n.

Fig. 13(c) plots the duty, d_{mlvs}, at each step of the cell total output voltage, such that d_{mlvs} varies from 0.0 to 1.0 in each step. This value is derived by taking the difference between the command voltage and the basic level, then dividing by the capacitor voltage. As a result, d_{mlvs} is defined by equation (19).

$$d_{mlvs} = \left|(i_s - 1) - nD\right| \tag{19}$$

where D is the cell duty which defined by equation (20). Note that i_s should be modified according to the number of voltage levels when the number of voltage levels is changed by the modulation.

$$D = \frac{1}{2}\left\{1 + \frac{1}{nV_C}\left(2\sqrt{\frac{2}{3}}E\cos(\theta + \phi) + V_{mmc}\right)\right\} \tag{20}$$

D. Clarification of the Ripple Current Formula

In order to determine the formula for the ripple current in the arm inductor, each parameter of equation (21) is replaced as follows.

$$V_{out\_ch} = V_C,\ T = \frac{1}{nf_C},\ D_{on} = d_{mlvs},\ L = L_a \tag{21}$$

The maximum value of the ripple current on the arm inductor, Δi_{Lm}, is given by equation (22).

$$\Delta i_{Lm} = \frac{V_C}{2nf_C L_a} d_{mlvs}\left(1 - d_{mlvs}\right) \tag{22}$$

In equation (22), the maximum value of the ripple current is varied by d_{mlvs}, which changes frequently. Therefore, equation (22) generates an envelope of maximum ripple current values. In addition, the peak value of the ripple current is obtained by differentiating equation (22) with respect to d_{mlvs} and determining the extremum.

$$\frac{d\Delta i_{Lm}}{dd_{mlvs}} = \frac{V_C}{2nf_C L_a}\left(1 - 2d_{mlvs}\right) \tag{23}$$

From equation (23), when d_{mlvs} is 0.5, the formula has an extremum, and Δi_{Lm} reaches its peak value at d_{mlvs} = 0.5.

Fig. 14 shows the multilevel voltage waveform for the cell total output voltage in one arm, v_{Br}, the duty of the cell total output voltage in each level, d_{mlvs}, and the waveforms for the ripple current, the envelope of the ripple current and the reversed envelope of the ripple current. These data confirm that the ripple current envelope calculated by equation (22) traces the maximum values. The ripple current is also seen to peak when d_{mlvs} is 0.5.

Thus, in the design of the arm inductor, the peak value at a d_{mlvs} of 0.5 is applied as the worst-case design scenario.

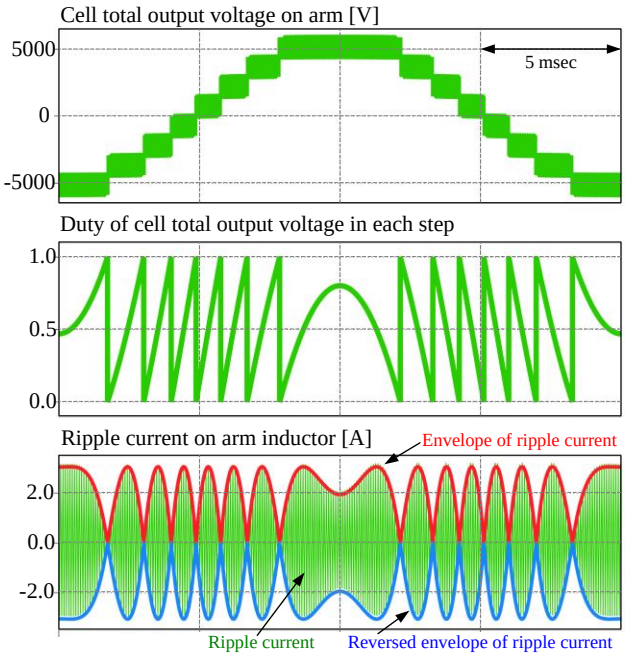
VII. Experimental Results from a Miniature Model

A. Verification of the Fundamental Operation of a Step-down Rectifier Using an MMC

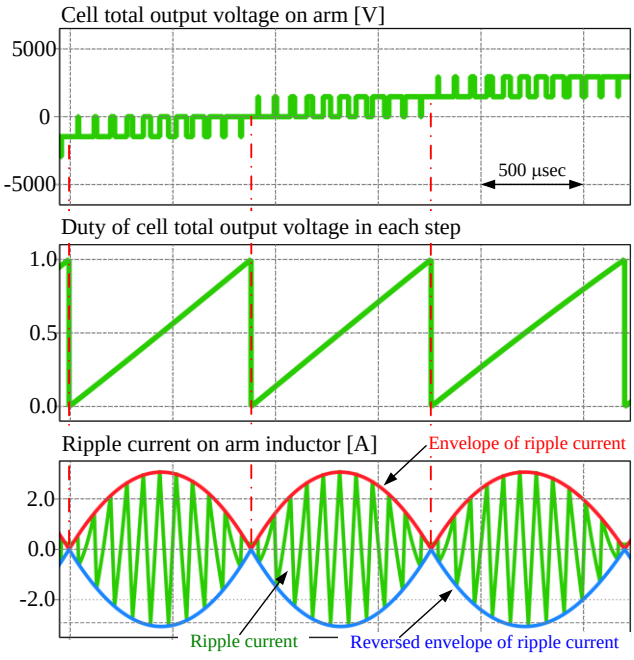
This paper includes the aim of clarifying the validity of formulae in experiments. Thus, expected circuit operations are required for the miniature model and experimental waveforms are shown to confirm fundamental operations.

Table I summarizes the experimental conditions. The miniature model was constructed using four cells per leg. Because this was a fundamental experiment, a resister was used as the MMC load without a smoothing capacitor.

Fig. 15 shows the waveforms for the input phase voltage, the input R-phase current and the DC output voltage. The waveforms for the input phase voltage and the input current confirm that a unity power factor was obtained in the input stage. The total harmonic distortion (THD) of the input current was 3.2% when the normalized impedance, %Z, of the arm inductor was 6.1%. It can also be seen that the output DC voltage waveform in the lower side of Fig. 15 indicates that the step-down rectifier converted the input voltage of 200 V into a constant output DC voltage of 75 V. Therefore, the proposed



(a) One cycle



(b) Expanded waveforms

Fig. 14. Multilevel voltage waveform of cell total output voltage in one arm, duty of cell total output voltage in each step and waveforms of ripple current, envelope of ripple current and reversed envelope of ripple current.

rectifier for the MMC generated step-down rectification.

Fig. 16 presents the arm voltage waveforms, representing the sum of the output voltages of all cells in each arm, and the waveform for the line voltage between the R-phase and S-phase in the upper side. The system produces five levels of arm voltage because one of the H-bridge cells, having unipolar modulation, produces three levels of voltage and the arm has two cells. In addition, the waveforms are not symmetrical between the positive and negative sides because the output voltage of the H-bridge cell includes a DC component.

TABLE I
EXPERIMENTAL CONDITIONS

Rated output power	P_O	1000 W
Input line voltage	E	200 Vrms
Input voltage frequency	f	50 Hz
Output voltage	V_{mmc}	75 V
Number of cell per leg	n	4
DC capacitor	C	1300 µF
Load	R	5.3 Ω
Carrier frequency	f_C	8 kHz
Arm inductor	L_a	8 mH (%Z = 6.1%)

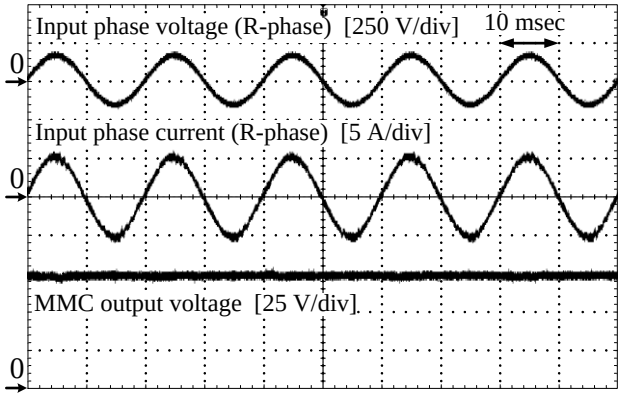


Fig. 15. Waveforms for input voltage, input current and output voltage. The unity power factor is obtained in the input stage. The THD of the input current is 3.2% when the %Z of the inductor is 6.1%.

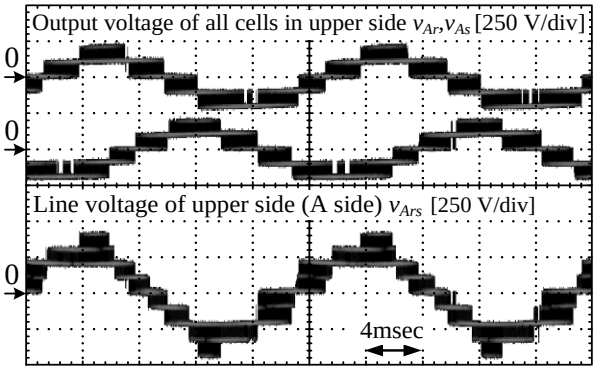


Fig. 16. Waveforms for arm voltage which is the summation of output voltage of all cells in each arm and waveforms of line voltage between R-phase and S-phase in upper side. The arm voltage is five levels and the line voltage is nine levels.

The waveform for the line voltage between the R-phase and S-phase in the upper side exhibits nine levels. However, the multilevel voltage waveform becomes non-uniform. This occurs because the arm voltage is not symmetrical between positive and negative, since the cell command voltage includes the bias of the MMC output voltage control. However, the voltage fluctuation is still small compared to that obtains when employing chopper cells or H-bridge cells with bipolar modulation. Thus, the MMC allows size reduction of the arm

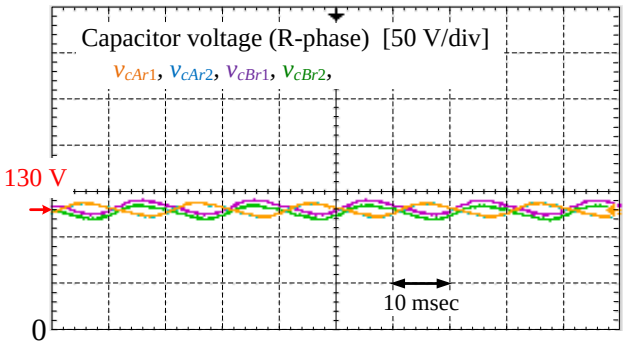


Fig. 17. Waveforms for the capacitor voltage in the R-phase leg. The proposed system maintains the capacitor voltage of each H-bridge cell to the voltage command of 130 V. In addition, the maximum voltage error between the capacitor voltage command and the measured voltage is 2% or less.

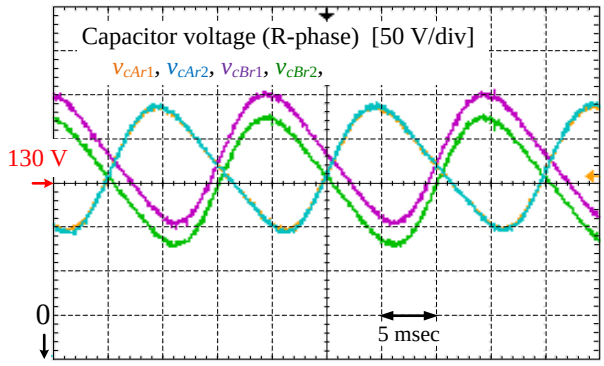


Fig. 18. Waveforms for the ripple voltages of all capacitors that are connected to the R-phase leg. In principle, each capacitor in the MMC has a low frequency ripple voltage because the frequency of the ripple voltage is based on the frequency of the input voltage source.

inductor s.

Fig. 17 plots the waveforms for all cell capacitor voltages that are connected to the R-phase leg. The cell capacitor voltage is controlled by the capacitor voltage command, v_c^*. As a result, the proposed step-down rectifier maintains the capacitor voltage of each H-bridge cell to the voltage command level of 130 V. Therefore, the proposed rectifier also achieves capacitor voltage control. In addition, the maximum voltage error between the voltage command of the cell capacitor and the measured voltage is 2% or less.

Fig. 18 shows the waveforms for the ripple voltages of all capacitors that are connected to the R-phase leg. In principle, each capacitor has a ripple voltage whose frequency is based on the frequency of the input voltage. From the waveforms for the ripple voltages, the low frequency waveforms for the ripple voltages are shown, as in the above discussion. In addition, there is some error among the capacitor voltages. However, as already discussed in Fig. 17, the voltage errors among all the capacitors are negligibly small compared to the average value of the capacitor voltages.

B. Verifications of the Theoretical Formula for the Ripple Current in the Capacitor

In this section, the results obtained from the theoretical formula for the capacitor ripple current are presented. In order to evaluate the ripple current of the capacitor, a frequency analysis of the capacitor voltage was conducted because it is difficult to measure the ripple current of the capacitor directly in the miniature model. However, because the ripple voltage is caused by the ripple current, the validity of the formula can still be verified if the measured ripple voltage and the theoretical value obtained from equation (3) are shown to be the same. The fundamental frequency component and the second-order frequency component of the ripple voltage which is given by equation (3) are compared with the measured values.

Fig. 19 shows a comparison of the theoretical and measured values of the fundamental frequency component in the ripple voltage. The experimental data agree with the theoretical values in a small error, with a maximum error of 4.3 %.

Fig. 20 compares the theoretical and measured second-order frequency components. Here, the difference between the theoretical and experimental values is large, with a maximum error of 34.2%. This is significant error results from the mismatch of the input active power and the output power due to the semiconductor loss and the inductor loss.

Fig. 21 shows a comparison of the theoretical and measured second-order frequency components based on the input active power. The value of input active power is assigned to the variable P in equation (3). Here, the maximum error is reduced to 4.1%, and this establishes that the high error in Fig. 20 was caused by the mismatch of the input active power and the output power due to the semiconductor loss and the inductor loss. In the design of a practical converter, all losses must be minimized in order to obtain high efficiency. Thus, the error in the second-order frequency component based on the output power is small because of the low loss.

The above results demonstrate the validity of the formula for the capacitor voltage ripple. These data also confirm that the ripple current of the capacitor can be calculated exactly by the theoretical formula.

C. Verification of the Theoretical Formula for the Ripple Current in the Arm Inductor

In this section, the results for the ripple current in the arm inductor are assessed.

Fig. 22 shows the expanded waveforms for the lower arm voltage in the R-phase and the arm current. The arm voltage is the total output voltage of the two cells. The expanded waveform focuses on the output voltage, for which the duty in each step of the cell total output voltage, d_{mlvs}, is 0.5 (equivalent to the point at which the ripple current reaches its maximum). As shown in Fig. 22, the measured peak-to-peak value of the ripple current was 118 mA. The theoretical value obtained by doubling the result from equation (22) is 124 mA, the doubling being applied because the peak-to-peak value is twice the maximum value. Thus, the error between the theoretical and measured values is 4.9%. Note that the inductance used in equation (22) is determined at a frequency of 32 kHz because this is the equivalent frequency of one arm in the miniature model. Moreover, unipolar modulation is applied to each cell.

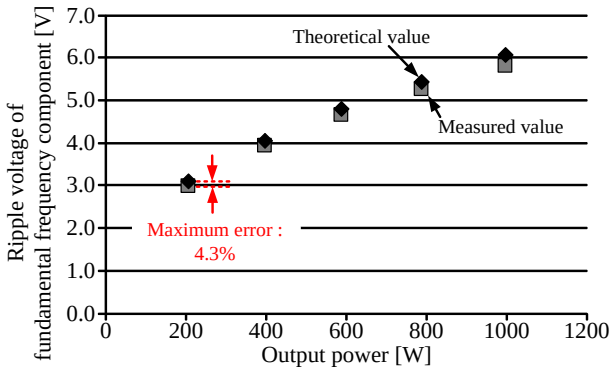


Fig. 19. Comparison of theoretical values and measured data for the fundamental frequency component of the ripple voltage. The maximum error between the theoretical and measured values is 4.3%.

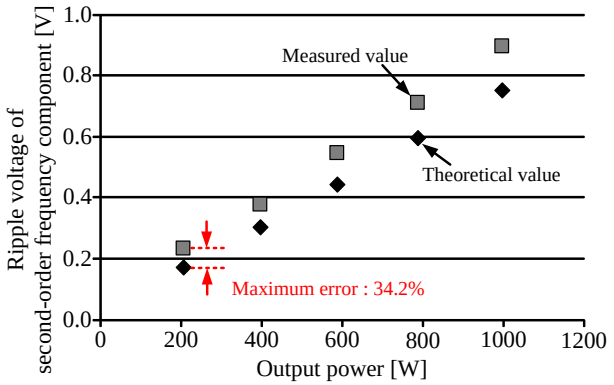


Fig. 20. Comparison of theoretical and measured values for the second-order frequency component in the ripple voltage. The maximum error between the theoretical value and the measured value is 34.2%. The cause of the large error is the mismatch of the input active power and the output power due to the semiconductor loss and the inductor loss.

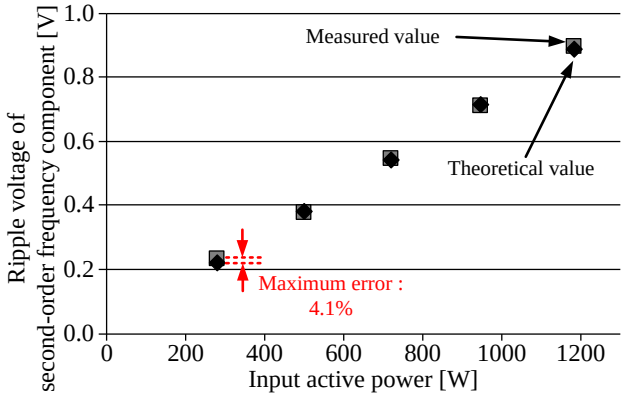


Fig. 21. Comparison of the theoretical and measured values of the second-order frequency component based on input active power. The maximum error between the theoretical and measured values is 4.1%.

Fig. 23 compares the theoretical and experimentally determined ripple currents in the arm inductor against the capacitor voltage. In the low voltage region, the error is 10% or less while, in the high voltage region, the error is increased to a maximum value of 11.8%. Although the theoretical values increase linearly, the measured values exhibit non-linear

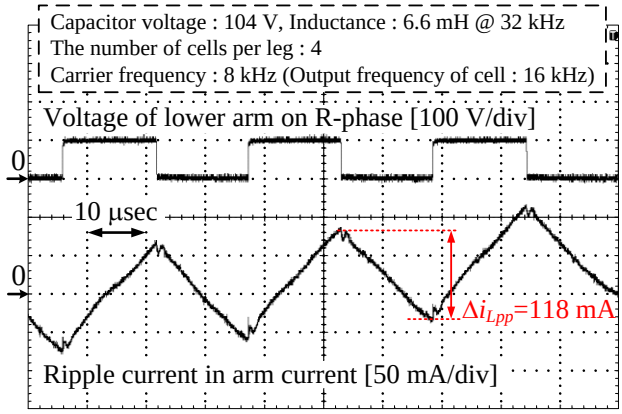


Fig. 22. Waveforms for lower arm voltage in R-phase and arm current. The expanded waveforms focus on the output voltage of which the duty in each step of the cell total output voltage, d_{mlvs}, is 0.5. The error between the theoretical value and the measured value is 4.9%.

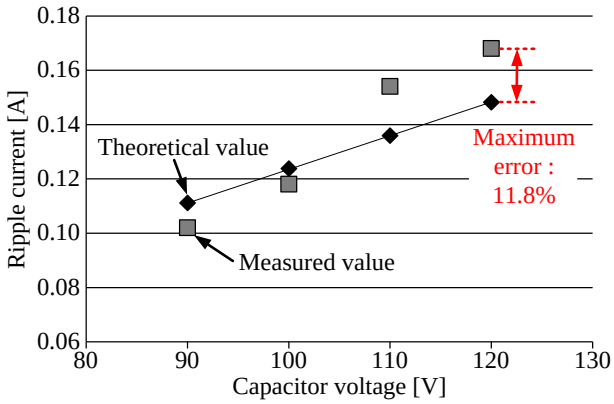


Fig. 23. Comparison of the theoretical and measured ripple currents in the arm inductor against capacitor voltage. The maximum error is 11.8%. This error results because the inductance decreases due to the decrease of the permeability as the core temperature is raised.

growth. Note that, at higher voltages, the experimental values are larger than the theoretical values. This is caused by a decrease in the inductance due to the characteristics of the core. In general, the permeability of the core will vary with temperature. In the experimental trials, the magnetic flux values increased due to the increase in the capacitor voltage, thus elevating the iron loss of the core. As a result, the core temperature was higher at high voltage. Thus, the inductance decreased due to the decreased permeability at higher core temperatures.

D. Verification of the Theoretical Formulae for Semiconductor Losses

In this section, the theoretical values of the semiconductor losses are assessed. In these experiments, the semiconductor, the arm inductor and no-load losses were considered. The no-load loss was measured as the MMC operated without the converter being connected to the load. In this state, the input power is defined as the no-load loss. The input power, output power and inductor loss were measured simultaneously as the MMC was operated with the converter connected to the load. By subtracting the output power, the inductor loss and the

no-load loss from the input power, the semiconductor loss is obtained.

Table II summarizes the circuit and loss parameters used during the verification of the semiconductor loss equations. The loss parameters relating to the conduction loss were obtained from the datasheets for the switching devices, whereas the switching and recovery loss parameters were obtained from the experimental values generated by switching tests.

Fig. 24 compares the experimental and theoretical values. The theoretical value is defined as the sum of the conduction, switching and recovery losses in all cells. The maximum error is seen to be 6.1%. However, over the entire range, the measured values are larger than the theoretical results. This is attributed to losses via the equivalent series resistance (ESR) of the capacitor and the wiring loss, neither of which are considered in the measurements. Thus, the experimentally determined semiconductor losses include losses that are not considered, and so these measured values are greater than the theoretical ones. The differences between the measured and theoretical data are also seen to increase as the output power increases. This occurs because both the loss in the capacitor and the wiring loss increase with increasing the output power, due to greater values of the ripple current of the capacitor and the arm current.

Fig. 25 shows a breakdown of the losses in the MMC. The no-load loss is constant against changes in the output power, while the semiconductor and inductor losses both increase with increases in the output power because the arm current is higher. From these results, it is evident that the semiconductor loss represents the majority of the overall losses. Therefore, the design should attempt to minimize the semiconductor loss in order to achieve the highest possible efficiency and volume reduction because the semiconductor loss and the volume of the heat sink are simultaneously reduced. One means of reducing the semiconductor loss is to decrease the arm current by raising the MMC output voltage, because the semiconductor loss is greatly affected by the arm current.

VIII. Volume Evaluation of the MMC and Clarification of Conditions for Volume Reduction

In this chapter, the volumes of the capacitor, the arm inductor and the heat sink are evaluated. Moreover, based on the results, the conditions required to obtain the highest power density are established.

With regard to evaluating the capacitor volume, the discussion in Chapter IV has already established that it is important to select the number of cells for which the voltage rating ratio is maximized in order to achieve volume reduction. In addition, the changes in the capacitor volume must be evaluated as the MMC output voltage is varied.

In this stage of the work, the total volume of the arm inductor and the heat sink were evaluated by the Pareto front optimization. It is often possible to reduce the inductor volume when the carrier frequency increases because this lowers the ripple current. However, the heat sink volume actually increases in the present scenario because the switching loss increases as a result of the high switching frequency. Hence, the heat sink volume and the inductor volume have a trade-off relationship. Furthermore, the efficiency also decreases due to the high switching loss, although the power density increases because the inductor volume is lowered. Therefore, in this study, the maximum power density was assessed based on using the Pareto front optimization [50].

TABLE II
CIRCUIT PARAMETERS AND LOSS PARAMETERS FOR VERIFICATION

Input line voltage	E	200 Vrms	The number of cells	n	4 /leg
Capacitor voltage	V_C	135 V	Load resistance	R	5.2 Ω
Carrier frequency	f_C	8 kHz			
Output power		P_O	200 - 1000 W		
Switching device		-	FGW30N60VD		
Drop voltage of switch		V_{0_SW}	0.74 V @ Tj =25 °C		
Resistance of switch		R_{SW}	0.0536 Ω @ Tj =25 °C		
Drop voltage of FWD		V_{0_FWD}	0.8 V @ Tj =25 °C		
Resistance of FWD		R_{FWD}	0.0492 Ω @ Tj =25 °C		
Turn-on energy of switch		w_{on}	52.98 μJ@V_{dcd}=135 V I_{md}=6.7 A		
Turn-off energy of switch		w_{off}	31.97 μJ@V_{dcd}=135 V I_{md}=8.3A		
Turn-on energy of FWD		w_{rr}	6.21 μJ@V_{dcd}=135 V I_{md}=0.6 A		

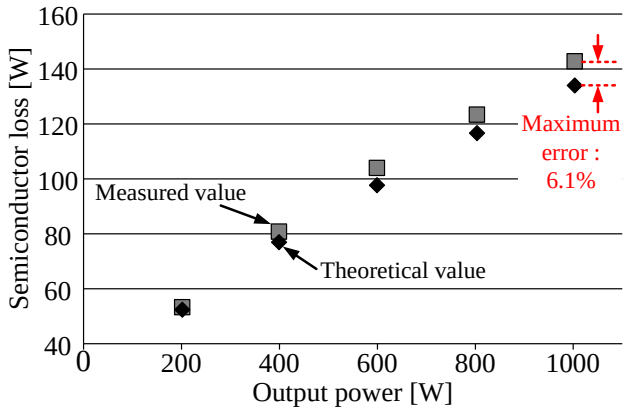


Fig. 24. Comparison of theoretical and measured semiconductor losses. The maximum error is 6.1%. This error is attributed to losses from the equivalent series resistance (ESR) of the capacitor and the wiring loss, which are not considered in the calculations.

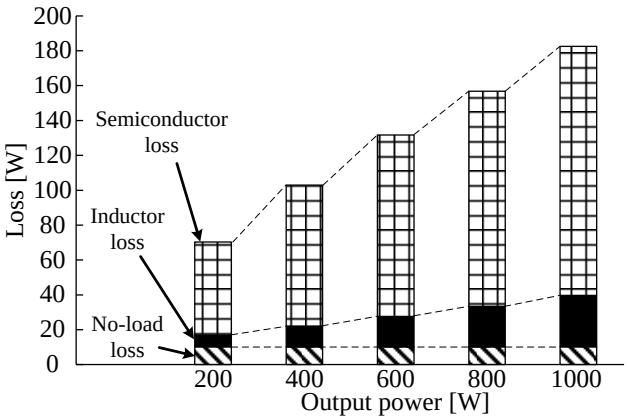


Fig. 25. Breakdown of losses in the MMC. The no-load loss is constant despite varying the output power. In contrast, the semiconductor and inductor losses increase with increases in the output power because the arm current is elevated.

A. *Conditions for Evaluation of the Overall Volume*

Table III shows the conditions of the overall volume evaluation. The detailed design conditions employed when evaluating the overall volume consisted of the following:
(1) an input line voltage of 6.6 kV and an MMC power capacity of 200 kVA,
(2) the capacitor was the NIPPON-CHEMICON model ERWF401LGC182MC85M and the voltage rating of the single capacitor was 400 V with a rated ripple current of 5 A at a frequency of 50 Hz [54],
(3) the increase in the internal temperature was limited to 25 °C based on the manufacturer's recommendations,
(4) the number of parallel connected capacitors was selected so as to ensure a capacitor lifespan of at a least decade,
(5) the charge voltage of the capacitor was calculated by equation (2) and the voltage rating included a 30% margin against the charge voltage while the number of series connected capacitors was determined based on the voltage rating,
(6) the voltage rating of the switching device was set at 80% more than the charge voltage of the capacitor and the current rating was set at twice the rated value of the arm current,
(7) the carrier frequency was varied from 10 Hz to 190 kHz,
(8) the loss data at the maximum junction temperature was obtained from each datasheet and the allowable junction temperature was set at 80% of the maximum allowable value [55]-[56],
(9) the heat sink was designed based on the CSPI [51] and the CSPI value was assumed to be 3.0 (natural air cooling),
(10) the loss data for the SiC-MOSFET was obtained from the loss characteristics of a single chip [57]-[58], so that the parallel connection number of the chip was determined in order to meet the conditions of the current rating, and
(11) the maximum junction temperature of the SiC-MOSFET was set at 175 °C.

B. *Evaluation of the Overall Volume*

In this section, the capacitor volume, the heat sink volume and the volume of the arm inductor are evaluated to establish the necessary conditions for volume reduction. Note that the curve of the Pareto front includes only the total volume of the heat sink and the arm inductor so as to evaluate only the change in the total volume. The overall volume including the capacitor volume is subsequently evaluated.

Fig. 26 shows the capacitor volume as a function of the MMC output voltage. The numbers under the graph indicate the number of cells for which a 1.7 kV IGBT is available. The capacitor volume is seen to decrease as the MMC output voltage increases even when the number of cells is kept constant. This is attributed to the decrease in the ripple current as the arm current decreases even at the same power rating. As a result, it is possible to reduce the capacitor volume by decreasing the required number of parallel connected capacitors. Moreover, the capacitor volume is small when the voltage rating ratio is high, as explained in Chapter IV. Thus, the number of cells should be determined based on the voltage rating ratio in order to reduce the capacitor volume.

Fig. 27 presents the Pareto front curve when the MMC output voltage is 800 V. The power density of the converter applied to the 3.3 kV SiC is approximately two times higher than that of a converter applied to other switching devices. A high efficiency is also obtained at a switching frequency of 5.2 kHz because the converter applied to the 3.3 kV SiC reduces

Table III
CONDITIONS OF OVERALL VOLUME EVALUATION

Power capacity	S	200 kVA	Input line voltage	E	6.6 kV
Input frequency	f	50 Hz	Input power factor	ϕ	1.0
Electrolytic capacitor					
Model number	ERWF401LGC182MC85M				
Voltage rating	30% margin against charge voltage				
Raise value of inside temperature	25 °C (Recommended value)				
Arm inductor					
Ripple current factor	5%		Flux density		1.56 T
Constant value	17.9		Current density		4 A/mm^2
Window utilization factor	0.3		Core type		C core
Heat sink					
Switching device	Infineon FF, FZ series and Hitachi 2.5 kV IGBT				
Operation junction temperature	80% of maximum temperature.				
Voltage rating	80% more than capacitor voltage				
Current rating	Twice value as rated current.				
CSPI	3.0 (Natural air cooling)				

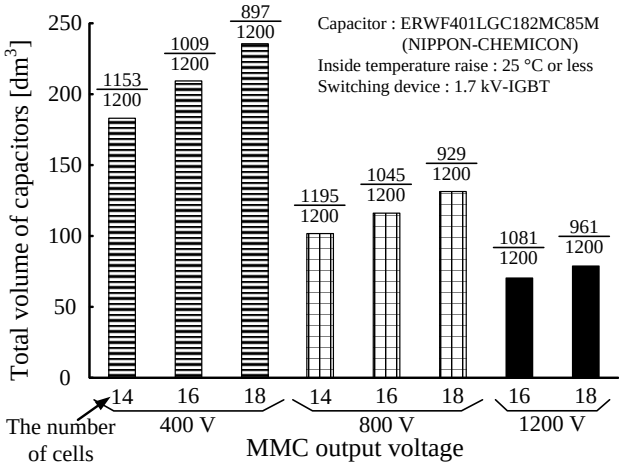


Fig. 26. Change in the capacitor volume against the MMC output voltage. The values under the graph indicate the number of cells for which a 1.7 kV IGBT is available. At the same output voltage, the capacitor volume is small when the voltage rating ratio is high.

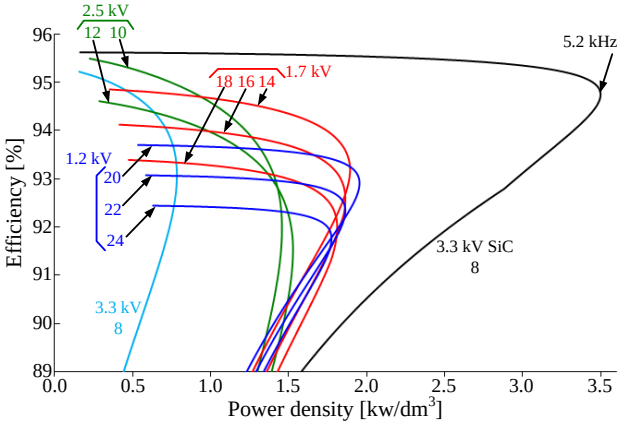


Fig. 27. Pareto front curve for an MMC output voltage of 800 V. The power density of the converter applied to the 3.3 kV SiC is approximately two times higher compared to the converter applied to other switching devices.

the volumes of both the heat sink and the arm inductor, since SiC devices exhibit especially low losses and can operate at higher switching frequencies.

Fig. 28 plots the Pareto front curve at an MMC output voltage of 1200 V. The converter applied to the 3.3 kV SiC also generates a higher power density and obtains high efficiency relative to that of other high voltage IGBTs, for the same reasons as outlined when discussing the MMC output voltage of 800 V. Higher power density and greater efficiency are achieved in all switching devices compared to the results in the case of an MMC output voltage of 800 V. The main reason for this is the decreased semiconductor loss and the heat sink volume decrease because of the decrease in the arm current upon raising the MMC output voltage.

Fig. 29 shows the expanded Pareto front curve at an MMC output voltage of 1200 V without a 3.3 kV SiC. The 3.3 kV SiC has the highest performance in terms of a low switching loss and high frequency switching. However, it is still difficult to apply a 3.3 kV SiC to a practical system because these switching devices are not yet readily available. The voltage stress of the arm inductor should be kept low for isolation protection because this stress is high when a 3.3 kV SiC is applied to the MMC. In the case that a 3.3 kV SiC is excluded from consideration, a 1.7 or 1.2 kV IGBT is the most preferable selection if the aim is to achieve high power density. In order to apply a 1.7 kV IGBT, the number of cells should be 16 or 18, whereas there should be 20, 22 or 24 cells in the leg when using 1.2 kV IGBT. Both IGBTs produce the highest power density when the design quantity of cells is kept to a minimum. A feature of multilevel converters is that it is possible to decrease the switching loss and the recovery loss by increasing the number of cells. However, within the range of cell quantities that can be employed in the same switching device, the potential decreases in the switching and recovery losses is limited because the charge voltage of the capacitor does not change drastically, which leads to a small volume reduction. To sum up, it is possible to slightly reduce the volume of a single heat sink by increasing the number of cells, but the total volume of the heat sink increases upon increasing the total number of cells. It is also difficult to reduce the volume of the arm inductor when using the same switching devices, even if the number of cells changes, because the ripple current in the arm inductor does not change drastically. Therefore, in order to reduce the total volume of the heat sink and the arm inductor, it is necessary to select the smallest number of cells for which the selected switching device is available.

Fig. 30 presents a breakdown of the overall volume when the MMC output voltage is 1200 V and a 1.7 or 1.2 kV IGBT is used. Comparing the volumes of the conventional power system and the MMC, it can be concluded that the MMC allows a 90% volume reduction if the 1.2 kV IGBT is employed in conjunction with 22 cells per leg. Furthermore, it is apparent that the capacitor volume is the largest component of the overall volume and that the variation in the capacitor volume with different devices and numbers of cells is remarkably high. These results demonstrate that, as the first step of the design of the MMC, it is necessary to focus on selecting the number of

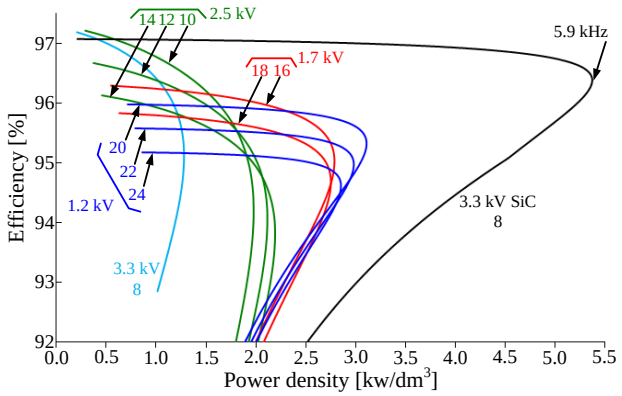


Fig. 28. Pareto front curve at an MMC output voltage of 1200 V. All switching devices achieve higher power density and higher efficiency compared to the evaluation result with the MMC output voltage of 800 V.

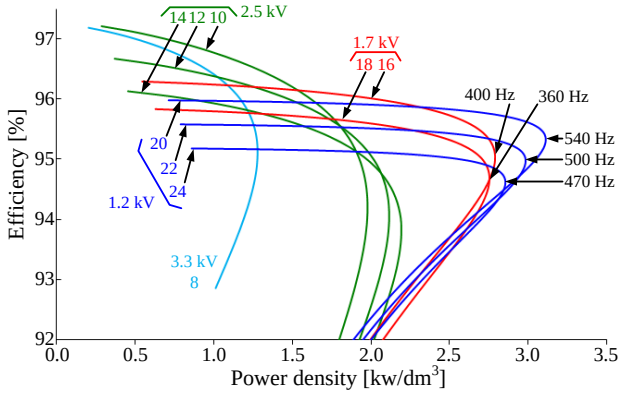


Fig. 29. Expanded Pareto front curve at an MMC output voltage of 1200 V without a 3.3 kV SiC. The converter applied to a 1.7 or 1.2 kV IGBT produces a higher power density except for the 3.3 kV SiC. Moreover, both 1.7 and 1.2 kV IGBT produce the highest power density when the lowest number of cells is employed.

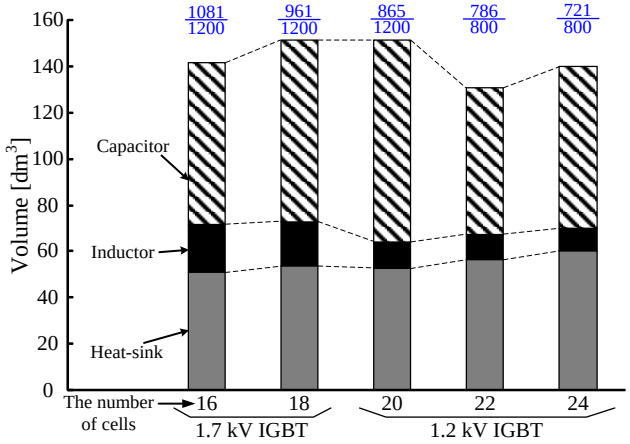


Fig. 30. Breakdown of the overall volume for an MMC output voltage of 1200 V and a 1.7 or 1.2 kV IGBT. The change in the capacitor volume is particularly large. From the above results, the first step in the design of the MMC should focus on the number of cells for which the capacitor volume is small based on the voltage rating ratio.

cells at which the capacitor volume is small based on the voltage rating ratio. Subsequently, the number of cells for which the volumes of both the heat sink and the arm inductor are minimized should be considered. Finally, these data confirm the effectiveness of the design flow proposed in

Chapter III as a means obtaining high power density with an MMC.

IX. Conclusion

This paper presented a design criteria to obtain the high power density in a step-down rectifier incorporating an MMC. Readily available commercial electrolytic capacitors were used. The work focused on the relationship between the volume and the number of cells. The major contributors to the overall volume of the MMC were found to be the heat sink, the capacitor and the arm inductor.

A flowchart for the high power density design process was constructed, based on assessing the capacitor, the heat sink and the arm inductor. This process omitted recalculation of the capacitor volume by employing a database containing capacitor volumes as functions of the number of cells.

In the evaluation of each component, theoretical formulae were generated and their validity confirmed based on experimental data obtained from a miniature model of the MMC. The following results were produced.

(a) When verifying the ripple voltage of the capacitor, there was a maximum error of 4.3% between the theoretical and measured values. Because the ripple voltage is caused by the ripple current, it is possible to accurately calculate the ripple current of an electrolytic capacitor using the theoretical formula.

(b) With regard to the ripple current in the arm inductor, there was a maximum error of 11.8%, caused by changes in the core characteristics. Therefore, it is possible to calculate the ripple current with a high degree of accuracy by considering the inductance changes resulting from the variations in the core characteristic.

(c) In the case of the semiconductor losses, there was a maximum error of 6.1%, showing that it is possible to calculate the semiconductor losses while designing the heat sink.

The overall volume of circuit devices, including the capacitor, the heat sink and the arm inductor, was evaluated. In particular, the capacitor volume was examined against the number of cells and the MMC output voltage. In addition, the total volume of the heat sink and the arm inductor was investigated using the Pareto front optimization. It was determined that the following conditions must be satisfied in order to achieve high power density:

(i) employing a capacitor with a small rated ripple current and increasing the quantity of parallel connected capacitors,

(ii) maximizing the voltage rating ratio, whose maximum value is 1.0,

(iii) selecting a 1.7 or 1.2 kV IGBT as the high voltage switching devices, and

(iv) using the smallest number of cells for which a selected switching device such as 1.7 or 1.2 kV IGBT is available.

Finally, when a 3.3 kV SiC is applied to the MMC, it is possible to obtain a higher power density compared to the use of other high voltage IGBTs. In the future, the cost reduction of the 3.3 kV SiC may allow this design to be considered and so further miniaturization is expected when a high performance switching device such as a 3.3 kV SiC is applied to the MMC.

It is expected that the results of this paper promote the discussion of the design criteria focused on the number of cells and the output voltage of the MMC for the high power density. In particular, the design criteria of the electrolytic capacitor, the volume comparison of the electrolytic capacitors and the film or ceramic capacitor and the usability of the electrolytic capacitor in the MMC will be promoted by this paper.

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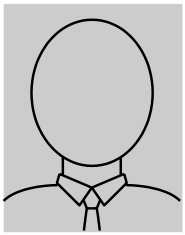

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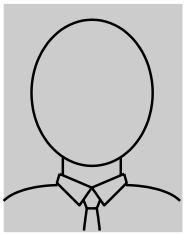

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