Isolated Single-phase Matrix Converter using Center-tapped Transformer for Power Decoupling Capability

Nagisa Takaoka, Hiroki Takahashi and Jun-ichi Itoh
Student member, IEEE, Member, IEEE, Senior Member, IEEE,
Nagaoka University of Technology, Japan
1603-1, Kamitomioka-machi
Nagaoka, Niigata, Japan
ntakaoka@stn.nagaokaut.ac.jp; thiroki@stn.nagaokaut.ac.jp; itoh@vos.nagaokaut.ac.jp

***Abstract* -- This paper proposes a bi-directional isolated single-phase matrix converter with a center-tapped transformer, which is used in a battery storage system connecting to a single-phase AC load. The proposed converter consists of a full bridge inverter, a high-frequency center-tapped transformer, and a matrix converter. The matrix converter is employed with a pulse density modulation in order to achieve zero-voltage switching (ZVS). On the other hand, a common mode voltage of the center-tapped transformer and a small capacitor are utilized in order to absorb the power ripple of the single-phase AC load without additional switches. Furthermore, the switches in the full bridge inverter partially achieve ZVS in order to reduce the switching loss. These characteristics result in a high-power-density converter. As the experimental results with a 1kW-prototype, the proposed converter reduces the DC current ripple generated by a single-phase AC load by 80.2% in the discharging mode, and 76.8% in the charge mode. Besides, the low AC side voltage THD in the discharge are below 3.0% over entire the AC power range.**

***Index Terms*-- Matrix converters, DC-AC power converters, Bidirectional power flow, Delta-sigma modulation;**

I. INTRODUCTION

Recently, photovoltaic (PV) and wind turbine systems have been actively researched for renewable energy [1-6]. Energy storage systems using batteries are required for power leveling in the renewable energy system due to the power fluctuation caused by weather condition. In these systems, bi-directional isolated DC-to-single-phase-AC converters are employed in order to provide a safe connection between the battery and the AC equipment. Downsizing and long life-time are desired features for such converters. A conventional converter constructed by a full bridge inverter as a primary converter, a high frequency transformer, and a secondary converter composed of a diode rectifier and an inverter, has been proposed in [7]. However, a bulky electrolytic capacitor is required in the secondary converter to smooth DC-link voltage. A bulky electrolytic capacitors limit converters to a short life-time. Therefore, this circuit topology restricts high power density and long life-time.

In last few years, several circuit topologies with the power decoupling capability have been proposed in order to eliminate the bulky capacitor [8-15]. However, these papers employ not only passive components but also additional switching devices for the power decoupling capability. It is limited the minimization and decreases the efficiency. In addition, an isolated type of DC to single-phase AC converter is compulsory in order to achieve the safety requirement. In order to avoid the additional switching devices, a power decoupling method using a center-tapped transformer and a small capacitor has been presented [16]. This topology does not need additional switches and can suppress significantly the ripple component in the input current caused by the single-phase AC load. However, this circuit topology cannot achieve the bi-directional power conversion because the authors in [16] constructs the isolated DC-to-single-phase-AC converter by using a diode bridge rectifier and a PWM inverter at the secondary side of the transformer. Thus, the application for the energy storage system in [16] is limited.

On the other hand, a matrix converter has attracted many attentions because no energy buffer stage is required, i.e. the elimination of the bulky electrolytic capacitor [17]. Thus, the matrix converter is expected to achieve smaller size and longer life-time compared to the conventional rectifier-inverter topology. Furthermore, the matrix converter can achieve the bi-directional power conversion. Therefore, the employment of the matrix converter together with the center-tapped transformer and the small capacitor can achieve for the requirements of the energy storage system, i.e. downsizing, long life-time, and bi-directional power conversion.

This paper proposes a bi-directional isolated DC-to-single-phase -AC converter, where a matrix converter and a center-tapped transformer are employed. The proposed converter does not require additional switching devices for the power decoupling capability, owing to the employment of the center-tapped transformer. In particular, a common mode voltage of the center-tapped transformer is generated to compensate the power ripple [18]. Furthermore, by applying a pulse density modulation (PDM) into the matrix converter, zero-voltage switching (ZVS) is achieved for all switches of the matrix converter. Besides, the switches of the full bridge inverter partially achieve ZVS, which further reduces the switching loss. This paper is organized as follows; in section II conventional and proposed topologies for the DC-to-single-

phase AC converter are introduced. In section III, the principle of the power decoupling in both direction, i.e. the charge and discharge mode of the battery, is explained. In section IV, the modulation methods of the converters in the primary and secondary side of the transformer are explained together with the mechanism of the ZVS achievement. Finally, in section V, the fundamental operation waveforms of the proposed system with discharging/charging operation modes are confirmed by simulations and experiments.

II. CIRCUIT TOPOLOGY

A. Conventional Circuit

Fig. 1 shows the conventional isolated DC-to-single-phase AC converter. The conventional circuit is comprised of a full bridge inverter, a high-frequency transformer and a rectifier-inverter topology. The full-bridge inverter at the primary side of the transformer outputs a high-frequency square voltage in order to reduce the volume of the transformer. The secondary-side rectifier converts the high frequency voltage to a DC voltage and the voltage-source inverter generates the grid current. When the grid current i_{grid} is sinusoidal waveform and the unity power factor is achieved, an instantaneous grid power p_{grid} is expressed by

$$\begin{aligned} p_{grid} &= \sqrt{2}V_{grid}\sin(\omega_o t)\cdot\sqrt{2}I_{grid}\sin(\omega_o t) \\ &= V_{grid}I_{grid}\{1-\cos(2\omega_o t)\} \\ &= P_{grid} - P_{grid}\cos(2\omega_o t) \end{aligned} \quad (1),$$

where V_{grid} is the root-mean-square values of the grid voltage, I_{grid} is the RMS value of grid current, P_{grid} is the average grid power and ω_o is the grid side angular frequency. A ripple component shown as the second term on the right side of (1) should be eliminated in order to obtain a constant DC current in the DC bus. Other topologies to absorb the power ripple, for example C-L-C topology, are not effective to reduce the volume of the conventional circuit [19]. Hence, this converter has to adopt a bulky electrolytic capacitor C_{dc} to absorb the power ripple. However, a bulky electrolytic capacitors limit converters to a short life-time.

B. Proposed Circuit

Fig. 2 shows the isolated DC-to-single-phase matrix converter using a smaller buffer capacitor. The matrix converter is employed as a secondary-side converter in order to eliminate the DC-link capacitor. In addition, the proposed circuit employs a center-tapped transformer, the role of which is not only to link the full bridge inverter to the matrix converter for isolation, but also to realize the power decoupling capability. In the buffer circuit, a buffer capacitor C_{buf} and an inductor L_{buf} is used to absorb the power ripple. In particular, the charge and the discharge of C_{buf} compensate the power ripple, whereas the inductor L_{buf} is used to control a buffer current i_{buf} which fluctuates the buffer capacitor voltage. The inductance of the buffer circuit is designed based on an allowable ripple current of the buffer current. Thus a higher

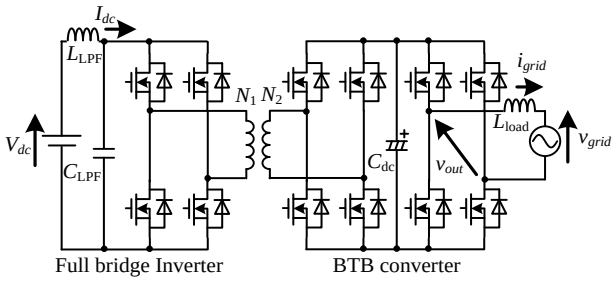


Fig.1. Conventional isolated DC-to-single-phase-AC converter. The conventional converter employs a bulky electrolytic capacitor C_{dc} to absorb the power ripple caused by the single-phase load.

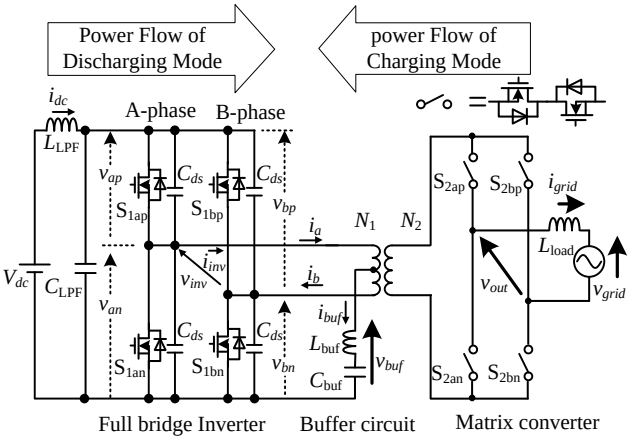


Fig.2. Proposed isolated DC-to-single-phase-AC converter. The secondary converter consists of the matrix converter in order to eliminate the DC-link smoothing capacitor.

inductance is not needed for the buffer circuit because capacitors for an active power decoupling typically accept large current ripple. In addition, the inductance of the buffer circuit can be small by using high switching frequency.

If the power ripple is absorbed by electric capacitors at a DC-link in the conventional system, the required capacitance in order to absorb the power ripple is decided by the ripple energy. Thus, the capacitor voltage ripple is presented by

$$\Delta E = \frac{1}{2}C\left\{(V_{ave}+\frac{\Delta V_c}{2})^2 - (V_{ave}-\frac{\Delta V_c}{2})^2\right\} \quad (2),$$

where E is a ripple energy caused by the single-phase AC side, C is a smoothing capacitor, V_{ave} is an average of a buffer capacitor voltage and ΔV_{c} is a fluctuation voltage of C. In the conventional method with a bulky electrolytic capacitor, and ΔV_{c} is designed to be small for a stable operation of an inverter. Therefore, in the power decoupling method using the bulky electrolytic capacitor, the large capacitance is required. Assuming the 1.5-kW conventional converter, the conventional converter needs an electrolytic capacitor of 2650 μF with a voltage ripple of 5% at the DC-link. In contrast, the same energy compensation capability is ensured by the fluctuated buffer capacitor voltage ΔV_{c} in the proposed method. Thus, the capacitance in the proposed system can be reduced. Note that in the center-taped transformer, the main power from the battery to the grid is controlled by the differential-mode

voltage, whereas the power ripple is absorbed by controlling the common-mode voltage in order to fluctuate the buffer capacitor voltage [18]. The inductance of the buffer circuit in the worst case is calculated by

$$L_{buf} = \frac{V_{dc} - v_{Cbuf}}{2\Delta i_L f_{sw}} \frac{v_{Cbuf} - \frac{V_{dc}}{2}}{V_{in}} \tag{3}$$

$$\Delta i_L = \frac{i_{buf\_ripple} / 2}{I_{buf\_max}} \tag{4}$$

where Δi_L is the allowable current ripple ratio, i_{buf_ripple} is the peak to peak value of the inductor current i_{buf}, V_{dc} is an average DC voltage and f_{sw} is the switching frequency of the AC link.

III. Power Decoupling Capability

When the battery is grid connected to the single-phase AC side, the DC input current i_{dc} includes a ripple component at twice of the grid frequency. In this section, the principle of the power decoupling for the bi-directional power flow, i.e. the charge and discharge modes of the battery, are explained.

A. Battery Discharging mode

Fig. 3 shows the relationship among the DC power, the instantaneous grid power p_{out} and the power decoupling with C_{buf} in the discharged mode. The buffer current i_{buf} is controlled to fluctuate the buffer capacitor voltage v_{Cbuf}, which then absorbs the power ripple caused by the single-phase AC load. First, the buffer capacitor energy W_{Cbuf} is derived as

$$\begin{aligned} W_{Cbuf} &= \int_{t_0}^{t} v_{Cbuf} i_{buf} d\tau = \int_{t_0}^{t} v_{Cbuf} \left(C_{buf} \frac{dv_{Cbuf}}{d\tau} \right) d\tau \\ &= \int_{t_0}^{t} P_{grid} \cos(2\omega_o \tau) d\tau \end{aligned} \tag{3}$$

by using (1) and the voltage–current equation of the capacitor. Where t_0 is the start time of the operation. Then, the buffer capacitor voltage v_{Cbuf} which absorbs the power ripple completely, is derived as

$$v_{Cbuf}{}^{*} = \sqrt{\frac{V_{dc}{}^{2}}{4} + \frac{P_{grid}}{\omega_o C_{buf}} \sin(2\omega_o t)} \tag{4}$$

from (3), where $V_{dc}/2$ is an initial voltage of C_{buf}. Finally, $i_{buf}{}^{*}$ is derived as

$$i_{buf}{}^{*} = C_{buf} \frac{dv_{Cbuf}{}^{*}}{dt} = \frac{P_{grid} \cos(2\omega_0 t)}{\sqrt{\frac{V_{dc}{}^{2}}{4} + \frac{P_{grid}}{\omega_o C_{buf}} \sin(2\omega_o t)}} \tag{5}$$

by using an grid power reference $P_{grid}{}^{*}$.

The power ripple in the discharging mode is compensated by regulate the buffer current into the current reference $i_{buf}{}^{*}$ as shown in (5).

B. Battery Charging Mode

Fig. 4 shows the relationship among the DC power, the instantaneous grid power p_{grid} and the power decoupling in the charging mode. Similarly, the buffer current regulation fluctuates the voltage of buffer capacitor v_{Cbuf}, which absorbs the power ripple caused by the single-phase load. However, the power flow is reverse compared to the discharging mode as described previously. Therefore, the buffer power p_{buf} which compensates the power ripple of the charging mode is derived by

$$p_{grid} = p_{in} - p_{buf} \tag{6},$$

$$p_{buf} = P_{grid} \cos(2\omega_o t) \tag{7}$$

corresponding to the power flow direction as shown in Fig. 2. Where the DC power p_{in} is equal the grid power $P_{grid.}$ Thus, the buffer capacitor voltage v_{Cbuf} is derived from

$$v_{Cbuf}{}^{*} = \sqrt{\frac{V_{dc}{}^{2}}{4} - \frac{P_{grid}}{\omega_o C_{buf}} \sin(2\omega_o t)} \tag{8}.$$

In summary, the buffer capacitor voltage v_{Cbuf} which absorbs the power ripple in both mode is decided by the power ripple

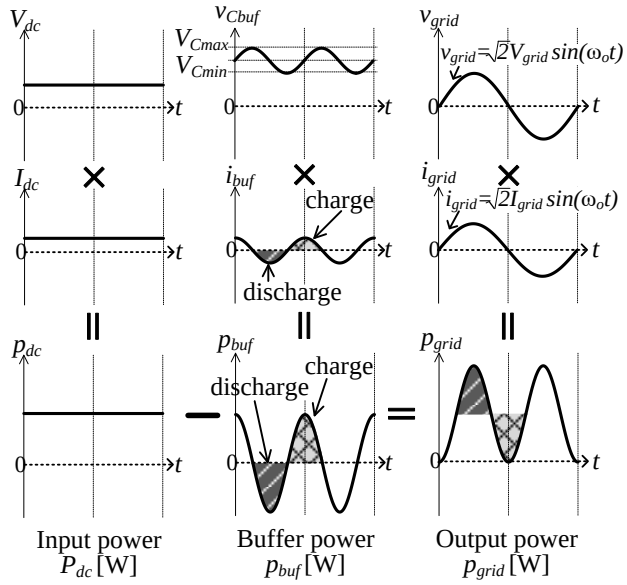


Fig.3. Principle of power decoupling capability with buffer capacitor in discharging mode. The buffer power to compensate the power ripple is charged or discharged at C_{buf}. Consequently, the DC input current without the ripple component is obtained.

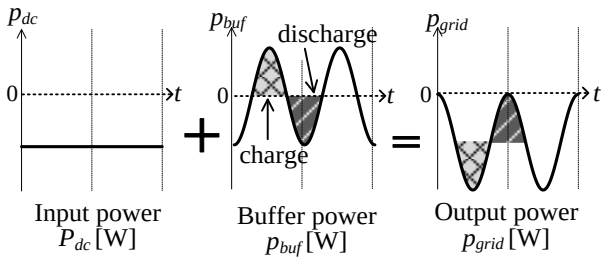


Fig.4. Principle of power decoupling with buffer capacitor in charging mode.

and the power flow. Hence, the buffer capacitor voltage can be controlled according to the power flow direction by detecting the polar of the grid power as shown in Fig. 3 and Fig. 4.

IV. Modulation Method

A. *Full Bridge Inverter*

The modulation for the full bridge inverter at the primary side of the transformer in the proposed converter is explained in this section. In the proposed converter, if the transformer current discharges completely the drain-to-source capacitor C_{ds} during dead time, the switching becomes ZVS. Note that if the buffer current flowing in the buffer circuit discharges C_{ds} during dead time, the switching also becomes ZVS. The ZVS achievement of the primary-side inverter depends on the operation mode of the secondary-side converter. When PDM is applied for the secondary-side converter, there are intervals when the secondary-side converter outputs the zero voltage and makes p-n line become open. In summary, two modes occur at the secondary side of the transformer; conduction mode and zero-voltage mode.

1) Conduction mode at secondary side of transformer

In this mode, the secondary-side converter does not generate the zero voltage. Therefore, the transformer current is flown continuously to the grid. In order to achieve ZVS in the primary-side inverter, the relationship among the buffer current i_{buf}, the output current of MC, i.e. the grid current $i_{grid,}$ and the currents in each arm of the full-bridge current $i_{a,}$ i_b is required.

In the conventional DC-to-AC converter without the buffer circuit, the grid current i_{grid} equals to the transformer current, i.e. i_{inv} or i_a, assuming that the exciting current is small enough to be neglected. Therefore, the switching devices achieving the ZVS are determined by the pole of the transformer current i_a. The relationship between the pole of the transformer current i_a and the ZVS-achieving switching devices is as follows.

$i_a > 0$: S_{an}, S_{bp} achieve ZVS

$i_a < 0$: S_{ap}, S_{bn} achieve ZVS

On the other hand, in the proposed converter, the transformer current overlaps with the common current. Thus, the currents i_a, i_b in each arm are presented by

$$i_a(t) = i_{dif}(t) + \frac{1}{2} i_{buf}(t) \quad (9),$$

$$i_b(t) = i_{dif}(t) - \frac{1}{2} i_{buf}(t) \quad (10),$$

where i_{dif} (t) is the transformer current which changes according to the output current of MC, and i_{buf}(t) is the buffer current in the buffer circuit, which changes according to the grid power. If the current i_a, i_b in each phase is below the lower limit value i_{lim} the charges in the drain-to-source capacitance C_{ds} cannot be discharged completely during dead time T_{dead}. The lower limit value i_{lim} which achieves ZVS in the primary side is presented by

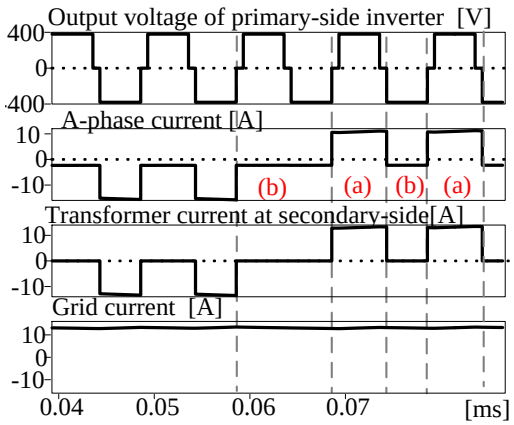


Fig. 5. Relationship between the phase current of the primary-side and the grid current. The phase current of the primary-side has two current mode; first, the condition mode (a) which the both of the buffer current and the grid current flow. Other is the zero-voltage mode which the buffer current flows to the primary-side of the transformer.

$$|i_{\lim}| \geq \frac{2C_{ds}V_{dc}}{T_{dead}} \quad (11).$$

Fig. 5 shows the relationship among the grid current, the transformer current and the voltage at the primary-side in one carrier period without the proposed power decoupling. The phase current of the primary-side has a two mode; first, the condition mode which the matrix converter does not generate the zero voltage, the transformer current and the buffer current are flowed to the primary-side of the transformer as shown the (a) range of Fig. 5. Other, the zero-voltage mode which the matrix converter generates the zero voltage, the buffer current is flowed to the primary-side of the transformer as shown the (b) of Fig.5. Thus, the current peak of the transformer without the buffer current component equal to the peak value of the grid current when m equals to the turn ratios of the transformer N_1/N_2. The condition which achieves ZVS at the primary-side inverter is presented by

$$|i_a| \geq |i_{\lim}| \quad (12),$$

$$|i_b| \geq |i_{\lim}| \quad (13).$$

In the (a) range of Fig.5, let the grid current be i_{grid} by (11)-(13), (9)-(10) are rewritten as

$$i_a(t) = m\frac{N_1}{N_2}\sqrt{2}I_{grid}\sin(\omega_o t) + \frac{1}{2}\frac{P_{out}\cos(2\omega_0 t)}{\sqrt{\frac{V_{dc}^{\ 2}}{4} + \frac{P_{out}}{\omega_o C_{buf}}\sin(2\omega_o t)}} \quad (14),$$

$$i_b(t) = m\frac{N_1}{N_2}\sqrt{2}I_{grid}\sin(\omega_o t) - \frac{1}{2}\frac{P_{out}\cos(2\omega_0 t)}{\sqrt{\frac{V_{dc}^{\ 2}}{4} + \frac{P_{out}}{\omega_o C_{buf}}\sin(2\omega_o t)}} \quad (15).$$

The current in each arm of the primary-side inverter is the sum of the buffer current and the output current in this mode as

shown the range (b) of Fig.5. Therefore, both the ZVS-achieving switching devices and the ZVS range are determined by the pole of transformer current, the buffer current and the phase $\theta = \omega_o t$.

In order to achieve ZVS in the primary-side inverter, the current i_a, i_b in each arm are required to be higher than the limit value, which enables. The limit current i_{lim} which achieves ZVS in the primary-side inverter is expressed as in

$$\left|i_{grid}\right| \geq \frac{2v_{Cbuf}\dfrac{C_{ds}}{T_{dead}}V_{dc} - P_{out}}{2v_{Cbuf}\,m\dfrac{N_1}{N_2} - v_{grid}} \quad (16).$$

2) Zero-voltage mode at secondary side of transformer

Fig. 6 shows the current path-way of the proposed converter when the matrix converter generates the zero voltage. In the conventional circuit without the buffer circuit, the secondary transformer current becomes zero. Therefore, the primary-side inverter cannot flow the transformer current in order to meet the ZVS achieving condition as in (16). On the other hand, in the proposed converter, by applying the center-tapped transformer and the buffer circuit as shown in chapter III the transformer current can still flow into the buffer circuit even during the zero-voltage mode at the secondary side of the transformer as shown the range of Fig.5. During this mode, the transformer current depends on the buffer current. Thus, the ZVS-achieving switching devices are decided by the grid current and the phase θ because the buffer current are dependent on the grid current i_{grid} (t). Note that, the ZVS condition of the ZVS-achieving switching devices which varies dependently on the grid current i_{grid} (t) and the phase θ are discussed by the simulation.

The current to discharge completely the drain-to-source capacitor C_{ds} has to meet (16). Therefore, the boundary condition of the buffer current to achieve ZVS at the primary-side inverter is expressed as in

$$\left|i_{grid}v_{grid}\right| \geq P_{out} - 4v_{Cbuf}\frac{C_{ds}}{T_{dead}}V_{dc} \quad (17)$$

using the grid current i_{grid} and (5).

Fig.7 shows the relationship between the phase current at the primary-side converter and the grid waveform. Note that the definition of the current flow is shown as in Fig. 2, the envelope curves of the each arm current do not include the

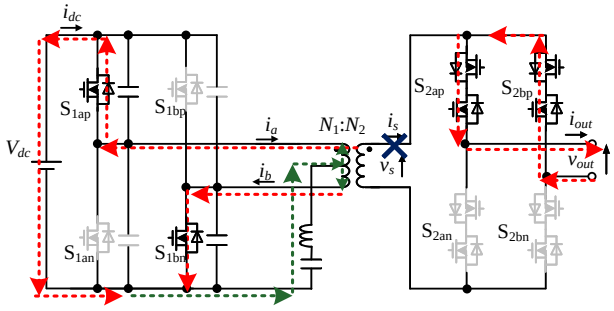


Fig. 6. Relationship between switching operation and current path in the proposed circuit when the matrix converter outputs zero voltage.

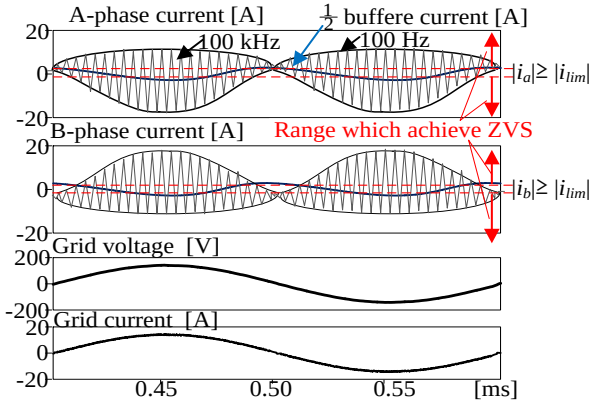


Fig. 7. Relationship between phase current at primary-side inverter and grid waveform. The limitation current i_{lim} and the range which achieves ZVS at the primary-side inverter is decided by i_{grid} and the phase θ as shown in (11)-(12).

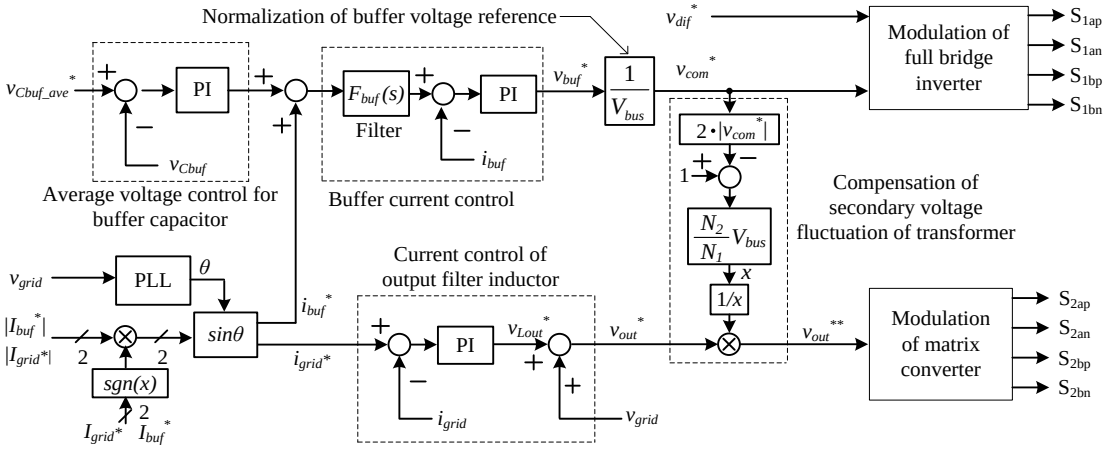


Fig.8. Control block diagram of proposed converter. The buffer current is controlled for the power decoupling. By PLL, the power flow direction is determined and the phase which is assigned to the grid current reference and the buffer current reference is calculated.

excited current. It is observed from Fig.7 that, if the current in each arm satisfies the condition of the ZVS achievement as in (16)-(17), the switching devices at the primary-side inverter can achieves ZVS. As a conclusion, this proposed converter can achieve both ZVS in the primary-side inverter and the power decoupling capability

B. Matrix Converter

Fig. 8 shows the control block diagram of the proposed converter. The current and voltage controls in the proposed method are realized with PI controllers. The full bridge inverter provides a differential-mode voltage to excite the transformer and a common-mode voltage to compensate the power ripple [18]. As shown in Fig. 8, the buffer current control for the power decoupling capability is employed in order to regulate the voltage of the buffer capacitor v_{Cbuf} which is used to absorb the power ripple caused by the single-phase AC load. The buffer current reference i_{buf}^* and the grid current reference i_{grid}^* are decided by the direction of the power flow in order to achieve the bi-directional power flow operation.

Fig. 9 shows the concept of the PDM method applied in the matrix converter as the secondary-side converter. The PDM generates the output voltage with the density and the polarity of the input voltage pulses. In Fig. 9, a half cycle of the input voltage pulses are used as the minimum unit of the output voltage waveform. All switching devices in the matrix converter are switched at the zero voltage interval of the secondary voltage of the transformer. Consequently, the matrix converter achieves ZVS which results in the decrease in the switching loss.

Fig. 10 shows the block diagram of the PDM based on the delta--sigma conversion [20]-[21]. A delta-sigma conversion is basically similar to an analog-digital conversion, which converts an analog signal into a digital signal of one bit. First, in the PDM, the quantization error is integrated by comparing the quantized grid voltage reference v_{out}* holding by Zero Order Hold (ZOH) and the quantizer output at one clock before. Note that the timing of the ZOH is synchronized to the peak of carrier in the matrix converter. The output signal of the quantizer changes when this integrated quantization error exceeds a threshold, which results in a switching. Because the switching signals do not depend on the carrier frequency of the matrix converter, the pulse density of the grid voltage changes continuously, which results in distributed pulses. Consequently, comparing to the conventional PDM method that outputs concentrated pulses, the grid voltage ripple becomes lower because the pulse is generated continuously in one carrier period [20].

V. SIMULATION AND EXPERIMENTAL RESULTS

Table I shows the simulation condition in order to verify the fundamental operation of the proposed converter with the power decoupling capability. When the ripple current ratio of the buffer circuit is less than 30% with the conditions shown

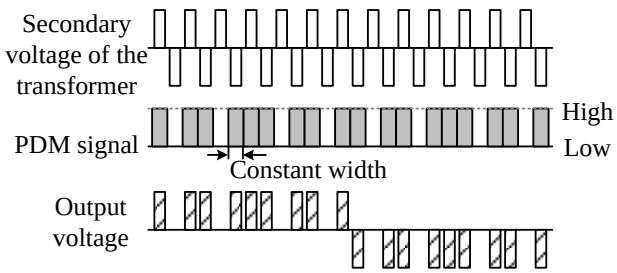


Fig.9. Concept of PDM method applied in matrix converter.

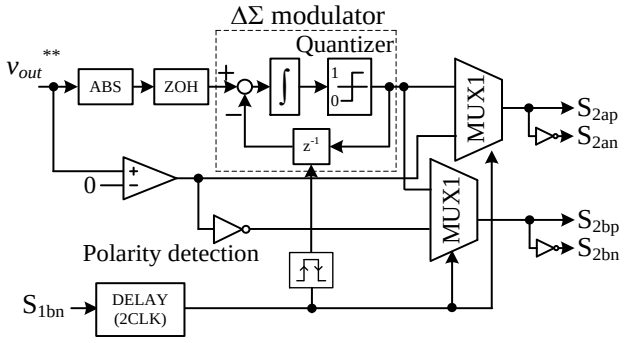


Fig.10. Block diagram of PDM based on delta-sigma conversion. This PDM reduces the quantization error and improves the output voltage distortion. The MUX consists AND and EXNOR. This MUX selects the switching phase of the matrix converter and synchronizes the on-off timing with the gate signal S_{1bn}.

TABLE I
SIMULATION CONDITION

DC bus voltage	380 V_{dc}	Grid voltage	100 V_{rms}
Rated power	1kW	Grid frequency	50 Hz
Buffer L (L_{buf})	2.0 mH	Buffer C (C_{buf})	200 μF
Grid connected inductor (L_{out})	2.0 mH (6.3%)	Turn ratio of transformer N_2/N_1	1.0
Natural angular frequency of buffer current control	4000 rad/s	Natural angular frequency of grid current control	4000 rad/s
Carrier frequency of full bridge inverter	100 kHz		

in table 1, the inductance of L_{buf} at 2.0 mH for convenience of the experiment.

A. Simulation results in discharging mode

Fig. 11 shows the input and grid waveforms in the discharging mode of at steady state. Fig. 11 (a) and (b) show results without/with the power decoupling, respectively. The DC input current is filtered by a LPF with a cut-off frequency of 1 kHz in order to remove a switching ripple. As shown in Fig.11 (a), the DC input current has a ripple component at 100 Hz caused by the single-phase load. The current ripple component at 100 Hz is 101% of the average current. In contrast, the current ripple component is reduced in Fig.10 (b) when the power decoupling capability is realized. As a result, the ripple of the DC input current is suppressed by 95.7%.

B. Simulation results in charging mode

1) Steady state

Fig. 12 shows the input and grid side waveforms in the charging mode at steady state. Fig. 12 (a) and (b) show results without/with the proposed power decoupling respectively. As shown in Fig. 12 (a), in the charging mode, the DC input current has a ripple component at 100 Hz caused by the single-phase load in the opposite direction compared with the discharging mode as shown in Fig. 12 (a). As a result, without the power decoupling in the charging mode, the current ripple component at 100 Hz is 102% of the average current. In contrast, the proposed power decoupling reduces the DC input current ripple by 82.3% as shown in Fig.12 (b). The effectiveness of the power decoupling is different between the discharging/charging modes because of the phase error of the grid current caused by PDM.

2) Charge and discharge mode transition

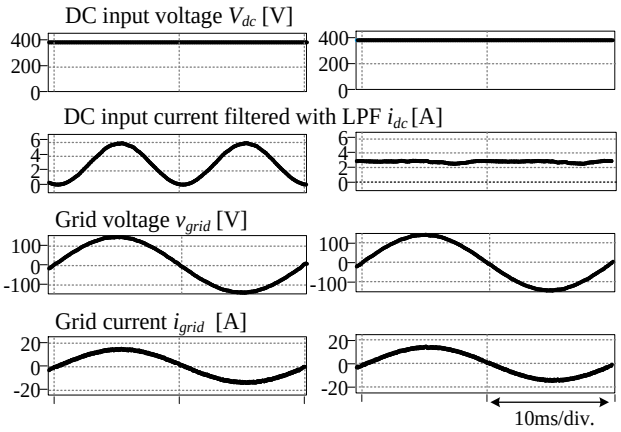
Fig. 13 shows the input and output waveforms in the mode transition when the charge and discharge mode alternates. The proposed power decoupling method can achieve the power decoupling capability even when the proposed system changes in the discharge or charge mode. Besides, the surge current which is generated at the moment of the power flow direction alternation can be absorbed by an input LC filter. In the other word, the proposed power decoupling always maintain the DC input current without the ripple for the battery.

C. Experimental results in discharging mode

Fig. 14 shows the experimental waveforms of the proposed converter with V_{dc} of 350 V, v_{grid} of 100 V_{rms} and an R-L load of 402 W. Fig. 14 (a) and (b) show results without/with the power decoupling, respectively. As shown in Fig. 14 (a), the buffer capacitor voltage does not vary because the full bridge inverter does not generate the common-mode voltage in the transformer. As a result, the DC input current has a high ripple component at 100 Hz. In contrast, the proposed power decoupling provides the common-mode voltage to fluctuate the buffer capacitor voltage. Consequently, the power ripple component in the DC current is suppressed greatly. Furthermore, the low grid voltage THD of 2.0% as shown in Fig.14 (b) is achieved by the PDM based on the delta-sigma conversion.

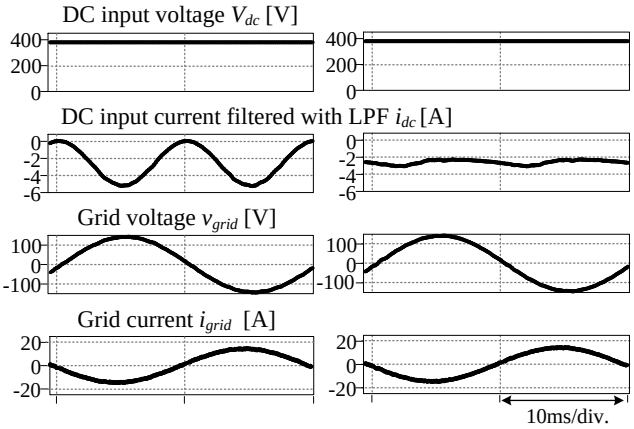
Fig. 15 shows the harmonic analysis of the DC bus current. Note that the fundamental harmonic is based on the output frequency of 50 Hz. From the result of Fig. 15, it is observed that without the power decoupling, the ripple component at 100 Hz is 59.1% of the average current, whereas the proposed power decoupling reduces the DC input current ripple by 80.2%. Therefore, these experimental results verified the effectiveness of the proposed power decoupling in the discharging mode.

Fig.16 shows the harmonic component of the DC input current and the grid voltage THD of the matrix converter. Note that the fundamental harmonic of the DC input current is 100 Hz, i.e. twice of the grid frequency, and the harmonic



(a) Without power decoupling method. (b) With power decoupling method.

Fig.11 Input and output waveforms in discharging mode at steady state. The proposed power decoupling reduces DC input current ripple by 95.7% in discharging mode.



(a) Without power decoupling method. (b) With power decoupling method.

Fig.12. DC and AC side waveforms in charging mode at steady state. The proposed power decoupling reduces DC input current ripple by 82.3% in charging mode.

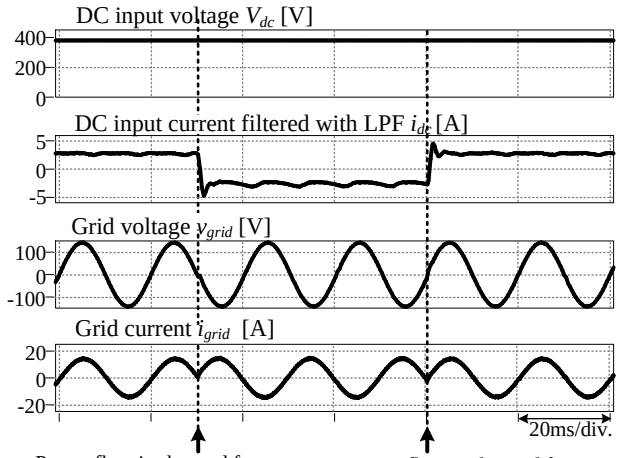


Fig.13. DC and AC side waveforms during charge and discharge mode transition.

amplitude is normalized by the DC component. It is observed from Fig. 15 that, the proposed power decoupling reduces the DC input current harmonic to 8.1% in maximum. In addition, when the proposed PDM based on delta-sigma conversion is applied for the secondary-side matrix converter, the output voltage THD of below 3.0% is achieved over entire the output power range.

D. Zero voltage switching operation in primary-side inverter

Fig. 17 shows the experimental waveforms of the gate-source voltage of S_{bn}, the drain-source voltage of S_{bn}, the inverter voltage V_{inv} and the grid current i_{grid}. Note that the operation condition of the circuit is as following; V_{dc} of 350 V, v_{grid} of 100 V_{rms}, T_{dead} of 500 ns and an R-L load of 500 W (50% rated power). It is observed from Fig. 17 that, the gate-source voltage of S_{bn} rises after the drain-source voltage drops in S_{bn} to zero due to the resonance between the drain-source capacitor of S_{bn} and the buffer inductor. In addition, the switching devices achieve ZVS when the condition of the output current value calculated by (16)-(17) is satisfied.

E. Experimental results in charging mode

Fig. 18 shows the experimental waveforms in the charge mode at the condition as following; V_{dc} of 350 V, v_{grid} of 100 V_{rms} and an R-L load of 500 W (50% rated power). As shown in Fig.18, the DC input current with very small ripple is achieved even in the charge mode. From the harmonic analysis result of Fig.18, the current ripple component at 100 Hz without the power decoupling method is 63.0% of the an average current. In contrast, with the power decoupling method in charging mode, the current ripple component at 100 Hz is reduced to 14.6%. Therefore, the bi-directional operation of the proposed converter is confirmed in experiments.

VI. CONCLUSION

This paper proposed a bi-directional isolated single-phase matrix converter with a center-tapped transformer, which provided the power decoupling capability for the battery energy storage systems. In the proposed converter, the bulky electrolytic capacitor was eliminated because the matrix converter was employed as the secondary-side converter. The power decoupling employed the center-tapped transformer and the small buffer capacitor without any additional switches. In this paper, the effectiveness of the power decoupling capability was confirmed in both the charge and discharge modes of the battery by simulations as first step. In simulation results, the propose d power decoupling reduced the DC input current ripple by 82.3% in the charge mode. In addition, the power decoupling reduced the DC input current ripple generated by the single-phase load to 80.2% in the discharge mode. Finally, the validity of the proposed power decoupling and the PDM based on delta-sigma conversion method for the matrix converter were also confirmed in experiments. In the future, the evaluation of the efficiency and the volume will be considered.

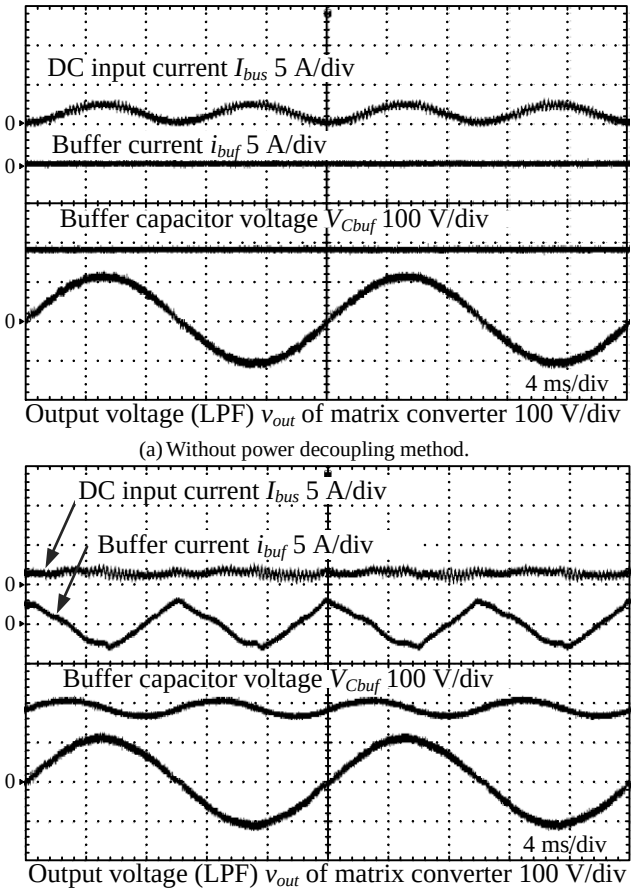


Fig. 14. Experimental waveforms in steady state. DC current with proposed power decoupling method do not have little harmonic component.

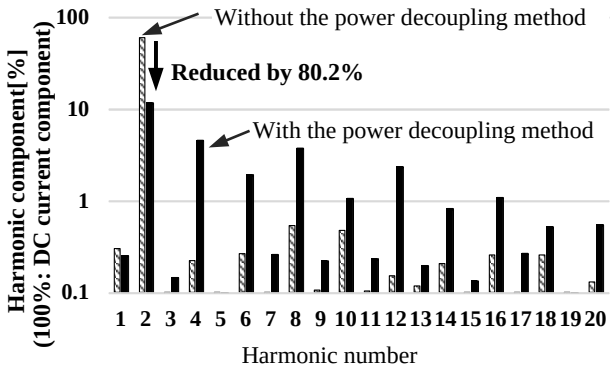


Fig.15. Experimental harmonic analysis of DC input current. It should be noted that harmonic number is based on output frequency of 50 Hz. Power decoupling method reduces DC input current ripple by 80.2%.

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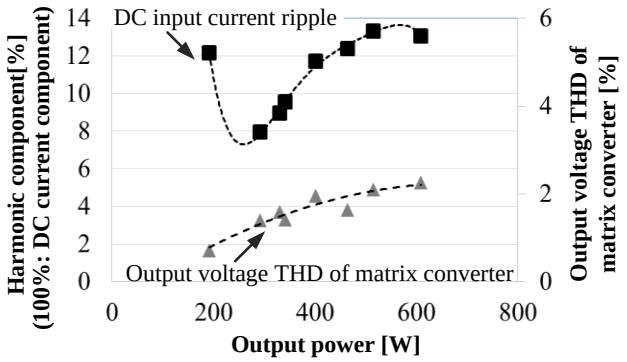

Fig.16. Harmonic component of DC input current and AC side voltage THD of matrix converter.

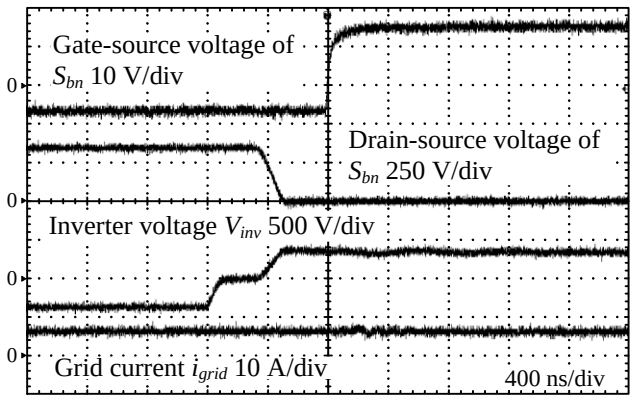

Fig.17. Experimental waveforms of gate-source voltage of S_{bn}, drain-source voltage of S_{bn}, inverter voltage V_{inv} and grid current i_{grid}. The gate-source voltage of S_{bn} rises after the drain-source voltage S_{bn} dropped to zero due to the resonance between the drain-source capacitor of S_{bn} and the buffer inductor.

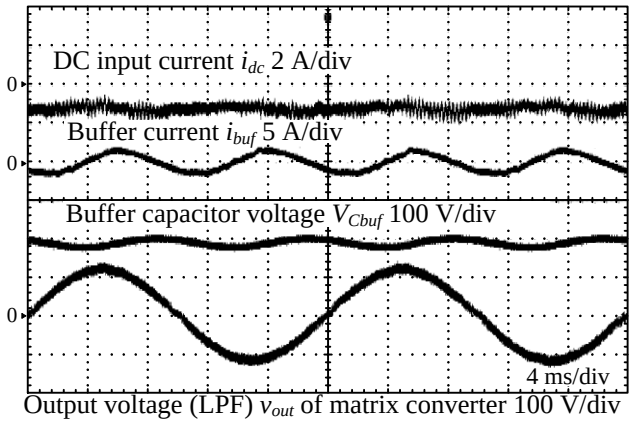

Fig.18. Experimental waveforms in charging mode.

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