Single-phase Solid-State Transformer using Multi-cell with Automatic Capacitor Voltage Balance Capability

Jun-ichi Itoh, Kazuki Aoyagi, Keisuke Kusaka and Masakazu Adachi
Department of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Niigata, Japan
itoh@vos.nagaokaut.ac.jp, aoyagi@stn.nagaokaut.ac.jp, kusaka@vos.nagaokaut.ac.jp,
m_adachi@stn.nagaokaut.ac.jp

***Abstract*- In this paper, a single-phase solid-state transformer (SST) system based on a multilevel topology using multi-cell is proposed. The proposed SST has an automatic capacitor voltage balancing capability on a primary side due to use of a resonant DC-DC converter. The main contribution of this paper is revealing the fundamental loss design of the proposed topology connected with a 6.6-kV grid. It is predicted that the maximum efficiency of full model SST reaches 99%. The miniature model SST is tested to confirm the fundamental operation with an input voltage of 1320 V, which is 1/5 of the full model. As a result, the sinusoidal input current is obtained with a total harmonic distortion of 4.3%. Besides, the bidirectional operation is verified. Then, it is confirmed that the primary side capacitor voltage of each cell is kept constant and balanced without a voltage balance control. Moreover, the loss analysis is derived in each part and compared with that of the experimental result. The error of the loss between the experimental result and the calculation is less than 5%.**

Keywords— Solid-State Transformer; Power factor correction converter; Resonant DC-DC converter; High-frequency transformer;

I. INTRODUCTION

Recently, a DC distribution system has been actively researched in order to achieve the energy-saving of the data-center or the large building [1] [2]. The DC distribution system is possible to achieve down-sizing and high efficiency compared with an AC distribution system [3]. Moreover, a 6.6-kV AC power grid is employed as one of the power sources.

In general, a transformer is applied between the AC power grid and the DC distribution system in order to achieve the step-down from 6.6 kV to the distribution voltage of several hundred volts and obtain galvanic isolation between the AC power grid and the DC distribution system [4] [5]. However, the conventional transformers are bulky and heavy because the transformers operate at a grid frequency, e.g., 50 Hz or 60 Hz.

As one of the solutions, a transformer-less converter is proposed [6]. In the five-level diode-clamped converter, the high voltage IGBTs with the voltage rating more than 4.5 kV are required. In addition, the balancing circuit is required as the auxiliary circuit in order to correct the unbalanced voltage among four capacitors in the DC link. Besides, it is operated by low switching frequency because the loss of high voltage rating devices is large compared to low voltage rating devices. Consequently, large passive components are required due to low switching frequency in order to suppress harmonic distortion of input current and voltage ripple of output DC voltage.

As another solution, solid-state transformers (SST) have been attracting attention [7]–[9]. SST is possible to significantly reduce the system volume compared to the conventional transformer by introducing high-frequency switching with the spread use of silicon carbide (SiC) and gallium nitride (GaN) devices [10]. SST simultaneously achieves the insulation and the step-down function by using a high-frequency transformer. To sum up, SST has following advantages [11]:

- Reduced size and weight of the system
- Harmonic suppression
- Active/ Reactive power control
- AC voltage adjustment
- DC voltage output

Besides, it is possible to compose the cell converters based on multilevel topologies, which enable to reduce a required voltage rating of the switching devices. The cell converters allow using switching devices with low on-state resistance and high-speed switching. In addition, the switching frequency is equivalently increased. Thus, the inductor volume can also be reduced [12]. Consequently, SST achieves high voltage rating with high switching frequency by multilevel topologies.

However, the number of the switches still increases greatly due to the multistage cell. Moreover, the control system, which drives the main circuit, is complicated because the number of the gate signal is increased with increased number of the switch [13]. Moreover, a balance control for each capacitor on the cells is required in the multilevel system, e.g., modular multilevel converter (MMC) [14]. The balance control may cause an unstable if a feedback control has a delay due to isolation or signal transmission [15]. Furthermore, the DC link capacitor with a large capacitance is required in order to maintain the constant capacitor voltage in each cell [16].

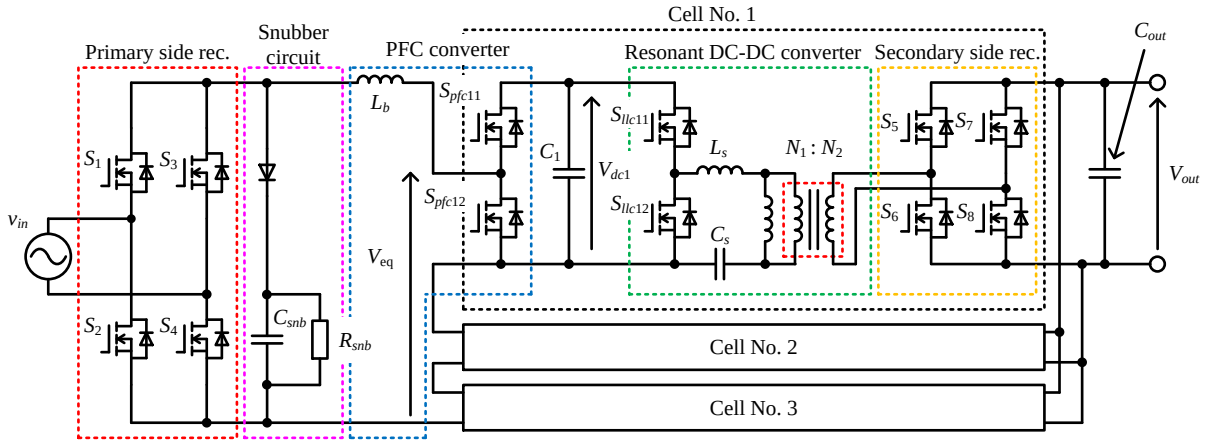


Fig. 1. Circuit configuration of proposed bidirectional single-phase SST.

In this paper, a simple circuit configuration of the single-phase SST is proposed. The proposed SST, which achieves capacitor voltage balance among cells without a complex voltage balance control with small primary side capacitor. Additionally, the proposed circuit reduces the number of the switching devices compared to the conventional circuit. The originalities of in this paper are proposing a new SST topology and the automatic voltage balancing method using a resonant DC-DC converter, which is connected in parallel in the secondary side. The contributions of this paper are that the volume of system is reduced and the control is simple. The proposed SST system is experimentally tested under a derating voltage of 1320 V which is 1/5 of the full model. In addition, the bidirectional operation is verified with the input voltage of 200 V to validate a loss distribution. Then, the proposed SST is designed for a 6.6-kV grid as the input voltage.

II. System Configuration of Proposed SST

A. Circuit configuration

Figure 1 shows the circuit configuration of the proposed SST. At the primary side, the output of the full bridge rectifier is connected to all cells in series. The devices with high voltage rating are required on the primary side. However, it is possible to use the devices with the slower switching speed because these switches are operated at the grid frequency. This system is characterized by a multi-cell input stage based on the full bridge rectifier. Each cell consists of a boost-type power-factor-correction (PFC) converter and a resonant DC-DC converter. PFC converter controls the input current to sinusoidal waveform with the unity power factor. Moreover, the rectified voltage is equally divided among each PFC converter because each cell at the primary side is connected in series. Thus, the voltage per cell is reduced. Consequently, at the primary side, it is possible to apply the switching device with low voltage rating and low on-state resistance. In the resonant DC-DC converter, the volume of the transformer is reduced because the transformer operates at high frequency.

In addition, a large capacitor is used in the output of a general PFC converter. In this system, small capacitors is used because the proposed circuit decouples a power pulsation at twice the grid frequency in the secondary side.

TABLE I. Comparison of Switching Device between Conventional SST and Proposed SST.

Rated Voltage	Number of cell	Number of Switching devices	
		Conventional SST (PWM rec. + DAB)	Proposed SST
3.3 kV	6	72	52
1.7 kV	11	132	92
1.2 kV	16	192	132

Table I shows the comparison of the switch number between the proposed SST and the conventional SST which includes a PWM rectifier and a dual active bridge converter [17]. Note that the number of cell is calculated by the rated voltage of the switch. As shown in table 1, the number of devices is reduced by 30% compared to conventional SST. The reason is because the proposed SST uses only one rectifier for each cell. Consequently, the proposed circuit increases the utilization rate of circuit compared the MMC.

B. Control system

Figure 2 shows the control block diagram of the proposed circuit. The proposed control includes an automatic current control (ACR) for the boost inductor current. In the ACR, the boost inductor current is controlled into full wave rectified waveform in order to correct the power factor of the grid side. Hence, the inductor current command value I_L^* is given by

$$I_L^* = I_{amp}\left|\sin(\omega t)\right| \quad \text{.....(1),}$$

where I_{amp} is the amplitude command value of the boost inductor current. Inductor current command I_L^* is generated by the multiplication of I_{amp} and the full-wave rectified waveform with same phase as the input voltage.

In the triangular wave comparator, the gate signal for PFC is generated by phase shifted carriers. Thus, the input voltage is equally divided because the switching timing is different. In addition, it is possible to use the switching device with low voltage rating. Note that the ripple current is reduced because the inductor voltage is reduced by the

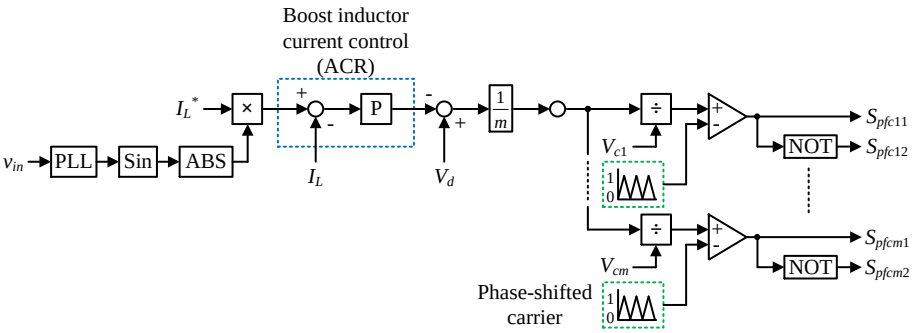


Fig. 3. Control block of PFC converter in proposed circuit.

series connection in the PFC converter. Then, the phase shift angle θ is given by (2).

$$\theta = \frac{2k}{m}\pi \ \ (k = 0, 1, \cdots, m-1) \quad \text{..... (2)}$$

Meanwhile, the balance control of the primary side capacitor voltage V_{dc1} is not required in this system. The voltage of the primary side capacitor may be imbalanced due to the variation of capacitances or a difference of transient response in general multilevel topology. However, due to the parallel connection of the resonant DC-DC converters, which is operated with constant duties, at the secondary side, the output voltage of each cell is automatically adjusted. Consequently, the primary side capacitor voltage is naturally clumped by the voltage which is decided by the turn ratio and the secondary voltage because the cell with low voltage is fed more power from the cell with high voltage. Thus, the voltage management on the high-voltage side is not required.

Figure 3 shows the switching pulse generation of the primary side rectifier. The switching pulse is generated by comparing the input voltage v_{in} and the thresholds voltage of positive/negative (V_{thp}/V_{thn}). The switching states are following:

- $v_{in} > V_{thp}$
  Turn on S_1 and S_4
  Turn off S_2 and S_3
- $v_{in} < V_{thn}$
  Turn on S_2 and S_3
  Turn off S_1 and S_4
- $V_{thn} < v_{in} < V_{thp}$
  Turn off S_1, S_2, S_3, and S_4

In the power running operation, the current flows the body diode of MOSFET. In the case of regeneration operation, the current flows the snubber circuit.

Table II shows the switching state of the primary side rectifier, the resonant DC-DC converter, and the secondary side rectifier. In the primary side rectifier, the switching frequency is set to the grid frequency in order to achieve the polarity inversion. In the resonant DC-DC converter, the switching frequency is set to the resonant frequency in order to achieve ZCS, and the switches are modulated with duty ratio of 50%. Hence, the closed-loop control for the resonant DC-DC converter is unnecessary. Consequently, the control is simple in this system because the current

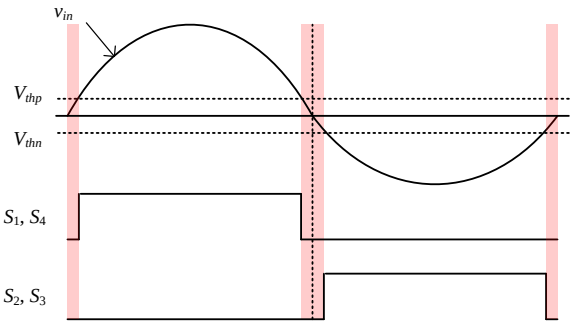


Fig. 2. Pulse generation for primary side rectifier.

TABLE II. SWITCHING MODE OF RESONANT DC-DC CONVERTER AND RECTIFIER.

	$S_1 \sim S_4$	$S_{llc11} \sim S_{llc12}$	$S_5 \sim S_8$
Switching frequency	50 Hz	50 kHz (= f_o)	
Duty ratio	50%		

control is achieved by only the switches of PFC (S_{pfc}). In the secondary side rectifier uses the switching pulse synchronized with the resonant DC-DC converter.

III. DESIGN OF PROPOSED SST

A. Snubber circuit

In the proposed SST, a snubber circuit is used in order to achieve the bidirectional operation. At regeneration operation, the continuous current flow is secured because the boost inductor current flows into the snubber circuit during the dead-time. Moreover, the snubber circuit also has to absorb all energy which is generated in the boost inductor when all gates are off with over current detection. Thus, the capacitor of the snubber circuit is given by

$$C_{snb} \geq \frac{L_b I_{\max}^2}{\Delta V^2} \quad \text{.....(3),}$$

where I_{max} is current at over current detection, ΔV is voltage rise value of capacitor. The resistor of the snubber circuit is given by

$$R_{snb} \leq \frac{2V_{clamp}^{\ 2}}{L_b I_{\max}^2 f_{sw\_rec}} \quad \text{.....(4),}$$

where f_{se_rec} is the switching frequency of the primary side rectifier, and V_{clamp} is the clamp voltage. The clamp voltage is designed to have a margin with respect to the rated voltage of device. In the miniature model SST, the margin is 20%.

B. Power-factor-correction (PFC) converter

The boost converter corrects the power factor of the grid side because the boost inductor current is controlled into full-wave rectified waveform same as general PFC circuit [18] [19]. The boost inductor L_b in the PFC circuit is given by

$$L_b = \frac{\sqrt{2}V_{in}}{4 f_{eq} \Delta I_{Lb}} \quad \text{..... (5)},$$

where ΔI_{Lb} is the ripple current of the inductor current, and f_{eq} is the equivalent switching frequency of the output voltage V_{eq}. Then, the equivalent switching frequency f_{eq} is given by

$$f_{eq} = m \times f_{sw} \quad \text{..... (6)},$$

where m is the number of cells, f_{sw} is the switching frequency of the PFC circuit. Each cell is operated by phase-shifted carrier. Consequently, the switching frequency component in V_{eq} is increased in proportional to the number of cells. Thus, the size of the boost inductor is reduced because the inductance is inversely proportional to frequency.

C. Resonant DC-DC converter

The resonant DC-DC converter generates a high-frequency voltage for the isolated transformer [20]. The high-frequency operation leads to the minimization of the isolation transformer. In addition, the zero current switching (ZCS) is achieved by the series resonance between the inductor L_s and the capacitor C_s. ZCS greatly reduce the switching loss of the proposed SST system.

Furthermore, the leakage inductance is designed to be negligibly smaller than the excitation inductance. Then, the switching frequency f_o of the resonant DC-DC converter is given by (7). From resonance frequency, and the duty ratio of the switch is set to 50%.

$$f_o = \frac{1}{2\pi\sqrt{L_s C_s}} \quad \text{..... (7)}$$

In the proposed SST, the operation mode is always the boost operation with respect of the primary side voltage. Thus, the turn ratio of the transformer is designed by

$$N = \frac{N_1}{N_2} \geq \frac{\sqrt{2}V_{in}}{2m\lambda V_{out}} \quad \text{..... (8)},$$

where N_1 and N_2 are the number of turns for primary/secondary side of the high-frequency transformer, V_{in} is the input voltage, V_{out} is the output voltage, and λ is the modulation index of the boost converter.

TABLE III. CIRCUIT PARAMETER OF PROPOSED SST FOR THE MINIATURE MODEL

Parameter	Symbol	Value
Input voltage	v_{in}	1320 V_{rms}
Rated output power	P_{out}	2 kW
Rated output voltage	V_{out}	320 V
Snubber capacitor	C_{snb}	0.2 μF
Sunbber resistance	R_{snb}	2.5 MΩ
Boost inductor	L_b	24 mH (%Z = 0.87%)
Primary side capacitor	C_1	48 μF
Resonant capacitor	C_s	204 nF
Leakage inductor	L_s	50 μH
Secondary side capacitor	C_{out}	8200 μF
Switching frequency of rec.	f_{sw_rec}	50 Hz
Switching frequency of PFC	f_{sw_pfc}	10 kHz
Resonant frequency	f_o	50 kHz
Number of cells	m	3
Trans turns ratio	N_1/N_2	1.0

IV. EXPERIMENTAL RESULTS

A. Power running operation

Table III shows the specifications and the circuit parameters. In this experiment, the fundamental operation is verified with the input voltage of 1320 V which is 1/5 of the full model. The prototype has three cells.

Figure 4 shows the waveforms of the input voltage, the input current, and the output voltage. The operation of the miniature model without the any large distortion is confirmed. At the input side, it is confirmed that the unity power factor between the input voltage and the input current is achieved. The input current THD is 4.3% at the rated load. At the output side, the step-down operation is achieved because the output voltage is regulated to 320 V.

Figure 5 shows the primary side capacitor voltage of each cell when the output power is changed from 0.8p.u. to 1.0p.u. (2 kW). It is observed that the primary side capacitor voltage is balanced even during transient response. Moreover, the maximum value of the primary side capacitor voltage also shows same value for all cells. Thus, it is confirmed that the primary side capacitor voltage is balanced among all cells without the balance control even when the output power suddenly changes.

Figure 6 shows the output voltage of all cells. From Fig. 6(a), the input voltage is equally divided to each cell because the output voltage of all cells forms balanced multilevel waveform. In Fig. 6(b), it is also confirmed that the equivalent switching frequency f_{eq} is 30 kHz. The equivalent switching frequency is determined by the switching frequency in PFC and the number of the cells.

Figure 7 shows the relationship between efficiency and input power factor. The maximum efficiency is 89.5% at the rated load. The reason is that the percentage of loss in devices against the power becomes low. The input power

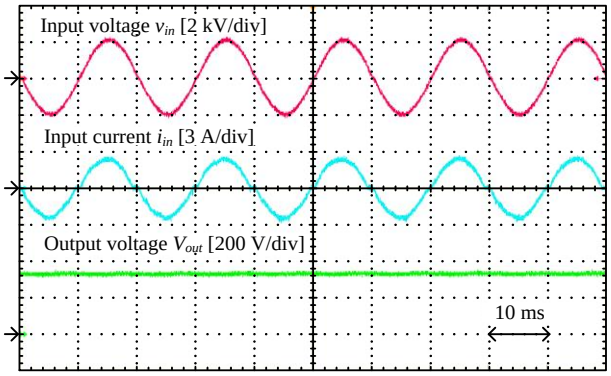


Fig. 4. Operation waveform at power running.

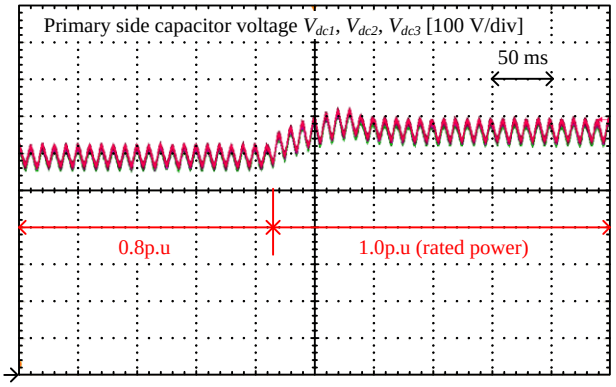


Fig. 5. Primary side capacitor voltage in each cell.

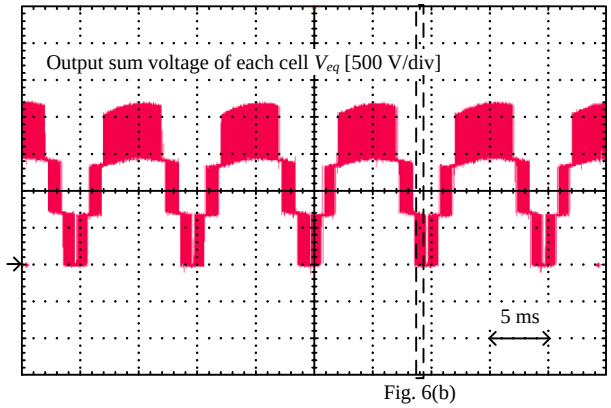
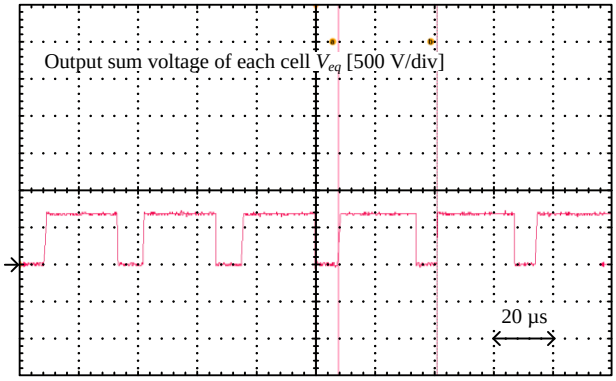


Fig. 6(b)

(a) Whole figure



(b) Enlarged figure

Fig. 6. Output voltage of all cells at power running.

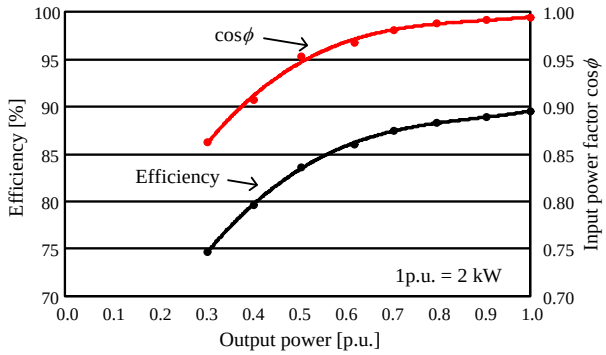


Fig. 7. Characteristic of efficiency and power factor.

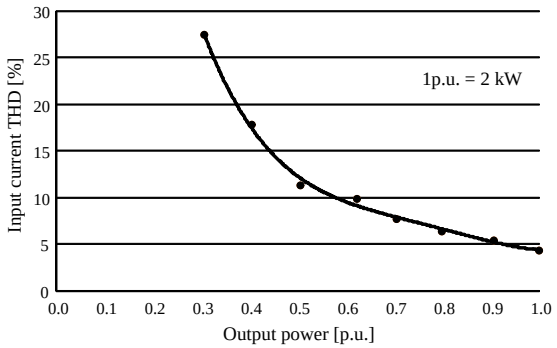


Fig. 8. Characteristic of input current THD

factor is over 0.95 with the output power from 0.5p.u. to 1.0p.u.

Figure 8 shows the relationship of the input current THD and the output power of the SST. It is confirmed that the input current THD is large when the output power is low. The reason is that the rate of the low-order harmonics component appears remarkably with respect to the fundamental component because the input current is low when the output power is low.

B. Bidirectional operation

In this experiment, the miniature model SST is tested to confirm the fundamental operation with the input voltage of 200 V due to the limitation of the experimental facilities. Note that the regeneration power supply is connected to the output side in order to achieve the regeneration operation.

Figure 9 shows the bidirectional operation of SST when the switching from power running to regeneration is tested. In the power running operation, it is confirmed that the unity power factor between the input voltage and the input current is achieved. On the other hand, it is confirmed that the input current is reversed against the input voltage in the regeneration operation. The input current THD of 4.2% is also confirmed. In the output sum voltage of each cell, it is confirmed that the waveform is four-level staircase voltage. Furthermore, an equivalent switching frequency f_{eq} of 30 kHz is also confirmed. Thus, the stable operation of the miniature model without the any large distortion is achieved even when the operation abruptly changes.

Figure 10 shows the primary side capacitor voltage of each cell in the bidirectional operation. It is observed from the waveform that the primary side capacitor voltage is balanced among all cells without the balance control even when the operation changes abruptly.

V. Loss Analysis and Estimation for Full Model

From Fig. 1, the loss of SST is separated following components:

(i) Primary side diode bridge
(ii) Switching devices of PFC converter
(iii) Switching devices of the resonant DC-DC converter
(iv) Secondary side rectifier

Table IV shows the selected devices in each part. In the proposed SST, the rated voltage of 3.3 kV is used in the primary side rectifier.

The current which flows into the electrolytic capacitor includes not only the power ripple component but also the switching frequency component from the inverter. Thus, it is very difficult to derive analytically. Hence, the capacitor ripple current is derived by simulation [21]. The capacitor ripple current is the function of the output power factor angle φ and the modulation index λ, which is a nonlinear value. Then, the effective value of the capacitor ripple current is given by

$$I_{rms\_cap} = K_{cap}(\varphi, \lambda) I_{out} \quad \text{..... (9),}$$

where I_{out} is the average value of the output current, and K_{cap} is the coefficient which is obtained by the simulation.

Figure 11 shows the simulation result of K_{cap}. The modulation index , which expresses the ratio of the voltage per cell and the dc-link voltage, is 0.94 in the miniature model SST. Therefore, from Fig. 11, K_{cap} (1.0, 0.94) is 0.83.

A. Primary side diode bridge

The loss of switches, which is calculated by the on-voltage of the switch and the current through the switch, is given by

$$P_{con} = \frac{1}{2\pi}\int_0^{\pi} v_{on}\, i_{sw}\, d\omega t \quad \text{..... (10),}$$

where v_{on} is the on-voltage of the switch, i_{sw} is the current through the switch. In this case, v_{on} and i_{sw} are given by.

$$v_{on} = r_{on}\sqrt{2}\frac{P}{V_{in}}\sin(\omega t) + v_0 \quad \text{..... (11),}$$

$$i_{sw} = \sqrt{2}\frac{P}{V_{in}}\sin(\omega t) \quad \text{..... (12),}$$

where r_{on} is the on-resistance of the switch, P is the rated power of SST. In (11), v_0 is defined as zero because the MOSFETs are used in the prototype. Moreover, the phase difference between the input voltage and the input current

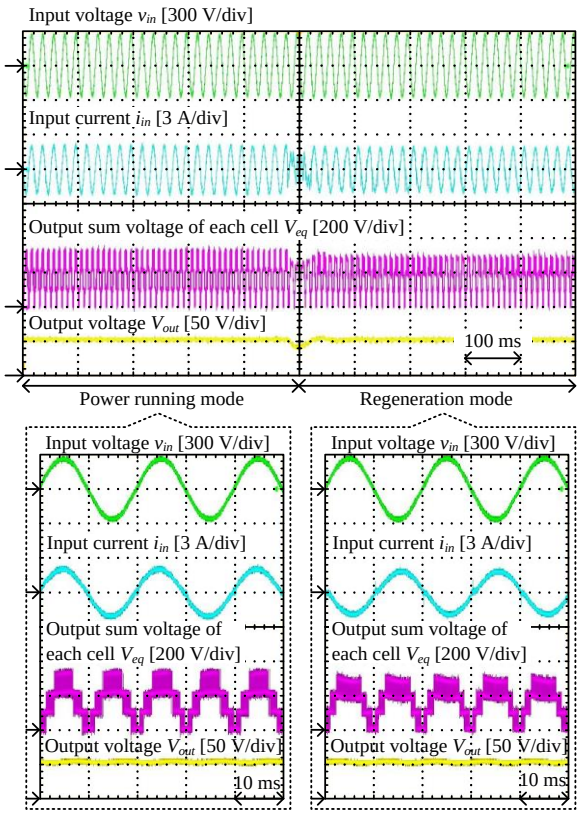


Fig. 9. Bidirectional operation of proposed circuit.

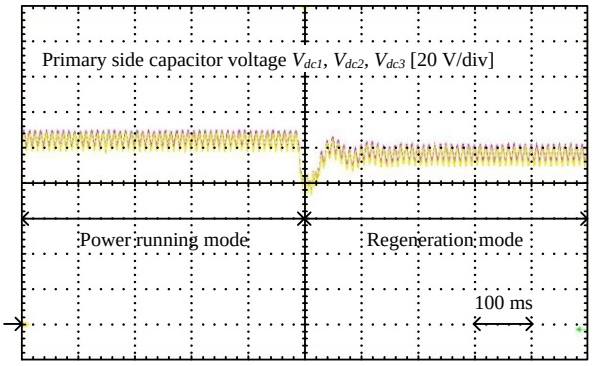


Fig. 10. Primary side capacitor voltage of each cell at bidirectional operation.

is not considered because the power factor is 1. The loss of the switches in the primary side rectifier is given by (13).

$$P_{con\_pri\_rec} = \frac{1}{2} r_{on}\left(\frac{P}{V_{in}}\right)^2 \quad \text{.....(13)}$$

B. PFC converter

The conduction loss of the switches in PFC is given by

$$P_{con\_PFC} = \frac{1}{2} r_{on} I_L^2 \quad \text{.....(14),}$$

where I_L is the current effective value through the boost inductor.

On the other hand, the switching loss of the switches, which is assumed that it is directly proportional to the voltage and the current of the switch, is given by

$$P_{sw\_PFC} = \frac{1}{\pi}\frac{e_{on}+e_{off}}{E_{nom}I_{nom}}\frac{V_{dc}}{V_{cell}}\frac{P}{m}f_{sw} \quad \text{..... (15),}$$

where V_{dc} is the voltage of the primary side capacitor, P is the rated power, m is the number of cell, f_{sw} is the carrier frequency, e_{on} and e_{off} are the turn-on and the turn-off energy per switching from datasheet, E_{nom} and I_{nom} are the voltage and the current under the measurement condition of the switching loss from the datasheet, and V_{cell} is the input voltage of each cell.

C. Resonant DC-DC converter

The loss of switches in the resonant DC-DC converter is only the conduction loss because ZCS assume achieving over all operation regions.

Therefore, the conduction loss is given by

$$P_{con\_LLC} = \frac{1}{2}R_{on}\left(\frac{N_2}{N_1}\right)^2\frac{I_{out}^2 - I_{rms\_cap}^2}{m^2} \quad \text{..... (16).}$$

At the secondary side, the conduction loss is given by

$$P_{con\_sec\_rec} = \frac{1}{2}R_{on}\frac{I_{out}^2 - I_{rms\_cap}^2}{m^2} \quad \text{..... (17).}$$

D. High-frequency transformer

Iron loss, which occurs in the high-frequency transformer, is calculated by the magnetic flux density and the characteristic of the core. The AC magnetic flux density B_{ac} is given by

$$B_{ac} = \frac{V_{out}}{4 f_o A_e N} \quad \text{..... (18),}$$

where A_e is the effective cross-section of the core, and N is the turns ratio of the transformer. The core loss value is given by the characteristic graph between the core loss value vs. the magnetic flux density, which is obtained from the core material, and the magnetic flux density which is calculated from (19). Therefore, the iron loss is given by

$$P_{iron\_loss} = P_{cv}V_e \quad \text{..... (19),}$$

where V_e is the effective volume of core.

The high frequency transformer of full model SST is designed by Gecko MAGNETICS which uses improved-improved Generalized Steinmetz Equation (i^2GSE) in order to calculate the iron loss of the transformer [22]. Consequently, it is possible to select the optimum core shape, core material and winding shape. From the analysis of Gecko MAGNETICS, it is confirmed that the loss is minimum by using EPCOS N95 as the core in the full model SST.

TABLE IV. SELECTED DEVICES OF PROTOTYPE FOR BIDIRECTIONAL OPERATION.

Circuit topology	Part	Type	Maximum ration
Single-phase rectifier	$S_1 \sim S_4$	-	3300 V
PFC converter	$S_{pfc11} \sim S_{pfc12}$	SCT2080KE	1200 V 40 A
Resonant DC-DC converter	$S_{llc11} \sim S_{llc12}$		
Secondary side rectifier	$S_5 \sim S_8$		

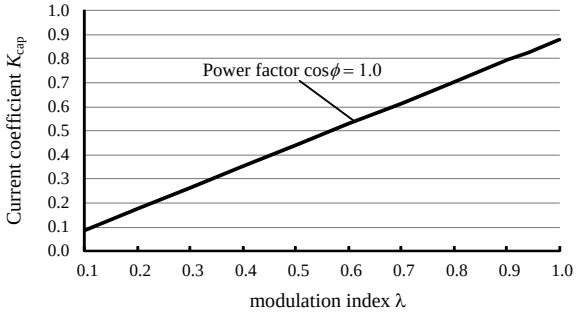


Fig. 11. Current coefficient of output capacitor.

E. Loss distribution

Figure 12 shows the loss distribution obtained from the experiment and the calculation of the bidirectional operation. Note that the loss is normalized with the experimental loss as 100%. The error of the loss between the experiment and the calculation is less than 5%.

Figure 13 shows the loss distribution of the full model SST. The loss distribution is calculated with assuming 6.6-kV input voltage and a 10-kVA rated power. Then, the number of cells is 15 because 1.2-kV switching devices can be used. From this consideration, a 99% efficiency at the rated power is expected. Moreover, it is possible to reduce the loss by applying synchronous rectification in the secondary rectifier.

VI. CONCLUSION

This paper has proposed a miniature model SST, which has a capacitor voltage balance capability without a control. The fundamental operation of SST was confirmed with the input voltage of 1320 V which is 1/5 of the full model from the experimental results. As a result, the sinusoidal waveform of the input current was obtained without any large distortion at the primary side. In addition, the bidirectional operation is confirmed in the proposed SST with the input voltage of 200 V. Furthermore, the average voltage of the primary side capacitor are stable and balanced among all cells without a voltage balance control.

Finally, the loss equation was derived at each part of the system and compared with experimental result. As a result, the error of the loss between the experimental result and

the calculation is less than 5%. It is predicted that the maximum efficiency of full model SST is 99%.

REFERENCES

[1] T. Tanaka, Y. Takahashi, K. Natori, and Y. Sato ”High-Efficiency Floating Bidirectional Power Flow Controller for Next-Generation DC Power Network,” IEEJ J. Industry Applications, vol. 7, no. 1, pp. 29-34, (2018)

[2] R. Chattopadhyay, S. Bhattacharya, N. C. Foureaux, A. M. Silva, B. Cardoso F., H. de Paula, I. A. Pires, P. C. Cortizio, L. Moraes, and J. A. de S. Brito: “Low-Voltage PV Power Integration into Medium Voltage Grid Using High-Voltage SiC Devices,” IPEC 2014, pp.3225-3232, (2014)

[3] T. Nakanishi, K. Orikawa, J. Itoh: “Modular Multilevel Converter for Wind Power Generation System Connected to Micro-Grid,” ICRERA2014, No. 219, (2014)

[4] L. Wang, D. Zhang, Y. Wang, B. Wu, and H. S. Athab: “Power and Voltage Balance Control of Novel Three-Phase Solid-State Transformer Using Multilevel Cascaded H-Bridge Inverters for Microgrid Application,” IEEE Trans. On Power Electronics, Vol. 31, No. 4, pp.3289-3301, (2016)

[5] T. Nakanishi, and J. Itoh, ”Control Strategy for Modular Multilevel Converter based on Single-phase Power Factor Correction Converter,” IEEJ J. Industry Applications, vol.6, no.1, pp.46-57, (2017).

[6] N. Hatti, Y. Kondo, and H. Akagi, “Five-Level Diode-Clamped PWM Converters Connected Back-to-Back for Motor Drives,” IEEE Trans. On Industry Applications, Vol.44, No.4, pp.1268-1276, (2008)

[7] M. Nakahara, and K. Wada, “Loss Analysis of Magnetic Components for a Solid-State-Transformer,” IEEJ Journal of Industry Applications, Vol.4, No.7, pp.387-394, (2015)

[8] D. Ronanki, and S. S. Williamson: “Evolution of Power Converter Topologies and Technical Considerations of Power Electronic Transformer based Rolling Stock Architectures,” IEEE Trans. On Transportation Electrification, (2017)

[9] X. Yu, X, She, X. Zhou and A. Q. Huang: “Power Management for DC Microgrid Enabled by Solid-State Transformer,” IEEE Trans., Vol.5, No.2, pp.954-965 (2014)

[10] A. Q. Huang, Q. Zhu, L. Wang, and L. Zhang, “15 kV SiC MOSFET: An Enabling Technology for Medium Voltage Solid State Transformers,” CPSS Trans., Vol.2, No.2, pp.118-130 (2017)

[11] J. W. Kolar and G. Ortiz: “Solid-State-Transformers: Key Components of Future Traction and Smart Grid Systems”, IPEC 2014, pp.22-35 (2014)

[12] T. Nakanishi, and J. Itoh, ”Design Guidelines of Circuit Parameters for Modular Multilevel Converter with H-bridge Cell,” IEEJ J. Industry Applications, vol.6, no.3, pp.231-244, (2017)

[13] H. Hwang, X. Liu, J. Kim and H. Li: “Distributed Digital Control of Modular-Based Solid-State Transformer Using DSP+FPGA,” IEEE Trans. On Industrial Electronics, Vol.60, No.2, pp.670-680, (2013)

[14] T. Nakanishi, and J. Itoh, “Capacitor Volume Evaluation based on Ripple Current in Modular Multilevel Converter,” 9th International Conference on Power Electronics, No. WeA1-5, (2015)

[15] J. Shi, W. Gou, H. Yuan, T. Zhao and A. Q. Huang: “Research on Voltage and Power Balance Control for Cascaded Modular Solid-State Transformer,” IEEE Trans. On Power Electronics, Vol. 26, No. 4, pp.1154-1166, (2011)

[16] T. Isobe, H. Tadano, Z. He, and Y. Zou: “Control of Solid-State-Transformer for Minimized Energy Storage Capacitors,” IEEE ECCE, pp.3809-3815, (2017)

[17] J. E. Huber, and J. W. Kolar: “Solid-State Transformer: On the Origins and Evolution of Key Concepts,” IEEE Industrial Electronics Magazine, Vol. 10, pp.19-28, (2016)

[18] T. Nussbaumer, K. Raggl, and J. W. Kolar: “Design Guidelines for Interleaved Single-Phase Boost PFC Circuits,” IEEE Trans. On Industrial Electronics, Vol. 56, No. 7, pp.2559-2573, (2009)

[19] Y. Hayashi, Y. Matsugaki, and T. Ninomiya, ”Capacitively Isolated Multicell Dc-Dc Transformer for Future Dc Distribution System,” IEEJ J. Industry Applications, vol. 6, no. 4, pp. 268–277, (2017)

[20] M. Sato, R. Takiguchi, J. Imaoka, and M. Shoyama: “A Novel Secondary PWM Controlled interleaved LLC Resonant Converter for Load Current Sharing,” IPEMC 2016, pp.2276-2280, (2016)

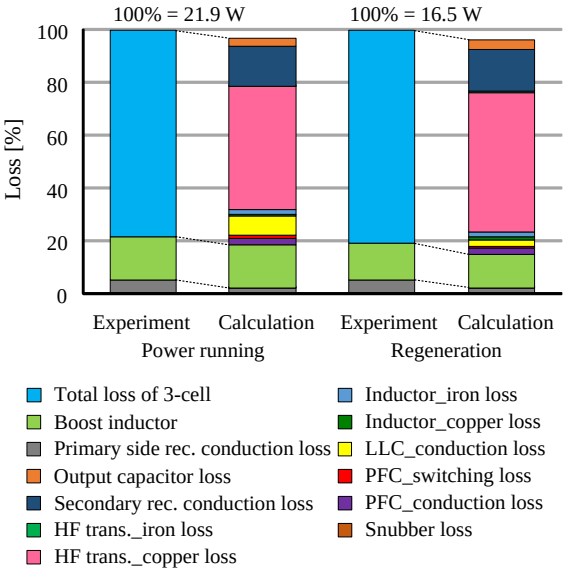


Fig. 12. Loss distribution result by experiment and calculation at bidirectional operation. (Explanatory note corresponds to each color of graph.)

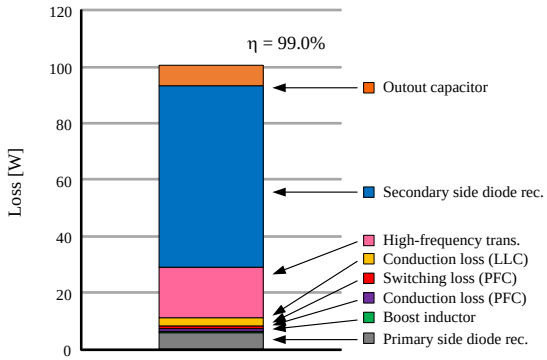


Fig. 13. Loss distribution of 6.6 kV/ 10 kW full model SST by calculation.

[21] J. Itoh, T. Sakuraba, H. N. Le, K. Kusaka: “Requirements for Circuit Components of Single-Phase Inverter Applied with Power Decoupling Capability toward High Power Density,” 18th European Conference on Power Electronics and Applications (EPE'16), DS2a 0291, (2016)

[22] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe: “Improved Core-Loss Calculation for Magnetic Components Employed in Power Electronic Systems,” IEEE Trans. On Power Electronics, Vol. 27, No. 2, pp.964-973, (2012)