Open-loop-based Island-mode Voltage Control Method for Single-phase Grid-tied Inverter with Minimized LC Filter

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***Abstract*— This paper proposes an island-mode voltage control method by using an open-loop control applying a high-gain disturbance observer (DOB) for a single-phase inverter with a low capacitance output filter. The output voltage is distorted with the low capacitance by the conventional method which consists of a PID regulator for an automatic voltage regulator (AVR) and a PI regulator for an automatic current regulator (ACR). In order to compensate the output voltage distortion, the high-gain DOB for the output voltage is applied in the open-loop-based voltage control. DOB is implemented into a field-programmable gate array (FPGA) with high-speed sampling. In the LC filter of a 1-kW prototype, the impedance of the inductor is minimized to 1.0% of the normalized inverter impedance, whereas the admittance of the capacitor is reduced to 0.25% of the normalized inverter admittance. By the proposed method, the inverter output voltage total harmonic distortion (THD) is reduced by 82.4% even with the diode rectifier load compared to the conventional voltage control, whereas the constant output voltage is achieved regardless of any conditions of load.**

Keywords*— *Grid-tied inverter, Island-mode, Minimized LC filter, Open-loop-based voltage control

I. INTRODUCTION

In recent years, grid-tied inverters, e.g. photovoltaic systems, fuel cell systems, and wind turbine systems, have been actively studied for energy saving [1]-[3]. The inverter is required to have a small volume in order to increase the power density of the system [4]-[5]. Generally, interconnected inductors occupy a majority of the inverter size. Therefore, the interconnected inductor is highly required to reduce the size. By reducing the inductance, it is possible to reduce the volume of the inductor. A high switching frequency with SiC or GaN devices is applied in term of a same current ripple in order to reduce the inductance of the interconnected inductor. Moreover, the capacitance of the filter capacitor is possible to reduce due to a filter design of high cutoff frequency. Therefore, it is possible to apply the high resonance frequency output filter for the inverter by increasing the switching frequency. On the other hand, the inverter output current overshoot rate becomes high during the voltage sag when the inductance of the interconnected inductor is reduced. Thus, the authors propose the high-speed gate-block method and the design method of LC or LCL filter in order to meet the fault-ride-through (FRT) requirements [6]-[7]. In particular, in order to meet the FRT requirements, a filter capacitor with low capacitance is desirably designed to reduce the resonance.

Meanwhile, when a black out in a long period that is exceeding the FRT requirements occurs, the grid-tied inverter is required to perform the island mode operation in order to supply the power to the load [8]-[10]. In order to output the voltage, it is necessary to implement the voltage controller for the inverter. However, the disturbance suppression performance of the voltage controller worsens due to the low capacitance of the filter capacitor in the minimized LC filter. The inverter output voltage is distorted when the island mode operation with the low disturbance suppression performance is connected to nonlinear-load such as a rectifier load. As one of the solution for this problem, the control response of the voltage controller and the current controller are increased in order to enhance the disturbance suppression performance. However, the increase in the control response is limited to the detection delay time and the sampling frequency. Moreover, in order to improve the output voltage distortion, the voltage control methods applied in such as Uninterruptible Power Supply (UPS) systems are proposed in [11]-[12]. The operation of UPS is not necessary to consider the FRT operation. Thus, the filter capacitor of the output filter is possible to increase the capacitance. The voltage control methods of [11]-[12] are not considered with the output filter of the low capacitance. Therefore, in the grid-tied inverter, the voltage control with the low capacitance has to be considered. Moreover, it is necessary to implement a complex control or sampling method for the control methods of [11]-[12].

This paper proposes new open-loop-based island-mode voltage control method equipped with a high-gain disturbance suppression in order to achieve a low total

harmonic distortion (THD) of the output voltage. The originality in this paper is that the island-mode voltage control with the minimized LC filter is possible to compensate an output error voltage for the load current without a current feedback loop. Moreover, it is not necessary to consider the interference between the voltage controller and the current controller. This control is defined as the VOLTAGE DISTURBANCE COMPENSATION OPEN-LOOP CONTROL (VDCOLC) in this paper. The proposed VDCOLC compensates the load current disturbance by using the output voltage detection value to calculate the disturbance through a high-gain disturbance observer (DOB) [13]-[15]. In order to compensate the disturbance with the high-speed sampling, the high-gain DOB is implemented in field-programmable gate array (FPGA). By using this proposed VDCOLC, a reduction of THD for the inverter output voltage is confirmed with a 1-kW prototype.

II. Problem of Island-mode Voltage Control with Minimized LC Filter

Figure 1 shows a circuit configuration of a single-phase grid-tied inverter with an LC filter. In this paper, an H-bridge single-phase two-level inverter is employed due to its simplicity. In order to reduce the volume, the LC filter is minimized. In the island mode operation, the output voltage is controlled by configuring the voltage controller with the filter capacitor of the output LC filter as the control object. The disturbance gain of the output current i_{out} $G_D(s)$ when the voltage controller is constructed by PI controller is expressed as

$$G_D(s) = \frac{s}{s^2 C_f + sK_p + \frac{K_p}{T_i}} \quad (1),$$

where C_f is the capacitance of the filter capacitor, K_p is the proportional gain, T_i is the integral time, s is the Laplace operator, and the current control gain is one. The disturbance suppression performance worsens due to the increase of the disturbance gain, when the capacitance of the filter capacitor C_f is decreased in (1). Thus, it is necessary to improve the disturbance suppression performance, in order to achieve the island mode operation with the minimized LC filter.

III. Open-loop-based Voltage Control for Island Mode Operation

A. Current Detection Problem of Filter Capacitor

Figure 2 shows a conventional closed-loop-based island-mode voltage control with current controller composed by PI regulator. In general, an island-mode voltage control is carried out by a voltage controller that has inner loop of the current controller. Note that, the disturbance suppression performance is improved by using the filter capacitor current control [16]. The disturbance for the voltage controller such as the load current is included in the filter capacitor current. Thus, the disturbance compensation for the output voltage controller is not

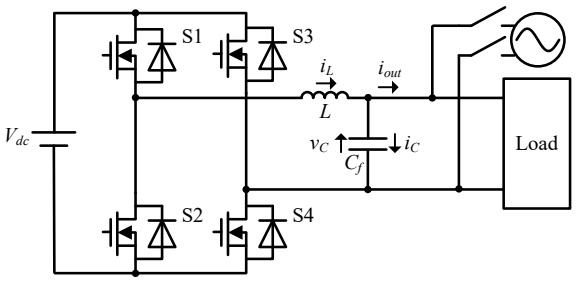


Fig. 1. Circuit diagram for island mode. In this paper, the output LC filter is minimized.

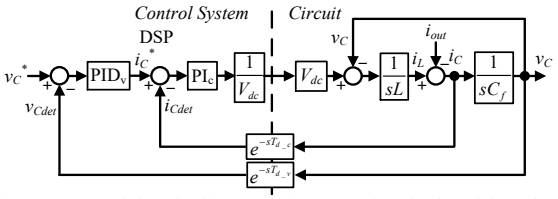


Fig. 2. Control block diagram of conventional closed-loop-based voltage control for island mode operation. In order to improve the disturbance suppression performance, the control response has to be increased.

necessary by the filter capacitor current feedback control. Moreover, it is necessary to increase the control response, which is limited due to the controller hardware, in order to achieve the island mode with the minimized LC filter.

Figure 3 shows the filter capacitor current detection value under the same output voltage with different detection delay time of the filter capacitor current, where the impedance of the interconnected inductor is 1.0% of the normalized inverter impedance, the admittance of the filter capacitor is 0.25% of the normalized inverter admittance in the 1-kW system. The detection of the filter capacitor average current for one switching period is required as shown in Fig. 2. However, the filter capacitor current has a large current ripple when the low capacitance of the filter capacitor is applied. Because the switching frequency becomes higher than the fundamental frequency component of the output current. Thus, it is impossible to detect the filter capacitor average current per the switching period due to the current detection delay time. In Fig. 3 (a) and (b), it is possible to detect the average filter capacitor current as a sinusoidal wave, when the detection delay time is 0 s or half period of carrier (6.25 μs). However, the detection point of the output current is different from the average value, i.e. the filter capacitor current detection value becomes non-sinusoidal wave, when the detection delay time of the filter capacitor current becomes longer as shown in Fig. 3 (c) as 10 μs. Thus, it is impossible to detect the filter capacitor average current due to the above problem. As a result, the inverter output voltage THD becomes worse. It is necessary to apply the multi-rate sampling for the average capacitor current detection [11]-[12], in order to solve above problem.

B. Proposed Open-loop-based Island-mode Voltage Control

The resonance frequency of the filter is shifted to the high frequency range when the LC filter is minimized.

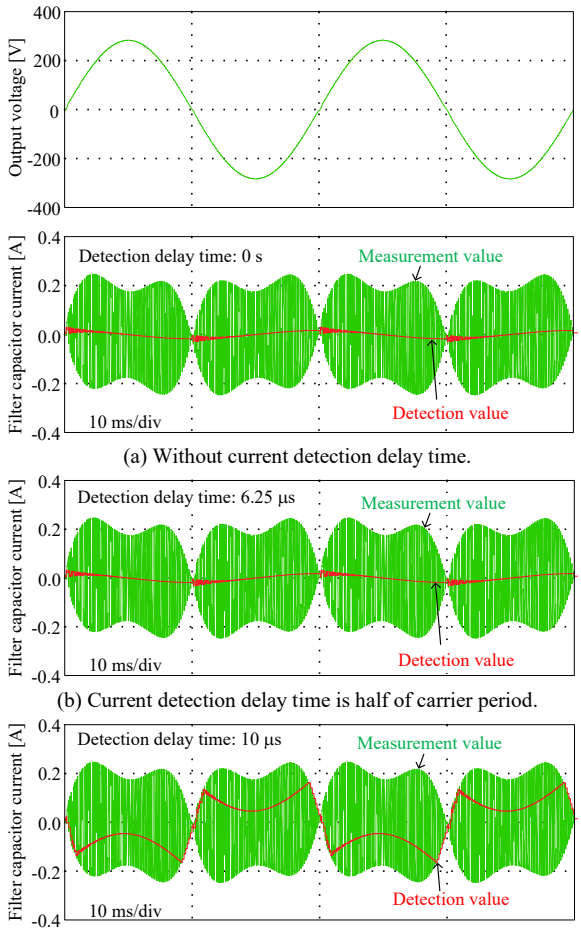


Fig. 3. Comparison of filter capacitor current detection with different current detection delay time.

The transfer function for the output voltage command with the open-loop operation $G_{com\_OL}(s)$ is expressed as

$$G_{com\_OL}(s) = \frac{1}{s^2 LC_f + 1} \quad (2).$$

The transfer function becomes wide bandwidth for the output voltage command v_c^* with the minimized LC filter by (2). Therefore, an open-loop-based voltage control can be employed without the occurrence of the output voltage resonance. Nevertheless, the output voltage with the open-loop-based voltage control varies highly dependently on the load, because the output voltage is not feedback and is not regulated by the voltage controller. Furthermore, odd number harmonic components occur in the output voltage due to the nonlinear output current, when a diode rectifier load is connected to the inverter. Therefore, it is necessary to compensate the disturbance of the output current in order to obtain the stable and constant output voltage regardless of the load.

Figure 4 shows the conventional open-loop-based island-mode voltage control with the typical dead-time compensation. The output voltage error due to the dead-time error voltage is compensated by using this method. However, the harmonic components due to the nonlinear-load such as the diode rectifier cannot be compensated.

Figure 5 shows the proposed VDCOLC. In order to achieve the high-gain compensation, the compensator is

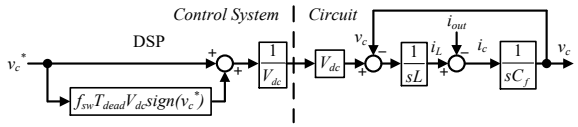


Fig. 4. Control block diagram of conventional open-loop-based island-mode voltage control for island mode operation.

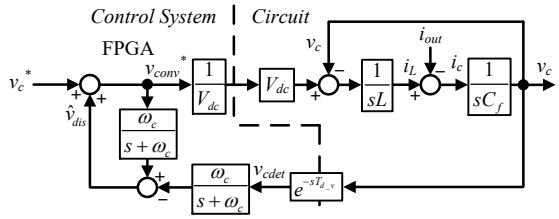


Fig. 5. Control block diagram of proposed VDCOLC for island mode operation. In order to compensate output voltage in the high-gain, the DOB is implemented in FPGA.

implemented by FPGA. Moreover, the compensator is operated as a DOB that compensates the disturbance due to the output current i_{out}. The disturbance estimation value $\hat{v}_{dis}$ is expressed by

$$\hat{v}_{dis} = \frac{\omega_c}{s+\omega_c} v_{conv}^* - \frac{\omega_c}{s+\omega_c} v_{cdet} \quad (3),$$

where ω_c is the cutoff angular frequency of the DOB, v_{conv}^* is the voltage command after the disturbance compensation, and v_{cdet} is the detection value of the filter capacitor voltage.

C. *Appling Area of Open-loop-based Voltage Control for Island Mode*

In the disturbance compensator of (3), the Low-pass-filter (LPF) is implemented into DOB in order to suppress the resonance components of the LC filter for the voltage command in the voltage controller. The resonance frequency of the LC filter f_{res_LC} is expressed as

$$f_{res\_LC} = \frac{1}{2\pi\sqrt{LC_f}} \quad (4).$$

In order to reduce the resonance component of the LC filter by using LPF, the cutoff frequency of LPF is designed to less than 1/10 to 1/2 for the resonance frequency of the LC filter f_{res_LC}. Thus, it is possible to reduce the effect of the LC filter resonance. However, in order to increase the performance of the disturbance compensator, it is necessary to increase the cutoff frequency of LPF. Due to the output current disturbance caused by the diode rectifier load, the odd-order harmonic components are included in the inverter output voltage. For instance, 11th order harmonic wave is 550 Hz; where fundamental wave is 50 Hz, when considering the reduction of the harmonics to 11th order for the fundamental wave of the output voltage. Thus, it is necessary to increase the LPF cutoff frequency of DOB higher than 550 Hz. Therefore, in order to consider the suppression of the harmonics to k order, the proposed method is applied as follows condition

$$kf_{out} < f_c < \frac{f_{res\_LC}}{n}, \left(n: 2 \sim 10, f_c = \frac{\omega_c}{2\pi} \right) \quad (5),$$

where f_{out} is the frequency of the output voltage, n is the ratio for the resonance frequency of the LC filter f_{res_LC}, which implies the DOB cutoff frequency from 1/10 to 1/2 of the resonance frequency of the LC filter. In this paper, the resonance frequency of the LC filter is approximately 10 kHz, where L is 1.29 mH (%Z = 1.0%), and C_f is 0.2 μF (%Y = 0.25%); therefore, if k is eleven, it is possible to meet (5). Furthermore, in order to compensate 11th order harmonic without interfering with the resonance frequency of the LC filter, the DOB cutoff frequency is set to 2 kHz.

Figure 6 shows the comparison of the disturbance gain characteristics of the conventional closed-loop-based voltage control and the proposed VDCOLC. The controller of the conventional method is similarly constructed as Fig. 2, where the angular frequency of the voltage controller is 3000 rad/s, and the angular frequency of the current controller is 30000 rad/s. Moreover, the disturbance suppression gain is calculated from the transfer function, where the output current i_{out} is the input, and the output voltage v_c is the output. Furthermore, the disturbance suppression performance is analyzed by sweeping the frequency of the disturbance suppression gain from 1 Hz to 100 kHz as Fig. 6. In Fig. 6, the disturbance gain is reduced with the proposed control from 30 Hz to 1 kHz of the disturbance frequency, which includes the harmonic components from first to 20th for the fundamental frequency of the output voltage. Thus, it is possible to reduce the output voltage distortion by using the proposed method.

IV. Simulation Result for Proposed VDCOLC

Table I shows the simulation conditions for the proposed method. The LC filter parameter and the DOB cutoff frequency are changed in the simulation results. Figure 7 shows the simulation results of the proposed method with the diode rectifier load. In Fig. 7 (a), it is possible to suppress the inverter output voltage THD less than 5.0%, when the resonance frequency of the LC filter is 10 kHz (L = 1.29 mH; %Z = 1.0%, C_f = 0.2 μF; %Y = 0.25%), and the DOB cutoff frequency is 2 kHz. The LC filter parameter is designed in order to suppress the output current overshoot with the low inductance during the voltage sag [7]. In order to reduce the resonance of the output current at the voltage fluctuation, the capacitance of the filter capacitor is designed to small. The inverter output voltage THD is 1.56%. Moreover, the design of the DOB cutoff frequency lower than the resonance frequency of the LC filter is possible to reduce the resonance component in the inverter output voltage. Thus, the resonance component of the inverter output voltage in Fig. 7 (a) does not occur, i.e. the condition of Fig. 7 (a) meets (5). In Fig. 7 (b), the resonance frequency of the LC filter and the DOB cutoff frequency are 2 kHz. The inverter output voltage is higher than 5%; in addition, the resonance occurs in the inverter output voltage. This is because the condition of Fig. 7 (b) does not meet (5), i.e. the LC filter resonance component is

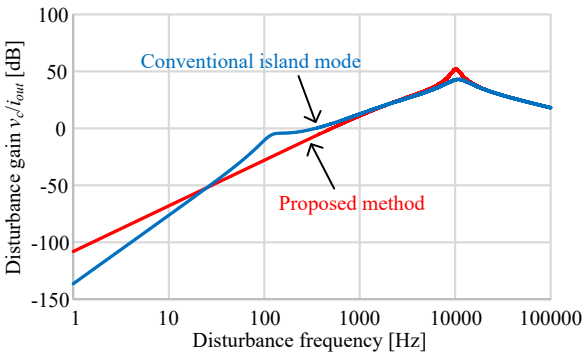


Fig. 6. Characteristics of disturbance gain from output current i_{out} to output voltage v_c. The resonance due to the controller is effected to the output voltage distortion with the conventional method.

TABLE I. SIMULATION CONDITIONS.

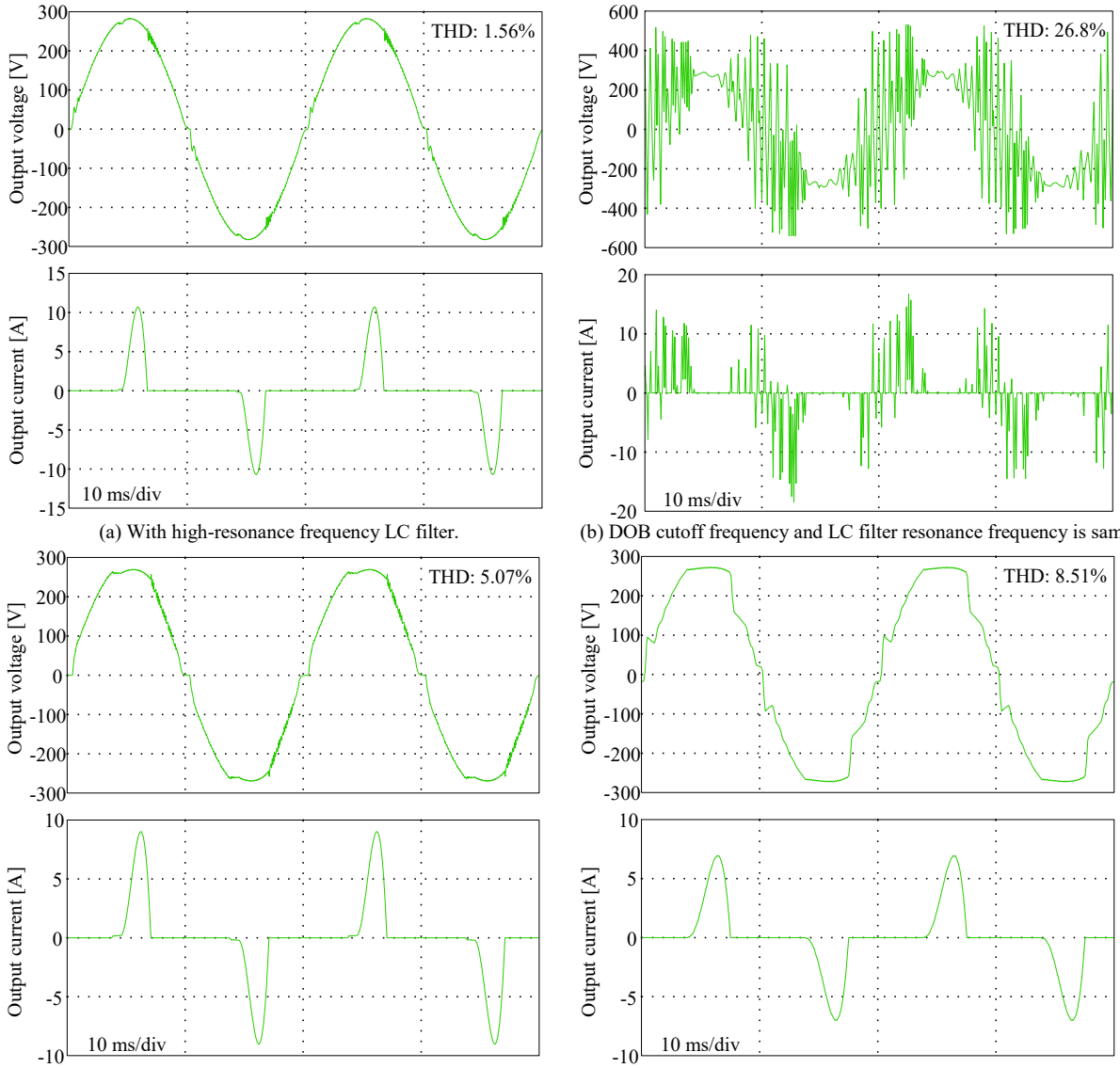
Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	80 kHz
DC link vol.	V_{dc}	380 V	Samp. fre. of DOB	f_{so}	80 kHz
Output volt. command	v_c^*	200 V_{rms}	Crest factor of load		3.0

included in the voltage command. In Fig. 7 (c), the resonance frequency of the LC filter is 10 kHz, and the DOB cutoff frequency is 200 Hz. The inverter output voltage THD is higher than 5.0% in this condition. This is because that the disturbance suppression performance of the DOB decreases due to the low DOB cutoff frequency. Thus, the inverter output voltage THD is worse due to the disturbance for the diode rectifier load. In addition, the dead-time error voltage compensation by DOB becomes not effective enough due to the low DOB cutoff frequency. In Fig. 7 (d), the resonance frequency of the LC filter is 2 kHz, and the DOB cutoff frequency is 200 Hz. The inverter output voltage THD is also higher than 5.0% in this condition. The inverter output voltage includes the distortion due to the low resonance frequency of the LC filter. Furthermore, the disturbance compensation value becomes not effective enough for the diode rectifier load due to the low DOB cutoff frequency. Thus, the inverter output voltage THD in Fig. 7 (d) is higher than the condition of Fig. 7 (c). In conclusion, the proposed method can only be applied in the area of (5).

V. Experimental Results

In the experimental verification of the island mode operation, three cases of load test are considered. The load conditions are as follows: (A) No-load, (B) Linear load such as resistance load, (C) Nonlinear-load such as diode rectifier load.

Table II shows the experimental conditions. By considering the frequency of the voltage command as 50 Hz, the angular frequency of the voltage controller for the conventional closed-loop-based island-mode voltage control is designed to ten times of the voltage command frequency. Thus, the angular frequency is set to 3000 rad/s. Moreover, in order to prevent the interference, the angular frequency of the current controller is designed to ten times for the angular frequency of the voltage controller. Thus, the angular frequency of the current



(a) With high-resonance frequency LC filter.

(b) DOB cutoff frequency and LC filter resonance frequency is same.

(c) With high-resonance frequency LC filter and low-DOB cutoff frequency.

(d) DOB cutoff frequency and LC filter resonance frequency is low.

Fig. 7. Simulation results for any condition of resonance frequency of LC filter and DOB cutoff frequency with the proposed VDCOLC. The inverter output voltage THD is suppressed to less than 5% when (5) is met.

controller is set to 30000 rad/s. Note that the minimized LC filter parameter is designed in order that the FRT requirements are met during the voltage sag [7]. The island mode operations are compared with the conventional closed-loop-based voltage control, the conventional open-loop-based island mode with the dead-time error compensation, and the proposed VDCOLC.

A. No-load Operation

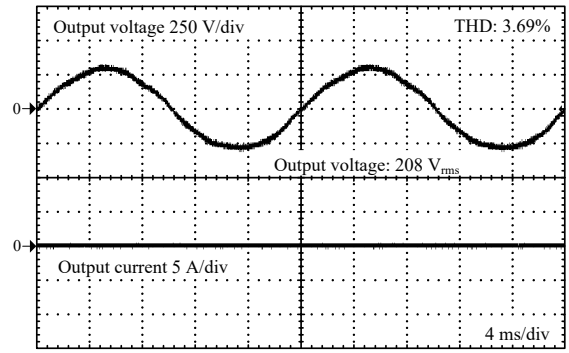
Figure 8 shows the experimental result for the no-load operation. In Fig. 8 (a), (b) and (c), the output voltage THD of three methods are suppressed to less than 5.0%. However, the inverter output voltage THD in Fig. 7 (a) is high in the conventional closed-loop-based voltage control. This is because the filter capacitor current detection has the delay time that is different from the half period of the carrier as shown in Fig. 3 (c). Thus, it is impossible to detect the average value for the filter capacitor current. Therefore, the inverter output voltage is distorted in Fig. 8 (a). In particular, the distortion of the inverter output voltage with the proposed method is reduced by 70.2% compared with the conventional closed-loop-based voltage control. In addition, the output voltage in Fig. 8 (a) is higher than the voltage command due to the high gain of the current controller. In order to regulate the output voltage in Fig. 8 (a), it is necessary to reduce the gain of the current controller. Moreover, the output voltage in Fig. 8 (b) is also higher than the voltage command due to the typical dead-time compensation. The dead-time error voltage does not occur in the no-load operation. Thus, the output voltage increases by the dead-time compensation value. On the other hand, the output voltage in Fig. 8 (c) is almost same compared with the voltage command.

B. Linear-load Operation

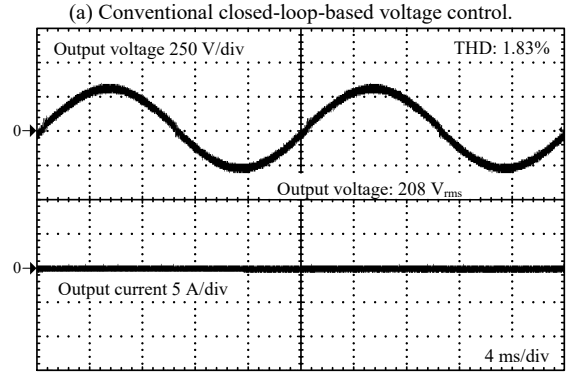
Figure 9 shows the experimental result for the linear load operation. In Fig. 9 (a), (b) and (c), the output voltage THD at the rated power with three methods are also suppressed to less than 5.0%. The inverter output

TABLE II. EXPERIMENTAL CONDITIONS.

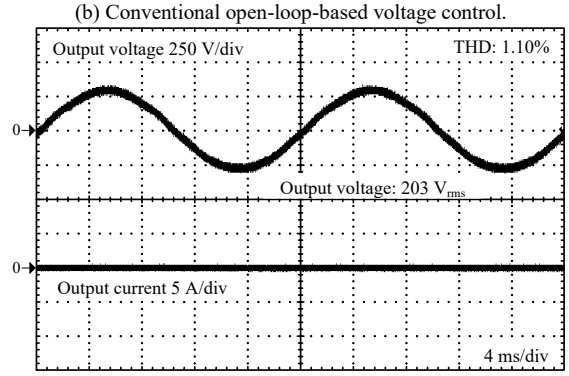
Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	80 kHz
DC link vol.	V_{dc}	380 V	Samp. fre. of DSP	f_s	20 kHz
Output volt. command	v_c^*	200 V_{rms}	Angl. fre. of AVR	ω_{avr}	3000 rad/s
Inter. Induc. (%Z)	L	1.29 mH (1.0%)	Angl. fre. of ACR	ω_{acr}	30000 rad/s
			Samp. fre. of DOB	f_{so}	80 kHz
Filter cap. (%Y)	C_f	0.2 μF (0.25%)	Cutoff fre. of DOB	f_c	2 kHz



(a) Conventional closed-loop-based voltage control.



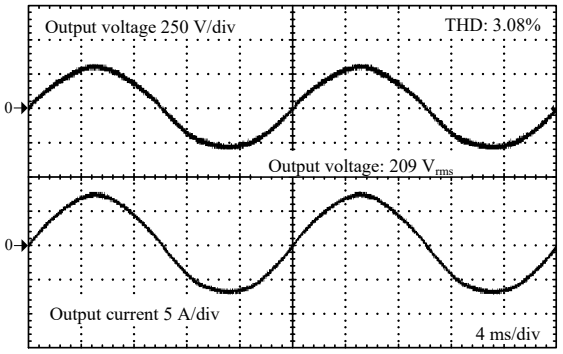
(b) Conventional open-loop-based voltage control.



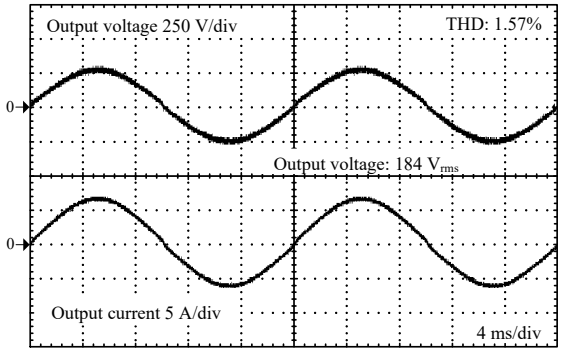
(c) Proposed VDCOLC.

Fig. 8. Experimental result for no-load operation. The output voltage THD is suppressed less than 5.0% in both the conventional method and the proposed method.

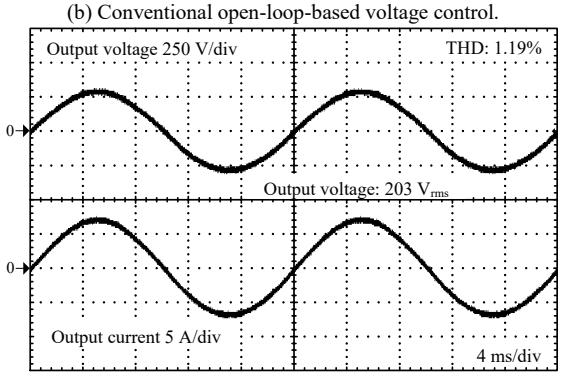
voltage THD in Fig. 9 (a) is high compared with both method of Fig. 9 (b) and (c), due to the same reason in Fig. 8 (a). In particular, the inverter output voltage THD with the proposed method is improved by 61.4% compared with the conventional closed-loop-based voltage control at the rated load. In addition, the output voltage in Fig. 9 (a) is higher than the voltage command due to the same reason in Fig. 8 (a). Moreover, the output voltage in Fig. 9 (b) decreases due to the load current compared with Fig. 8 (b). On the other hand, the output voltage in Fig. 9 (c) is almost same compared with the voltage command.



(a) Conventional closed-loop-based voltage control.



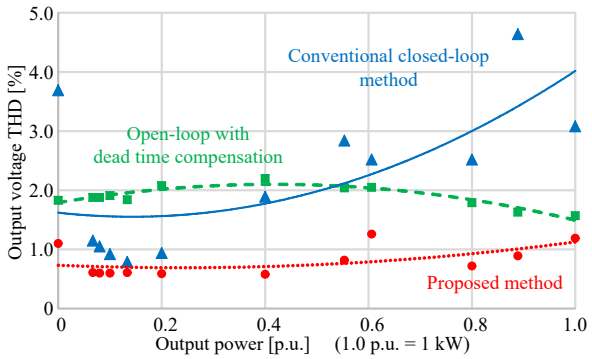
(b) Conventional open-loop-based voltage control.



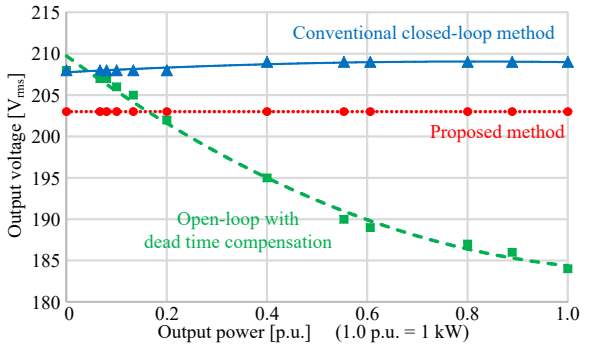
(b) Proposed VDCOLC.

Fig. 9. Experimental result for linear load operation at rated load. The output voltage THD is suppressed to less than 5.0% in both the conventional method and the proposed method.

Figure 10 shows the output voltage THD characteristic and the output voltage variation against the linear load. In Fig. 10 (a), the output voltage THD with the proposed method is reduced more effectively than with the conventional closed-loop-based voltage control. The maximum improvement of the output voltage THD is 80.8% at load of 0.9p.u.. Moreover, the inverter output voltage THD characteristics with the conventional open-loop-based island mode or the proposed method are approximately constant compared with the conventional closed-loop-based voltage control in the load range from 0p.u. to 1.0p.u.. The cause of difference for the inverter output voltage THD with the conventional closed-loop-based voltage control is that the variation of the load current causes the error of the filter capacitor average current detection value. Due to the detection error of the filter capacitor average current, the inverter output voltage becomes non-sinusoidal wave. Thus, the operation of the conventional closed-loop-based voltage control becomes unstable. On the other hand, in Fig. 10 (b), the inverter



(a) Output voltage THD characteristic with linear load.



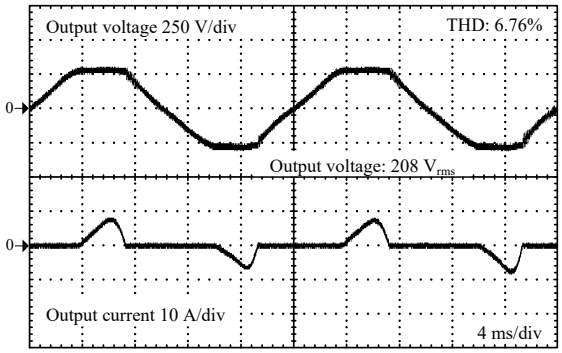
(b) Output voltage variation with linear load.

Fig. 10. Relationship between output voltage and resistive load in 1-kW system. By the proposed method, the output voltage THD is better than other two method. In addition, the output voltage is constant.

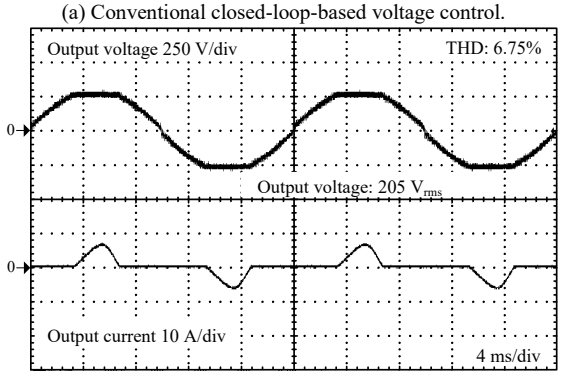
output voltage with the conventional closed-loop-based voltage control is almost constant in the load range from 0p.u. to 1.0p.u.. This is because the voltage controller regulates the inverter output voltage. However, the output voltage with the conventional open-loop-based voltage control varies significantly depending on the load. This is because that the inverter output voltage decreases due to the decrease of the filter capacitor current by the load current. On the other hand, the output voltage with the proposed method is constant. In the proposed control, DOB uses the detection value of the output voltage in order to estimate the output current and then compensate for the disturbance of the output current. On other perspective, the output voltage is indirectly regulated by a feedback loop in DOB. Therefore, it is possible to achieve that the inverter outputs the constant voltage during the island mode with the linear load in the proposed method.

C. Nonlinear-load Operation

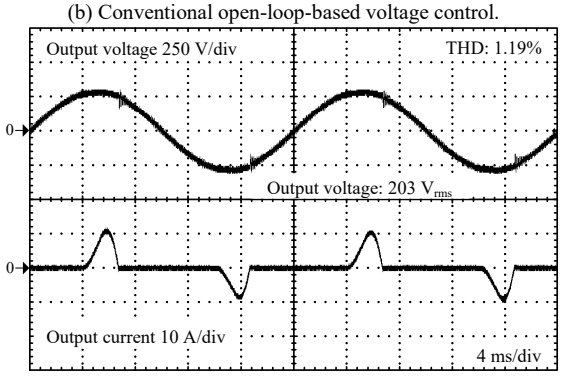
Figure 11 shows the experimental result for the nonlinear-load operation. The diode rectifier is applied as nonlinear load. The crest factor of the diode rectifier load is approximately 3.0. The output voltage THD is higher than 5.0%, when using the conventional closed-loop-based voltage control and the conventional open-loop-based island mode as in Fig. 11 (a) and (b). The inverter output voltage with the conventional closed-loop-based voltage control distorts due to the reduction of the disturbance suppression performance by the low capacitance of the filter capacitor and the error of the filter



(a) Conventional closed-loop-based voltage control.



(b) Conventional open-loop-based voltage control.



(c) Proposed VDCOLC.

Fig. 11. Experimental result for diode rectifier-load operation. By using the proposed method, the output voltage THD is reduced to 1.19% with the nonlinear-load.

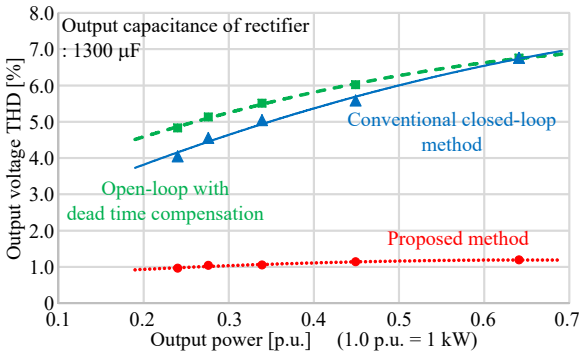
capacitor average current detection. In particular, the disturbance compensation is not effective enough for the output current control with the nonlinear load. Moreover, the inverter output voltage with the conventional open-loop-based island mode also distorts due to the non-sinusoidal output current which flows during the output voltage peak. On the other hand, by using the proposed method as in Fig. 11 (c), the output voltage THD is less than 5.0%. It is possible to compensate the drop voltage due to the open-loop-based operation with the high-gain DOB in the proposed method. Thus, the inverter output voltage becomes sinusoidal wave even with the diode rectifier load. Therefore, it is possible to suppress the output voltage THD by using the proposed method.

Figure 12 shows the THD characteristic and the output voltage variation against the nonlinear-load. In Fig. 12 (a), the output voltage THD with the proposed method is reduced more effectively than with the conventional closed-loop-based voltage control or the conventional open-loop-based voltage control. The maximum

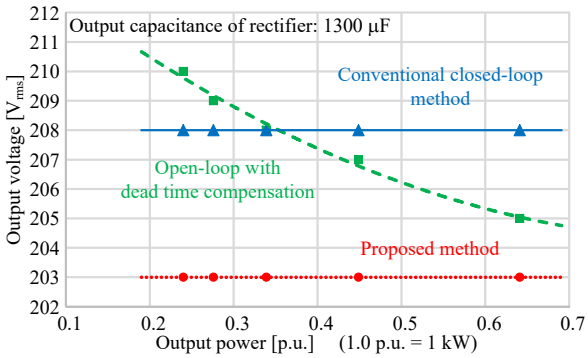
improvement of the output voltage THD with the proposed method is 82.4% compared with the conventional closed-loop-based voltage control at the heavy nonlinear load. Moreover, in Fig. 12 (b), the output voltage with the conventional open-loop-based island mode decreases greatly at the heavy nonlinear-load. On the other hand, the output voltage with the conventional closed-loop-based voltage control and the proposed method is constant value. Thus, it is possible to achieve that the inverter outputs the constant voltage during the island mode with the nonlinear-load in the proposed method. Therefore, it is confirmed that by using the proposed method, the output voltage is constant regardless of any conditions of load, i.e. linear/nonlinear load, or light/heavy load.

VI. Conclution

This paper proposed the open-loop-based island-mode voltage control with the high-gain disturbance compensation when the LC filter is minimized. Moreover, the applying area of the proposed method is clarified by the DOB cutoff frequency and the resonance frequency of the LC filter. By using the proposed method, the output voltage is constant in the island mode during regardless of any conditions of load. Furthermore, the output voltage THD with the proposed method is suppressed to less than 5.0%. In particular, the output voltage THD was improved by 82.4% compared with the conventional closed-loop-based voltage control when the nonlinear-load was connected. Therefore, the proposed method was confirmed to the utility for the island mode with the minimized LC filter.



(a) Output voltage THD characteristic with nonlinear-load.



(b) Output voltage variation with nonlinear-load.

Fig. 12. Relationship between output voltage and rectifier load in 1-kW system. By using the proposed method, the output voltage THD is suppressed to less than 50%. Moreover, the output voltage is constant.

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