Discontinuous Current Mode Control for Minimization of Three-phase Grid-Tied Inverter in Photovoltaic System

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***Abstract*— In this paper, a current control method of discontinuous current mode (DCM) is proposed for a three-phase grid-tied inverter in order to minimize inductors without worsening current total harmonic distortion (THD). In a conventional continuous current mode (CCM) control, current THD increases as an inductor value is reduced, because a zero-clamping phenomenon occurs due to dead-time. In the proposed DCM current control, a zero-current interval is intentionally controlled and a dead-time-induced error voltage is simply compensated with a conventional dead-time compensation. The validation of the control method is confirmed by simulation and a 700W-prototype. As simulation results, compared to the conventional CCM current control, the current THD is reduced by 97.6% with the proposed DCM current control, whereas the inductor volume is reduced by 70%. In the experiments, the current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u. even when the inductance impedance is reduced to 0.5% of the inverter total impedance.**

Keywords*— *three-phase grid-tied inverter, continuous current mode, discontinuous current mode

I. INTRODUCTION

In the last decade, researches on photovoltaic system (PV) have accelerated due to an increasing demand of renewable and sustainable energy sources [1]-[3]. In the PV system, H-bridge three-phase grid-tied inverters are generally employed as an interface between solar panels and three-phase grid. In such grid-tied inverters, a grid filter is required to connect between an output of the inverter and the grid in order to filter out the current harmonics and to meet grid current harmonic constraints as defined by standards such as IEEE-1547 [4]. Due to the observation that inductors in the grid filter occupy a major volume of the inverter, an inductor value of the grid filter is necessarily reduced in order to minimize the grid filter as well as the inverter. However, this reduction of the inductor value implies a design of a high switching current ripple due to a high dc-link voltage to inductance ratio. This high current ripple results in a current distortion phenomenon called zero-current clamping, where a current distortion increases notably as the switching current ripple increases [5]-[9].

Due to the zero-current clamping effect, the dead-time-induced error voltage exhibits a strong nonlinear behavior around zero-current crossing points. Hence, conventional dead-time compensation methods such as, e.g. two-level approximation compensation method (ACM) [10]-[11], linear ACM [12] and three-level ACM [13]-[15], cannot compensate for this nonlinear behavior of the dead-time-induced error voltage. Several compensation methods for the nonlinearity of the dead-time-induced error voltage such as adaptive dead-time compensation method and turn-off transition compensation method have been proposed to deal with this nonlinearity behavior and to reduce the zero-crossing current distortion [16]-[17]. Nevertheless, both methods exhibit the requirements which restrict the employment over a wide range of application. Adjustment mechanism parameters for the adaptive dead-time compensation must be properly tuned for each individual system [16]. Meanwhile, accurate device parameters, e.g. parasitic capacitances, are required for the turn-off transition compensation method [17].

In this paper, a current control for the three-phase grid-tied inverter operated in discontinuous current mode (DCM) is proposed in order to minimize the grid filter without worsening the current distortion. In order to deal with the zero-current clamping effect, the inverter is intentionally operated in DCM instead of a conventional continuous current mode (CCM). In other words, the zero-current interval with the DCM operation is controlled, enabling a proper compensation for the nonlinear behavior. Consequently, the conventional dead-time compensation method, i.e. two-level ACM, can be employed simply in order to compensate the dead-time-induced error voltage and reduce the current

distortion. The contribution of this paper is that the proposed DCM current control is implemented with the conventional dead-time compensation method to simply compensate the dead-time-induced error voltage. The effectiveness of the proposed current control is confirmed by simulations and experiments.

II. Discontinuous-Current-Mode Current Control

A. Zero-crossing distortion

Figure 1 depicts the H-bridge three-phase grid-tied inverter with a *LCL*-based grid filter. The minimization of the *LCL* filter generates a current with a high ripple in the inductors L. The filter stage with L_f and C_f can suppress the high-order current harmonics in order to meet grid current harmonic constraints as defined by standards such as IEEE-1547 [4].

Figure 2 describes the zero-crossing current distortion phenomenon. As the current ripple increases with the minimized *LCL* filter, the current distortion increases notably around the zero-crossing points due to the zero-current clamping effect, making the dead-time-induced error voltage become nonlinear. Therefore, the employment of the conventional two-level ACM just further increases the current distortion [17].

B. Discontinuous-current-mode operation

Figure 3 indicates the phase clamping selection in six cycles of traditional discontinuous pulse width modulation (DPWM), and the inverter output current waveform in one switching period during 0°-60° region. In order to simplify the control of DCM, only two phase currents should be controlled, whereas the current of the third phase is the summation of the currents of the first two phases. Hence, DPWM is employed in order to satisfy this control condition. During each 60-degree time region in DPWM, one phase is clamped to P or N polarity of dc-link voltage as shown in Fig. 3(a), whereas the other two phases are modulated to control separately two inverter output currents as shown in Fig. 3(b). Note that D_1 and D_2 indicate the duty ratios of the first and the second intervals of the first controlled current, D_3 and D_4 indicate the duty ratios of the first and the second intervals of the second controlled current, whereas D_5 depicts the duty ratio of the zero-current intervals. The duty ratios in Figure 3 are calculated as follows.

The inductor voltage of the inverter-side inductor L during a switching period T_{sw} is given by (1),

$$L\frac{di_{avg\_u}}{dt} = D_1\left(V_{dc} - v_{uo} + v_{vo}\right) + D_2\left(-v_{uo} + v_{vo}\right) \quad \ldots (1)$$

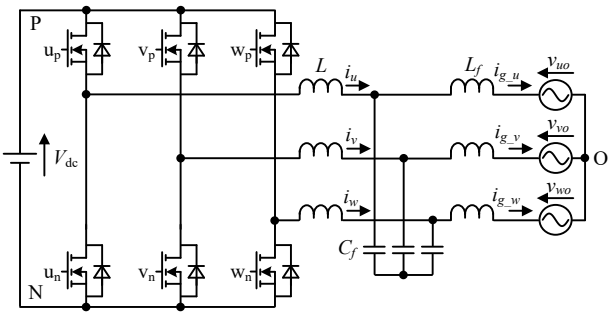
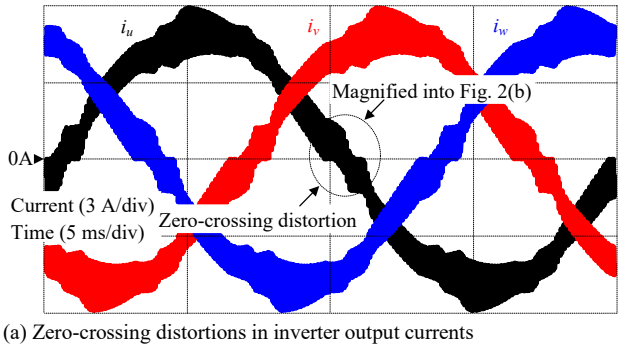
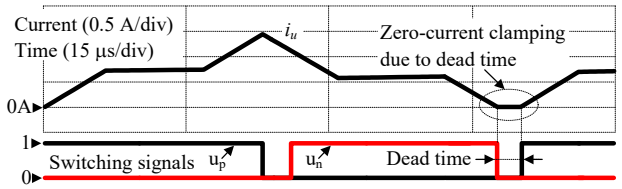


Fig. 1. H-bridge grid-tied three-phase inverter. This topology is employed due to its simple control and construction.

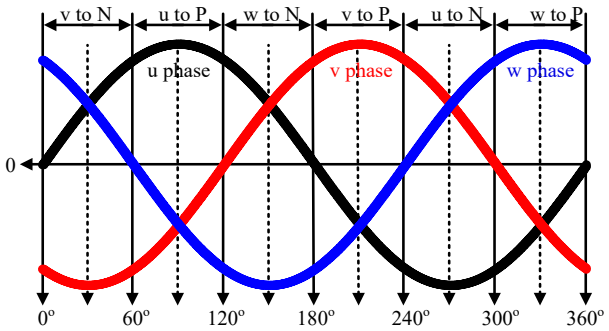


(a) Zero-crossing distortions in inverter output currents

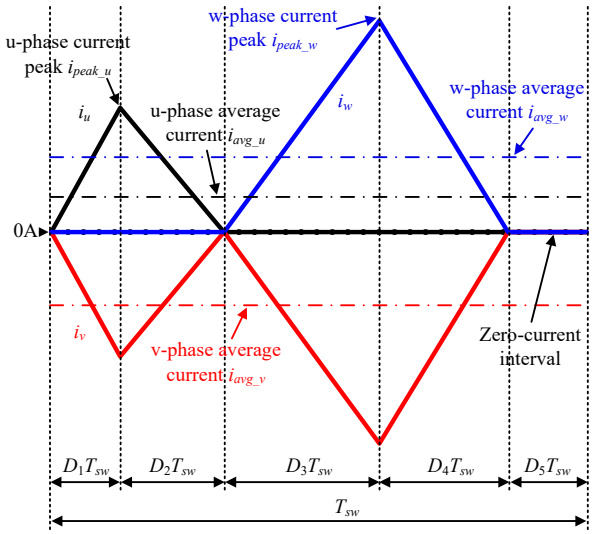


(b) Zero-current clamping effect due to dead-time

Fig. 2. Zero-current distortion phenomenon. The current distortion increases with the high current ripple due to the dead-time.



(a) Phase clamping selection in six cycles of DPWM



(b) Inverter output current waveform in one switching period during 0°-60° region

Fig. 3. Six 60-degree time regions of DPWM and inverter output current in DCM. In order to simplifying the DCM control, DPWM is employed, controlling only two phase currents at the same time.

where V_{dc} is the dc-link voltage, v_{uo} and v_{vo} are the grid phase voltages. The average current i_{avg_u} and the current peak i_{peak_u} shown in Figure 3 is expressed as,

$$i_{avg\_u} = \frac{i_{peak\_u}}{2}(D_1 + D_2) \quad \text{.....(2)}$$

$$i_{peak\_u} = \frac{V_{dc} - (v_{uo} - v_{vo})}{2L} D_1 T_{sw} \quad \text{.....(3)}$$

Substituting (3) into (2), and solving the equation for the duty ratios D_2, then the duty ratio D_2 is expressed by (4),

$$D_2 = \frac{4Li_{avg\_u}}{D_1 T_{sw}(V_{dc} - v_{uo} + v_{vo})} - D_1 \quad \text{.....(4)}$$

Substituting (4) into (1) in order to remove the duty ratio D_2 and representing (1) as a function of only the duty ratio D_1, (5) is obtained [18].

$$L\frac{di_{avg\_u}}{dt} = D_1 V_{dc} - \frac{4Li_{avg\_u}(v_{uo} - v_{vo})}{D_1 T_{sw}(V_{dc} - v_{uo} + v_{vo})} \quad \text{.....(5)}$$

Substituting the differential of the inductor current di_{avg_u}/dt in (5) as zero and the duty ratio D_1 is expressed as in (6),

$$D_1 = 2\sqrt{\frac{i_{avg\_u} L f_{sw}(v_{uo} - v_{vo})}{V_{dc}(V_{dc} - v_{uo} + v_{vo})}} \quad \text{.....(6)}$$

where f_{sw} is the switching frequency. Then, substituting the differential of the inductor current di_{avg_u}/dt in (1) as zero and the duty ratio D_2 is expressed as in (7),

$$D_2 = \frac{D_1(V_{dc} - v_{uo} + v_{vo})}{v_{uo} - v_{vo}} \quad \text{.....(7)}$$

Similarly, the duty ratios D_3 and D_4 shown in Figure 3 can be expressed as in (8)-(9),

$$D_3 = 2\sqrt{\frac{i_{avg\_w} L f_{sw}(v_{wo} - v_{vo})}{V_{dc}(V_{dc} - v_{wo} + v_{vo})}} \quad \text{.....(8)}$$

$$D_4 = \frac{D_3(V_{dc} - v_{wo} + v_{vo})}{v_{wo} - v_{vo}} \quad \text{.....(9)}$$

Figure 4 shows the control system of the three-phase grid-tied inverter operating completely in DCM, whereas Table I depicts the values for the duty calculation and the switching signal output in each 60-degree time region. When the grid operates normally, the inverter only has to regulate the grid current following the sinusoidal waveform. First, the 60-degree time region is detected by detected values of the grid phase voltage v_{uo}, v_{vo}, and v_{wo}. Then, the phase current references and the phase voltages are distributed to input values of a duty calculation based on the detected 60-degree time region as shown in Table I. In the duty calculation step, the duty ratios D_1-D_5 are expressed as follows. Note that the calculation of the duty ratios D_1-D_5 is similar to that of the duty ratios D_1-D_4 shown in Figure 3.

$$D_1 = 2\sqrt{\left|\frac{i_{1\_ref} L f_{sw}(v_1 - v_2)}{V_{dc}(V_{dc} - v_1 + v_2)}\right|} \quad \text{.....(10)}$$

$$D_2 = \frac{D_1(V_{dc} - v_1 + v_2)}{v_1 - v_2} \quad \text{.....(11)}$$

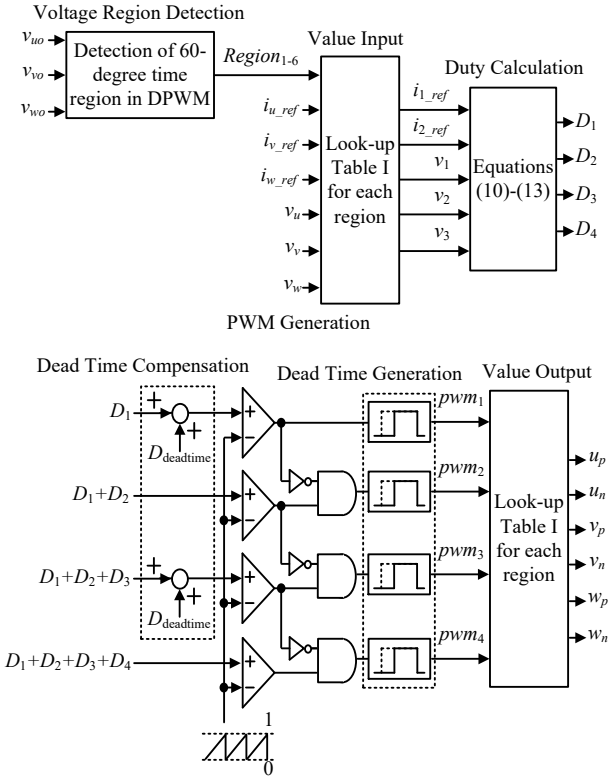


Fig. 4. Control system of the three-phase grid-tied inverter operating completely in DCM. The dead-time-induced error voltage is compensated simply when the inverter is intentionally operated in DCM because the zero-current interval is controlled.

TABLE I
LOOK-UP VALUES FOR DUTY CALCULATION AND PWN OUTPUT.

Region / Variable	0°-60°	60°-120°	120°-180°	180°-240°	240°-300°	300°-360°
i_{1_ref}	i_{u_ref}	i_{w_ref}	i_{v_ref}	i_{u_ref}	i_{w_ref}	i_{v_ref}
i_{2_ref}	i_{w_ref}	i_{v_ref}	i_{u_ref}	i_{w_ref}	i_{v_ref}	i_{u_ref}
v_1	v_u	$-v_w$	v_v	$-v_u$	v_w	$-v_v$
v_2	v_v	$-v_u$	v_w	$-v_v$	v_u	$-v_w$
v_3	v_w	$-v_v$	v_u	$-v_w$	v_v	$-v_u$
u_p	pwm_1	1	pwm_3	pwm_2	0	pwm_4
u_n	pwm_2	0	pwm_4	pwm_1	1	pwm_3
v_p	0	pwm_4	pwm_1	1	pwm_3	pwm_2
v_n	1	pwm_3	pwm_2	0	pwm_4	pwm_1
w_p	pwm_3	pwm_2	0	pwm_4	pwm_1	1
w_n	pwm_4	pwm_1	1	pwm_3	pwm_2	0

$$D_3 = 2\sqrt{\left|\frac{i_{2\_ref} L f_{sw}(v_3 - v_2)}{V_{dc}(V_{dc} - v_3 + v_2)}\right|} \quad \text{.....(12)}$$

$$D_4 = \frac{D_4(V_{dc} - v_3 + v_2)}{v_3 - v_2} \quad \text{.....(13)}$$

$$D_5 = 1 - D_1 - D_2 - D_3 - D_4 \quad \text{.....(14)}$$

where i_{1_ref} and i_{2_ref} are the first and second controlled currents in each 60-degree time region, and v_1, v_2 and v_3 are the voltages corresponding to the controlled currents.

For instance, during the 0°-60° time region, the controlled currents are i_u and i_w as shown in Fig. 3. Therefore, the input values to i_1, i_2, v_1, v_2, and v_3 are i_{u_ref}, i_{w_ref}, v_{uo}, v_{vo} and v_{wo}, respectively, as shown in Table I.

Next, the dead-time compensation is introduced at the first step of PWM generation. The duty ratio which compensates for the dead-time-induced error voltage, is expressed as follow,

$$D_{deadtime} = f_{sw} T_{deadtime} \quad \text{.....(15)}$$

where $T_{deadtime}$ is the dead-time. The dead-time-induced error voltage is simply compensated as shown in Fig. 4 because when the inverter is intentionally operated in DCM, the zero-current interval is under control. The compensated duty ratios are then compared with the sawtooth waveform to generate the PWM signals. In order to avoid the simultaneous turn-on of both switching devices in one leg, the typical dead-time generation is used to delay the turn on. Finally, the PWM signals are distributed to the switching devices corresponding to each 60-degree time region of DPWM based on Table I. Note that if the outputs pwm_2 and pwm_4 are utilized as shown in Table I, the inverter is operated under synchronous switching; otherwise, if the outputs pwm_2 and pwm_4 are set to zero, the inverter is operated under asynchronous switching.

III. Simulation Results

Table II shows the circuit parameters to evaluate the operation of the inverters, whereas Figure 5 depicts the inductor volume against the inductor impedance. The inverter-side inductors L in Fig. 1 occupy a majority of the inverter volume. Therefore, the minimization of L is mainly focused in this paper. Generally, the inductor value is expressed as a grid filter impedance scaled to the inverter total impedance $\%Z_L$ [21]. In particular, three designs of the grid filter impedance are evaluated. As shown in Fig. 5, the inverter-side inductor L volume is minimized by 70% when the inductor impedance $\%Z_L$ is reduced from 2.5% to 0.075%.

Figure 6 shows the inverter output currents and the average currents of the conventional CCM current control and the proposed DCM current control at rated load with three inductor designs from Fig. 5. As the current ripple increases, i.e. the decrease in the inductor impedance, the current with the conventional CCM current control distorts notably around the zero-crossing points. Consequently, the current THD increases from 1.5% to 9.8% when the inductor impedance $\%Z_L$ is reduced from 2.5% to 0.075%. On the other hand, when the inverter is operated in DCM, the zero-current interval can be controlled and the dead-time-induced error voltage can be compensated simply as shown in Fig. 4. Therefore, even with the minimized inductor impedance of 0.075%, the low current THD of 0.3% is achieved with the proposed DCM current control.

Figure 7 depicts the load step response of the proposed DCM current control. As shown in Fig. 7(a), even under the sudden load step between the load of 0.1 p.u. and the load of 1.0 p.u., the stable inverter operation and the balanced three-phase currents are still achieved with the proposed control.

TABLE II
Simulation Parameters.

Circuit Parameter		
V_{DC}	DC link Voltage	500 V
v_g	Line-to-line Voltage	200 Vrms
P_n	Nominal Power	3 kW
f_g	Grid Frequency	50 Hz
Z_b	Total Impedance	13.3 Ω
f_{sw}	Switching Frequency	40 kHz
$T_{deadtime}$	Dead-time	500 ns
L_1	1st Inductor Value	1061 μH (2.5%)
L_2	2nd Inductor Value	254.6 μH (0.6%)
L_3	3rd Inductor Value	31.8 μH (0.075%)
Current Controller Parameter		
ζ	Damping Factor	0.7
f_c	Cutoff Frequency	1 kHz

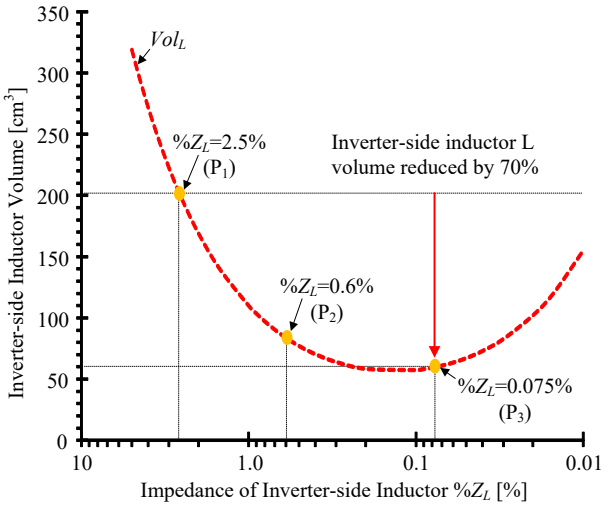
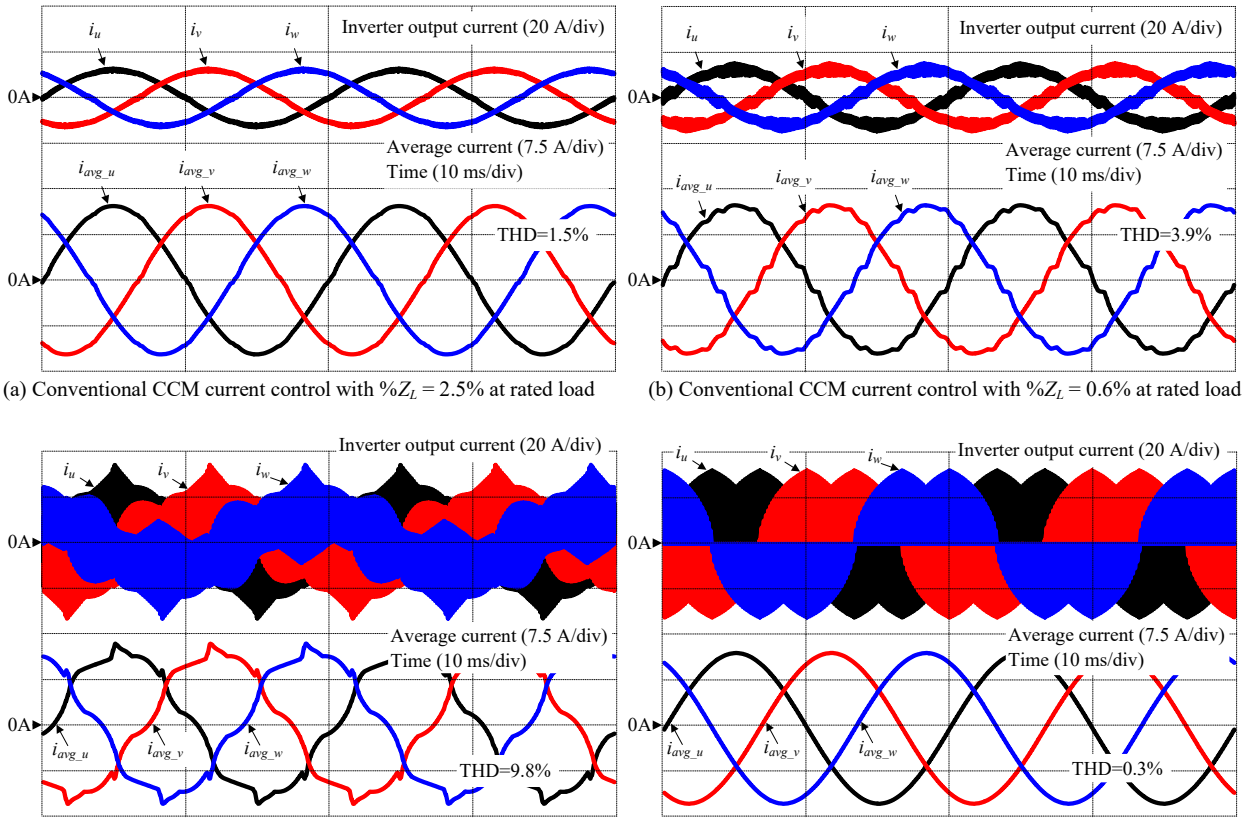


Fig. 5. Relationship between filter volume and inductor impedance at switching frequency of 40 kHz. The inductor volume can be minimized greatly when reducing the inductor impedance.

Figure 8 shows the current THD characteristics of the conventional CCM current control and the proposed DCM current control with three inductor designs from Fig. 5. At rated load with the inductor impedance of 0.075%, the current distortion of the proposed DCM current control is reduced by 97.6% compared to the conventional CCM current control. Note that the current THD of the conventional CCM current control with the inductor impedance of 0.075% or 0.6% has a tendency to decrease at light load. The reason is when the average current is significantly smaller than the current ripple, the current mode is no longer CCM but triangular current mode (TCM) [22]-[23]. In TCM, all the turn on of the switching devices is zero voltage switching. On other words, the dead-time-induced error voltage does not occur in TCM. Hence, the current distortion due to the zero-clamping phenomenon disappears at light load.



(a) Conventional CCM current control with $\%Z_L = 2.5\%$ at rated load

(b) Conventional CCM current control with $\%Z_L = 0.6\%$ at rated load

(c) Conventional CCM current control with $\%Z_L = 0.075\%$ at rated load

(d) Proposed DCM current control with $\%Z_L = 0.075\%$ at rated load

Fig. 6. Inverter output currents and average currents of conventional CCM current control and proposed DCM current control at rated load. The current THD of the conventional CCM current control increases with the reduction of the grid filter impedance, whereas the current THD of the proposed current control is still low.

IV. Laboratory Setup

Table III shows the experimental parameters, whereas figure 9 depicts the prototype of the miniature three-phase grid-tied inverter. In order to operate the inverter under DCM over entire load range with the switching frequency of 20 kHz, the inverter-side inductor value is designed at 80 μH, whose impedance is 0.5% of the total inverter impedance.

A. Discontinuous-current mode operation

Figure 10 depicts the three-phase grid-tied inverter DCM operation waveform at rated load. In Figure 10(a), the phase difference between the grid current of u phase and the grid u-phase voltage is almost zero, i.e. the unity-power-factor operation. Furthermore, even with the small inverter-side inductor impedance of 0.5%, the low current THD of 2.4% is still achieved. As shown in Figure 10(b)-(c), the three-phase inverter output currents are similar to those shown in Figure 6(c), i.e. the operation of the proposed DCM control is confirmed.

Figure 11 shows the grid phase voltages and the grid currents of u phase and w phase at the normal operation and at step-up load change. At the normal operation, the three-phase grid current is well balance and the low current THD of 2.4% is achieved for all three-phase grid current. At the step-up load change from 0.1 p.u. to 1.0 p.u., the stable current response is confirmed. Note that

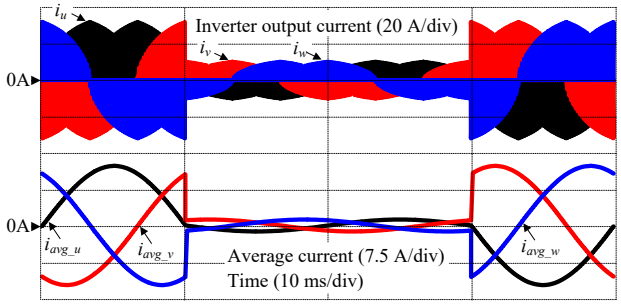


Fig. 7. Load step response between load of 0.1 p.u. and load of 1.0 p.u.. The stable inverter operation is confirmed even at load step change.

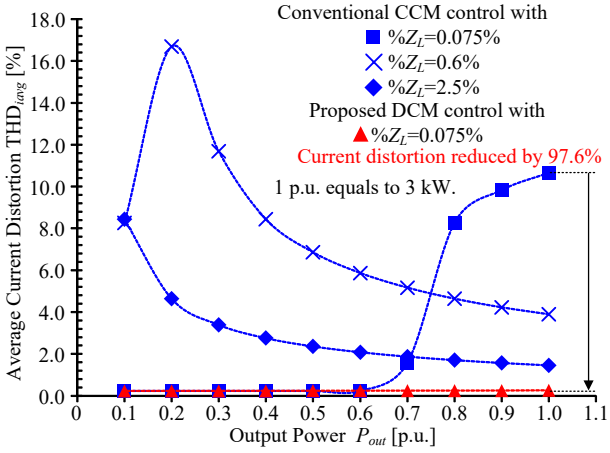


Fig. 8. Current THD characteristics of conventional CCM current control and proposed DCM current control with three different inductor designs. With the proposed DCM current control, the current THD is maintained below 5% over entire load range from 0.1 p.u. to 1.0 p.u..

TABLE III
EXPERIMENTAL PARAMETERS.

Circuit Parameter		
V_{DC}	DC link Voltage	300 V
v_g	Line-to-line Voltage	100 Vrms
P_n	Nominal Power	700 W
f_g	Grid Frequency	50 Hz
Z_b	Total Impedance	4.8 Ω
f_{sw}	Switching Frequency	20 kHz
$T_{deadtime}$	Dead-time	500 ns
L	Inductor Value	80 μH (0.5%)

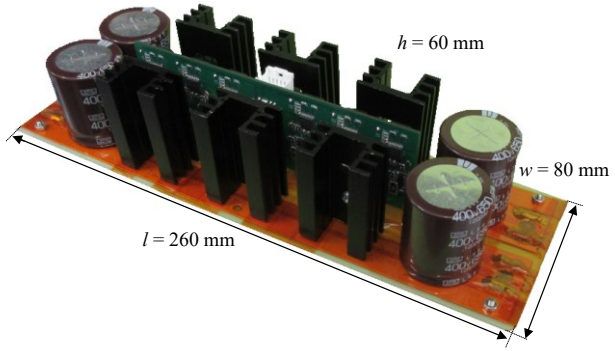


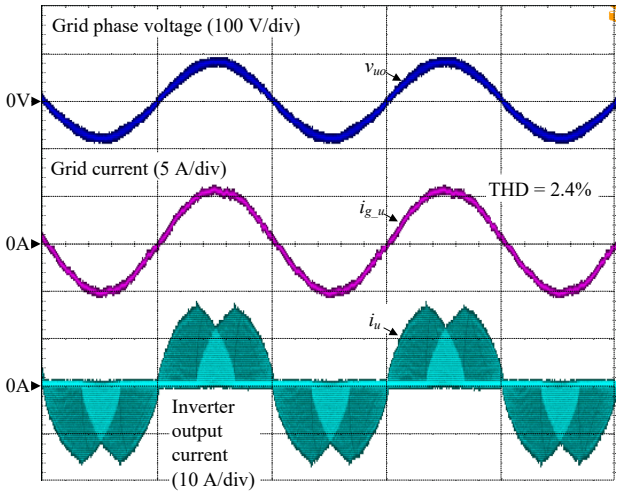
Fig. 9. Prototype of miniature three-phase grid-tied inverter.

the three-phase grid currents are still balance both before and after the step-up load change.

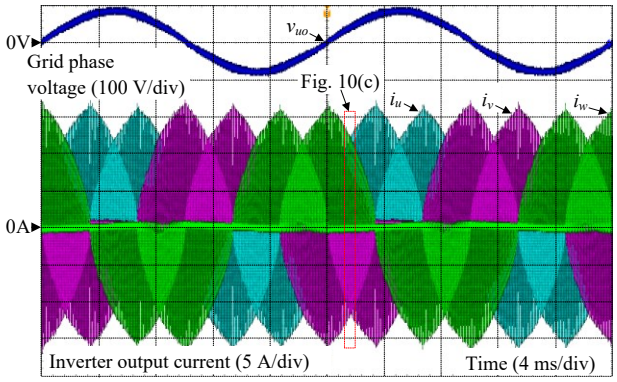
Figure 12 depicts the current THD characteristics of the proposed DCM current control. The current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u., which satisfies the current THD constraint in IEEE-1547, even when the inductance impedance is reduced to 0.5% of the inverter impedance. The increase of the current THD at light load can be explained due to the high occupation of the reactive current flowing through the filter capacitor. Therefore, in order to reduce the current THD at light load, the DCM control should also consider the effect of the reactive current in the filter capacitor.

B. *Efficiency comparison between asynchronous switching and synchronous switching in DCM*

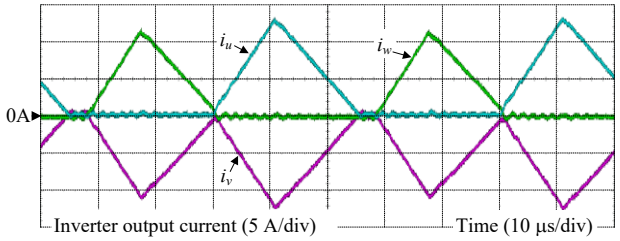
Figure 13 shows the asynchronous switching and synchronous switching in DCM. In the asynchronous switching, the corresponding switches are turned after the period D_1T_{sw} and D_3T_{sw} finish. Therefore, the current has to flow through the diode. In the next generation switching devices such as SiC or GaN, the forward voltage of the inverse diode in such devices is generally higher than that of the conventional MOS-FET devices. Consequently, the conduction loss with the asynchronous switching is higher that of the synchronous switching, where the current flows through the FET part. As shown in Figure 13, the synchronous switching can also be applied into DCM in the same manner as the conventional CCM. Consequently, the conduction loss of



(a) Grid phase voltage, grid current, and inverter output current of u phase



(b) Grid phase voltage of u phase, and three-phase inverter output currents



(c) Zoom-in three-phase grid current from Fig. 10(b)

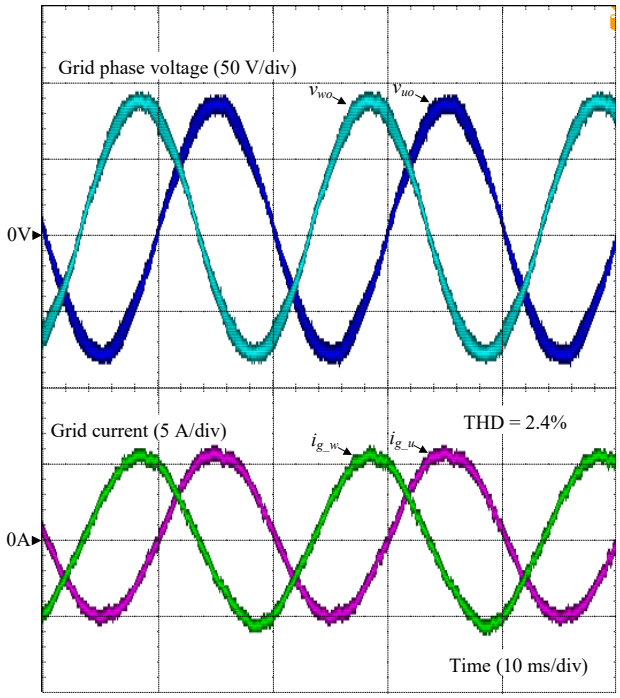
Fig. 10. Three-phase grid-tied inverter DCM operation waveform at rated load. The three-phase inverter output currents shown in Fig. 10(b) are similar to those shown in Fig. 6(c). This confirms the operation of the proposed DCM control.

the switching device is reduced.

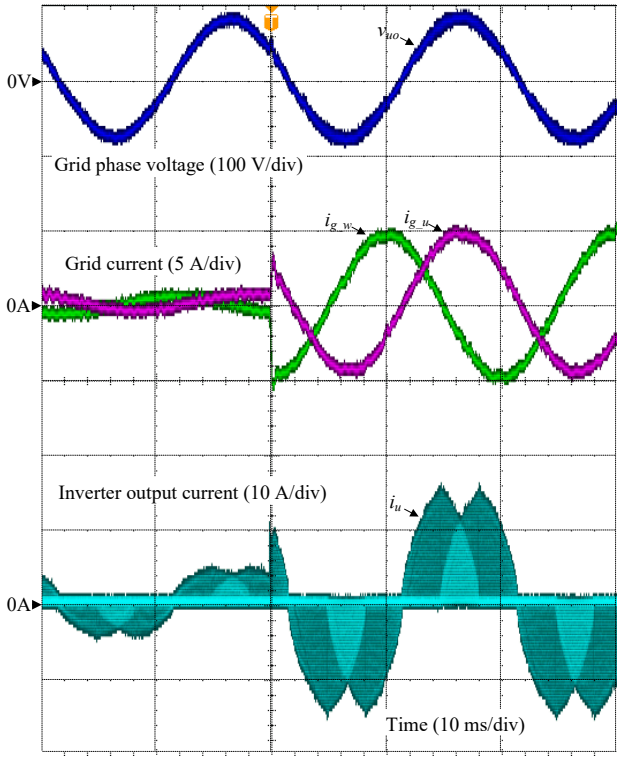
Figure 14 depicts the efficiency comparison between asynchronous switching and synchronous switching in DCM. The application of the DCM synchronous switching reduces the conversion loss by 33% compared to the DCM asynchronous switching at rated load. Furthermore, the maximum efficiency of 97.8% is achieved at rated load.

V. CONCLUSION

In this paper, the DCM current control was proposed to the grid-tied three-phase inverter in order to minimize the grid filter volume without worsening the current THD. When the inverter is operated under DCM, the zero-



(a) Grid phase voltages and grid currents of u phase and w phase at normal operation



(b) Current response of step-up load change

Fig. 11. Grid phase voltages and grid currents of u phase and w phase at normal operation and at step-up load change. Three-phase currents are balanced at normal operation as well as at step-up load change.

current interval can be controlled, compensating simply the dead-time-induced error voltage. Consequently, when the inductor impedance is reduced to 0.075%, the current THD of the proposed DCM current control is reduced by 97.6% compared to the conventional CCM current control as simulation results. In the experiments, the

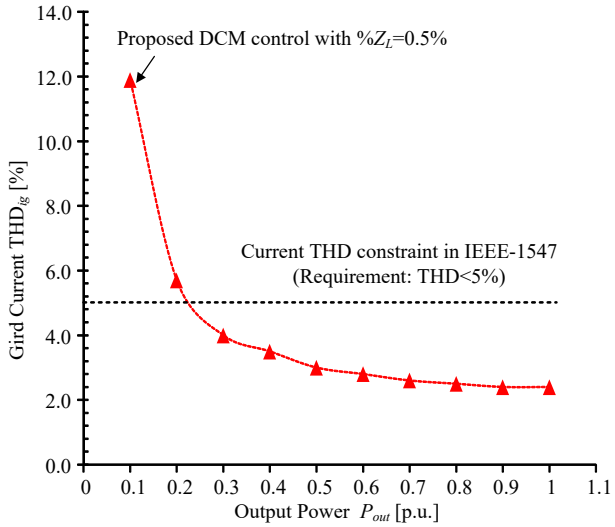


Fig. 12. Current THD characteristics of proposed DCM current control. The current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u., which satisfies the current THD constraint in IEEE-1547, even when the inductance impedance is reduced to 0.5% of the inverter impedance.

current THD was maintained below 5% over load range from 0.3 p.u. to 1.0 p.u. even when the inductance impedance is reduced to 0.5% of the inverter impedance.

In the future work, the DCM current feedback control will be considered in order to eliminate the circuit-parameter dependency.

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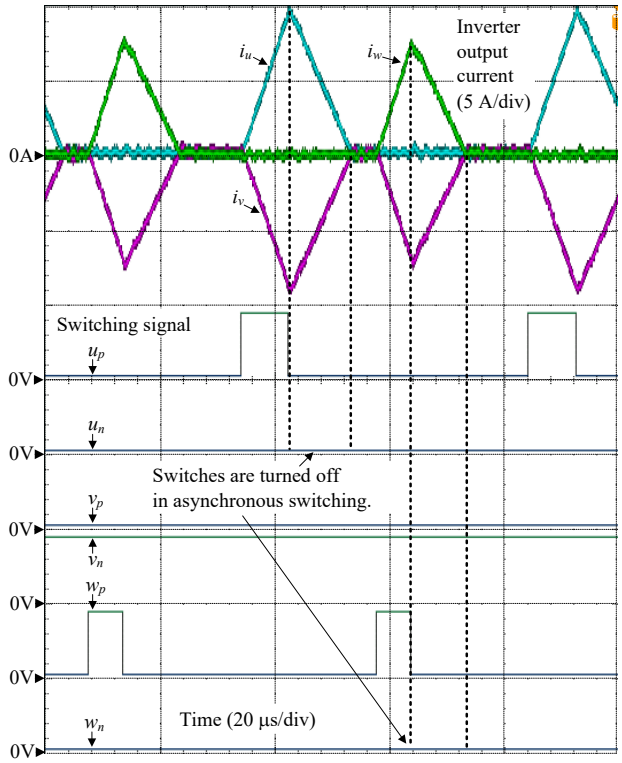
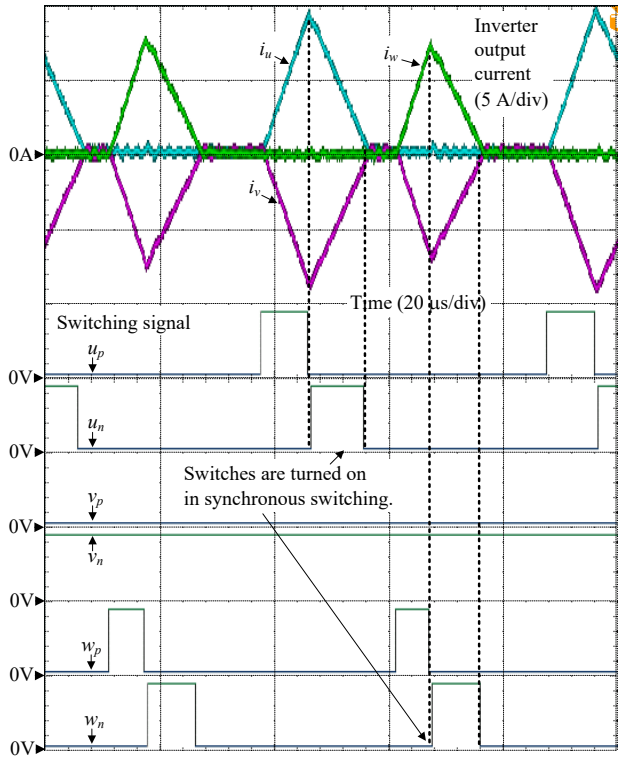


(a) Asynchronous switching in DCM



(b) Synchronous switching in DCM

Fig. 13. Asynchronous switching and synchronous switching in DCM. Similar to the conventional CCM, the synchronous switching can also be applied into DCM. This makes the current flow through the FET part instead of the diode. Consequently, the conduction loss of the switching device can be reduced.

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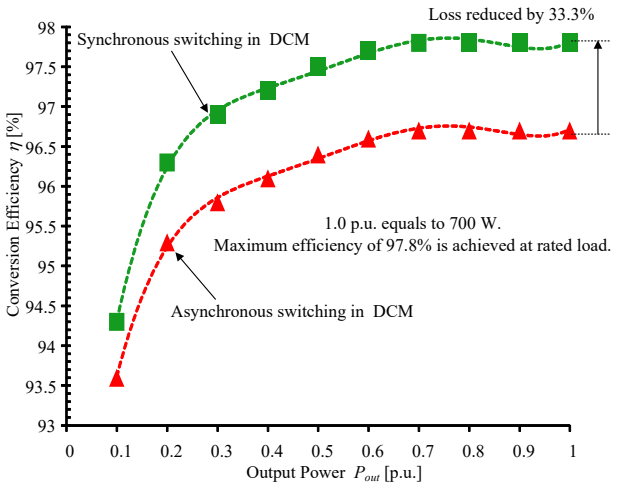

Fig. 14. Efficiency comparison between asynchronous switching and synchronous switching in DCM. The application of the DCM synchronous switching reduces the conversion loss by 33% compared to the DCM asynchronous switching at rated load.

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