Zero Voltage Switching Scheme for Flyback Converter to Ensure Compatibility with Active Power Decoupling Capability

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***Abstract*—In this paper, a novel ZVS method with synchronous rectifier is proposed in order to achieve the soft switching and the active power decoupling without additional component. The proposed method separates the ZVS operation and the snubber capability to keep the discontinuous current mode (DCM) for the power decoupling. In addition, an active clamp circuit which achieves soft switching operation is applied for the surge voltage suppression of a main switch. From the experimental results, 0.4% of a second-order harmonics on a DC input current is obtained in comparison with a DC component. In addition, it is confirmed that the surge voltage is reduced by 50% owing to the active clamp circuit, and the ZVS operation by the experiment.**

Keywords— micro inverter; active power decoupling; zero voltage switching

I. INTRODUCTION

Recently, micro inverter systems for PV applications are actively researched for a sustainable power solution due to the attractive characteristics such as; flexibility, high-system efficiency, and low manufacturing cost [1]. The micro inverter promisingly becomes a trend for the future PV system instead of the large capacity inverters, and the micro inverter requires the high reliability because the large number of the converter units are adopted to the PV generation system. Generally, in the power converter for DC to single-phase AC grid system, an electrolytic capacitor is usually employed owing to the large capacitance for the double-line frequency power ripple compensation. These capacitors limit the life-time of the converter, which results in low reliability.

According to this problem, the active power decoupling techniques which have a film or ceramic capacitor are attracted as the one of this solution [2]-[9]. The active power decoupling circuit charges and discharges the decoupling capacitor in order to absorb the double-line frequency power ripple, which enables to small capacitance. As a result, large electrolytic capacitor does not necessary. However, a lot of conventional active power decoupling circuits require the additional components such as the switching devices and the additional inductor. Although the low cost is the one of the advantages in the micro inverter, these components increase complexity of the circuit configuration and the cost. Therefore, the active power decoupling technique which utilize the discontinuous current mode (DCM) was already proposed by authors [10], and it reduces the DC link capacitance without the additional components.

The ZVS techniques for the flyback converter have been hot research topics in order to reduce the switching losses and the voltage stress due to the leakage energy of transformer [11]. The quasi-resonant (Q-R) operation is the one method, which adjusts the switching timing to the zero voltage by a pulse frequency modulation (PFM) [12].

The other technique utilizes an active clamp circuit for the ZVS operation. In this method, the magnetizing current becomes negative due to the series resonance between the leakage inductance and the clamp capacitor, and the parasitic capacitor is discharged before turn-on. As a result, the ZVS operation is obtained.

In the active power decoupling technique by authors, the flyback converter has to limit the operation condition because it is achieved under the constant switching frequency and the DCM operation. In this case, the conventional ZVS method as the Q-R operation and the active clamp circuit cannot apply to the proposed converter. This is because the Q-R operation needs the PFM, and conventional active clamp method has to operate under the continuous current mode (CCM).

This paper proposes a novel ZVS scheme to ensure compatibility with the active power decoupling circuit. For that, the synchronous rectifier is applied instead of the diode rectifier. In addition, the active clamp circuit is only used to reduce the turn-off surge voltage of the main switch. The originality of this paper is that the switching pattern is added to a synchronous rectifier for ZVS operation. Similar ZVS method with forward converter was already reported by Ref. [13], however, this method is also operated under the CCM condition. The differential point is that the proposed converter needs the zero current period of the magnetizing current for power decoupling. In addition, the magnetizing current should be negative to discharge the parasitic capacitor of the main switch. In order to satisfy these condition, the conduction modes for the synchronous rectifier switch is turned-on before the main switch is turned-on, and the active clamp circuit is turned-off when the released energy of the magnetizing

inductance becomes zero to ensure the zero current period for DCM. Finally, the active power decoupling and the ZVS operation is confirmed by experiment.

II. CIRCUIT CONFIGURATION

Fig.1 shows a conventional micro inverter topology with the conventional active power decoupling circuit [14]. In order to reduce the buffer capacitance C_{buf}, the small decoupling capacitor C_{apd} and the auxiliary circuit are adopted on the transformer secondary side. The decoupling capacitor C_{apd} is charged and discharged in synchronized with the double-line frequency to compensate the power ripple with small capacitor. However, these additional components complex the circuit configuration, and the transformer has to compose the three winding transformer which has complicate configuration.

Fig. 2 shows the proposed converter which consists of the flyback converter, the voltage source inverter (VSI) and small buffer capacitor C_{buf}. The flyback converter isolates between the PV and the single-phase grid, and it has the high voltage gain to push up the DC input voltage. The proposed converter compensates the double-line frequency power ripple by the small DC link capacitor C_{buf} without additional components. In addition, the active clamp circuit is applied for the surge voltage suppression due to the leakage energy of the transformer. Moreover, the synchronous rectifier is implemented for the ZVS operation and the reduction of the conduction losses.

The hard switched flyback converters undergo substantial switching losses in the high switching frequency and high voltage stress on the each switching devices. This is because the parasitic capacitor of S_1 is quickly charged due to the leakage energy. Typically, The RCD snubber is connected to primary side in order to suppress the huge surge voltage. However, the reduction of the switching losses and the snubber losses is the important to improve the conversion efficiency. According to these reason, the active clamp circuit is considered. The leakage energy transfers to the clamp capacitor C_{clamp} when the active clamp switch S_{clamp} is turned-on. In order to reduce the peak surge voltage, the C_{clamp} should be large to delay the charge period in comparison with the parasitic capacitor.

Fig. 3 shows the principle of the power decoupling between the DC and single-phase AC sides. The proposed active power decoupling separates the DC component and double-line frequency component by the flyback converter. Thus, the DC input power P_{in} is always constant, and the DC link capacitor C_{buf} stores the differential power between input and output power.

When both the output voltage and current waveforms are sinusoidal, the instantaneous output power p_{out} is expressed as

$$p_{buf} = \frac{V_{acp} I_{acp}}{2}(1-\cos 2\omega t) \qquad (1)$$

where V_{acp} is the peak voltage, I_{acp} is the peak current, and ω is the angular frequency of the output voltage. From (1),

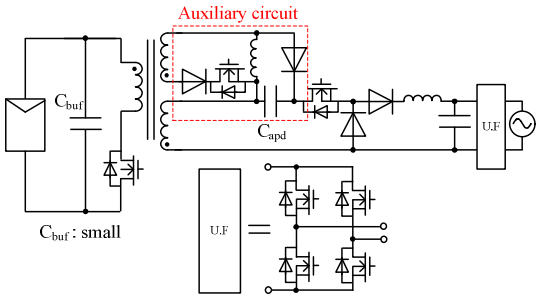


Fig 1. Conventional flyback micro inverter with active power decoupling circuit. It can reduce the capacitance of C_{buf}. However, auxiliary circuit is necessary.

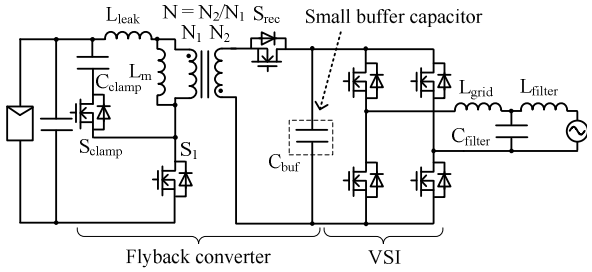


Fig 2. Circuit configuration of proposed flyback converter. Active clamp circuit suppress turn-off surge voltage. Synchronous rectifier utilizes ZVS operation for S_1.

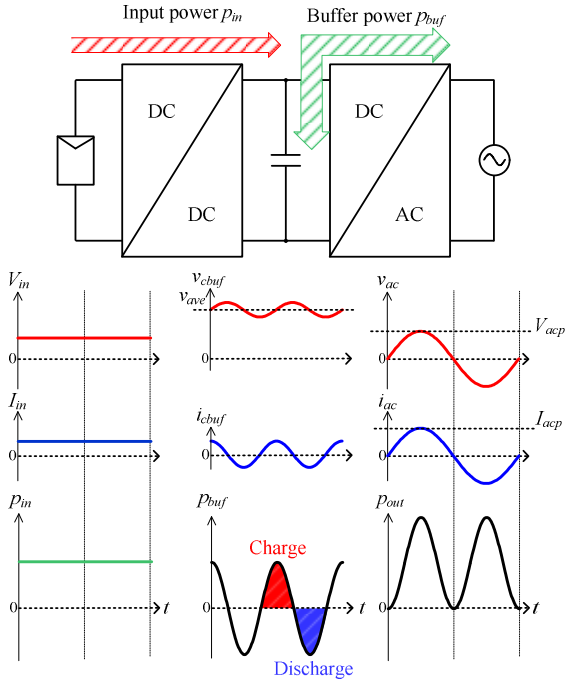


Fig 3. Relationship between input and output power. DC link capacitor receives differential power due to double-line frequency power ripple, and input power becomes constant.

the power ripple that contains double-line frequency of the power grid, appears at DC link.

In order to absorb the power ripple, the instantaneous power p_{buf} is expressed as

$$p_{buf} = \frac{1}{2} V_{acp} I_{acp} \cos 2\omega t \qquad (2)$$

where, the polarity of the p_{buf}, is defined as positive when the DC link capacitor C_{buf} discharges. Note that the active power of C_{buf} should be zero. Owing to the power decoupling capability, the input power is matched to the output power. Thus, the relationship between the input and output power is expressed as

$$p_{pv} = \frac{1}{2} V_{acp} I_{acp} = V_{in} I_{in} \tag{3}$$

The proposed converter achieves the active power decoupling by the DC link capacitor C_{buf}. As a result, the DC link voltage v_{cbuf} fluctuates at the double-line frequency of the single-phase grid frequency as Fig. 3.

III. OPERATION MODES OF PROPOSED CONVERTER

A. Active power decoupling operation

Fig. 4 shows the drain current waveforms of the main switch S_1 without active clamp circuit. The proposed active power decoupling method is very simple, and the detail is following.

Firstly, the average primary current both CCM and DCM are expressed as

$$I_{ave\_CCM} = \frac{V_{dc}}{V_{in}} I_{dc} \tag{4}$$

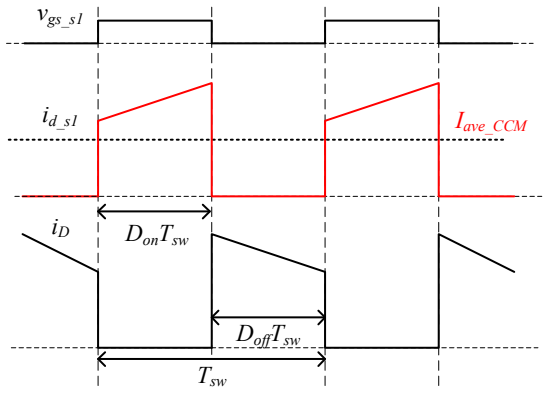
$$I_{ave\_DCM} = \frac{I_{peak}}{2} D_{on} \tag{5}$$

$$I_{peak} = \frac{V_{in}}{L_m} D_{on} T_{sw} \tag{6}$$

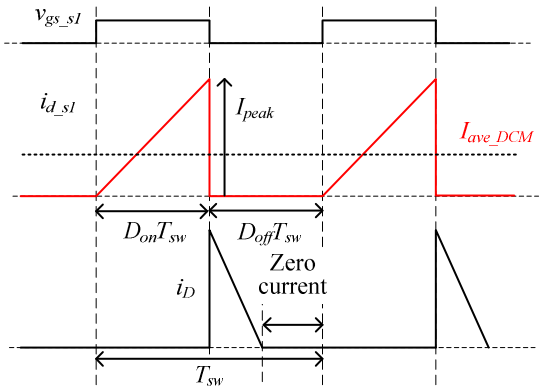
where, I_{ave_ccm} is the average current in CCM, V_{dc} is the DC link voltage, I_{dc} is the DC link current, V_{in} is the DC input voltage, L_m is the magnetizing inductance, D_{on} is the on duty ratio of the main switch S_1, T_{sw} is the switching period. Note that, the V_{dc} fluctuates at double-line frequency when the DC link capacitor is small. In the CCM condition, the PV side average current I_{ave_ccm} is decided from DC link parameters such as V_{dc} and I_{dc}. As a result, the power decoupling fails.

On the other hand, the PV side average current in DCM I_{ave_DCM} is only decided primary parameters such as DC input voltage, and the switching period and on duty. In order to achieve the active power decoupling, the proposed converter is operated by the constant on duty reference and the constant switching frequency. As a result, constant average current is obtained, and the double-line frequency power ripple does not occurs on PV side.

Fig.5 shows the current waveforms of the DC input current I_{in}, DC link current i_{dc}, and the inverter output current i_{ac}. The proposed converter obtains the constant input power by the flyback converter, and the DC link capacitor C_{buf} compensates the power ripple due to single-phase AC grid. In this case, the DC link current includes



(a) Continuous current mode (CCM)



(b) Discontinuous current mode (DCM)

Fig.4. Fundamental waveforms without active clamp circuit. In DCM, power decoupling can achieve under constant duty reference and switching frequency condition.

the charge and discharge current of C_{buf}, and it has the double-line frequency component as Fig. 5.

According to these method, the proposed converter decouples the DC components and the double-line frequency components. However, it limits the operation condition of the flyback converter to constant duty command and switching frequency. As a result, the conventional ZVS techniques cannot apply to the proposed converter. This is because the Q-R operation needs the PFM. In addition, the ZVS with the active clamp circuit is operated under the CCM condition. In order to solve this problem, the new ZVS method is proposed from the next chapter.

B. Operation modes of flyback converter

Fig. 6 shows the key ZVS switching waveforms of the conventional and proposed method. The large surge voltage occurs on main switch S_1 due to the resonance between leakage inductance L_{leak} and the parasitic capacitor of S_1 at turn-off transition when the snubber circuit does not places. The active clamp circuit suppresses the peak drain-source voltage V_{ds_s1} by the clamp capacitor C_{clamp}, and the clamp voltage is expressed as

$$V_{dS\_s1} = V_{in} + \frac{V_{dc}}{N} \tag{7}$$

where, N is the turn ratio of the transformer.

According to Fig. 6 (a), the active clamp circuit is used for both the ZVS operation and the surge voltage suppression. The active clamp switch S_{clamp} and S_1 are switched to complementation through the dead-time period [15]. At the dead-time before turn-on of S_1, the magnetizing current i_{Lm} reaches to the negative current. In this state, the parallel diode is turned-on, and the parasitic capacitor discharged. As a result, ZVS is achieved at S_1. However, this method is only applied the continuous current mode, and it disturbs the proposed power decoupling operation as (4). Thus, the magnetizing current has to become discontinuous current for the proposed power decoupling.

Fig. 6 (b) shows the proposed ZVS method using synchronous rectifier. In the proposed method, the active clamp circuit is only used for the surge voltage suppression. Instead, synchronous rectifier switch S_{rec} has the turned-on state before turn-on of S_1 in order to generate the negative current for ZVS.

Fig.7 shows the operation modes of the proposed flyback converter, and the detail of each mode are described in the following.

Mode 1 (t_0 - t_1):

In mode 1, the main switch S_1 is turned-on, and the active clamp switch S_{clamp} is remaining off-state. The DC input voltage is applied to the transformer and each energy storage. The magnetizing current linearly increases until the end of the mode 1, and the energy is stored both leakage inductance and magnetizing inductance.

Mode 2 ($t_1 - t_2$, dead-time):

This mode starts when the main switch S_1 is turned-off. In this mode, the energy of the leakage inductance L_{leak} is transferred to the parasitic capacitor C_{oss}. In this mode, the synchronous rectifier switch S_{rec} and the parallel diode of S_{rec} is remaining off-state. Thus, the primary side composes the series resonance circuit with L_m, L_{leak} and C_{oss}. Note that C_{oss} is very small, and it is charged quickly. This mode is the end when the V_{ds_s1} reaches to (7).

Mode 3 ($t_2 - t_3$, dead-time):

This mode starts when the parallel diode of S_{rec} and S_{clamp} is turned-on, and the magnetizing inductor energy is released and delivered to the VSI side. L_{leak}, C_{clamp} are resonant during in this interval. This mode is the end when the S_{clamp} is turned-on.

Mode 4: ($t_3 - t_4$)

This mode starts when S_{rec} and S_{clamp} is turned-on. The period of this interval is set to the energy release period of the magnetizing inductance, and it is expressed as

$$T_{t3-t4} = I_{peak} \frac{NL_m}{V_{dc}} \qquad (8)$$

where, I_{peak} is the magnetizing peak current, N is the turn ratio of the transformer, L_m is the magnetizing inductance, and the V_{dc} is the DC link voltage. At the $t = t_3$, S_{clamp}

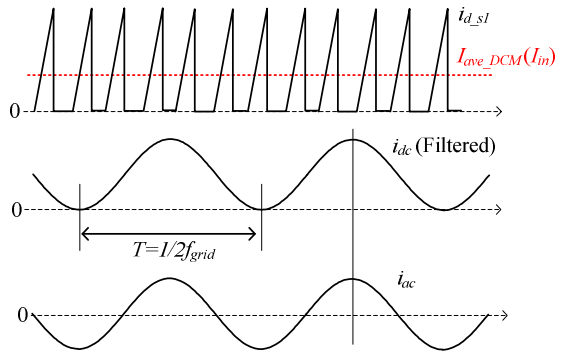
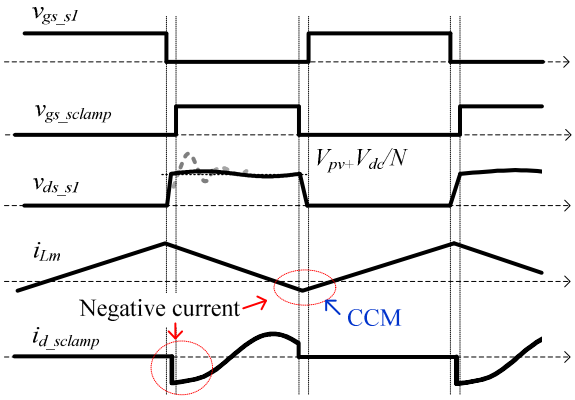
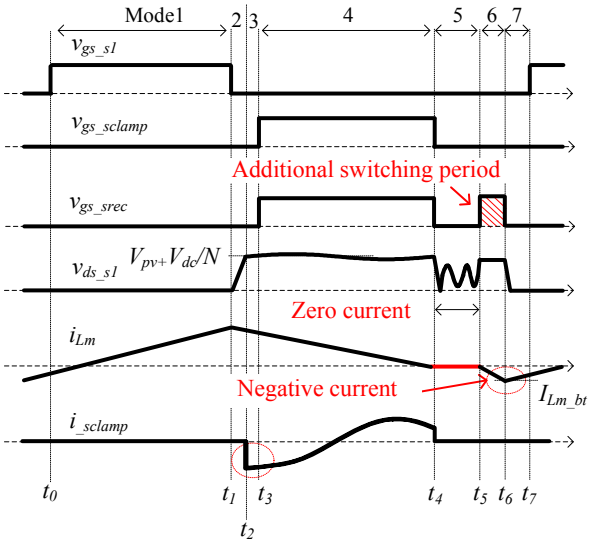


Fig.5. Current waveforms of PV input current I_{ave_DCM}, DC link current i_{dc} and inverter output current i_{ac}. DC link capacitor is charged and discharged due to double-line frequency in order to compensate the differential power during input and output power.



(a) Conventional ZVS method with active clamp circuit. This method, active clamp circuit and main circuit are switched to complementation.



(b) Proposed ZVS method with active clamp circuit.

Fig.6. Key waveforms of flyback converter in switching cycle. In order to achieve ZVS, negative current period is necessary before S_1 is turned -on. In addition, zero current period is required for proposed active power decoupling capability.

achieves the ZVS because the parasitic capacitor of S_{clamp} is already discharged before the turn-on.

Mode 5: $(t_4 - t_5)$

This modes starts when the magnetizing current becomes zero. The all switches are tuned-off, and the magnetizing current remaining zero. The proposed active power decoupling method operates under DCM. Thus, this mode is important in order to achieve the active power decoupling capability without the additional components. In this interval, the primary side composes the series resonance circuit with L_m, L_{leak} and C_{oss}, and the voltage oscillation occurs. The resonance period is expressed as

$$T_{res} = 2\pi\sqrt{(L_{leak} + L_m)C_{oss}} \tag{9}$$

Mode 6: $(t_5 - t_6)$

This mode is for the ZVS operation of the main switch S_1. The negative voltage provides to the transformer, and the magnetizing current reaches negative when the synchronous rectifier S_{rec} is turned-on. The bottom current of the magnetizing inductance I_{Lm_bt} is expressed as

$$I_{Lm\_bt} = \frac{V_{dc}}{NL_m} T_{t5-t6} \tag{10}$$

Mode 7 ($t_6 - t_7$, dead-time):

At the $t = t_6$, the magnetizing current is remaining negative. In this interval, the parasitic capacitor C_{oss} is discharged, and the drain source voltage $v_{ds\text{-}s1}$ is decreased to zero. After that, the parallel diode of S_1 is turned-on. After this mode, S_1 is turned-on, and the ZVS is achieved.

The proposed converter is added the switching state of mode 6 and 7 for ZVS. Due to these modes, the parasitic capacitor C_{oss} is discharged before turn-on of S_1. In addition, the operation mode of the proposed converter has the zero current period as mode 5, and the magnetizing current becomes discontinuous current. As a result, the proposed power decoupling is also achieved.

C. Control block diagram

The control block diagrams of the flyback converter is shown in Fig. 7. The Flyback converter operates by the constant duty reference and switching frequency. In order to avoid the short circuit between S_1, S_{clamp}, and S_{rec}, the dead-time is implemented after modulation part. In addition, the dead-time of S_1 is separated to two steps for generation of the synchronous rectifier on-state.

According to (5), the PV side average current is decided by the peak current of the magnetizing current, and the on duty including the dead-time period is expressed as

$$D_{on\_s1} = D_{ref} - \frac{T_{dead}}{T_{sw}} \tag{11}$$

$$T_{dead} = T_{d1} + T_{d2} \tag{12}$$

where, T_{dead} is the dead-time period, and it is the sum of the dead-time T_{d1} and T_{d2}. The turn-on period of S_{clamp} equal to the energy release period of the magnetizing inductance, and it is expressed as

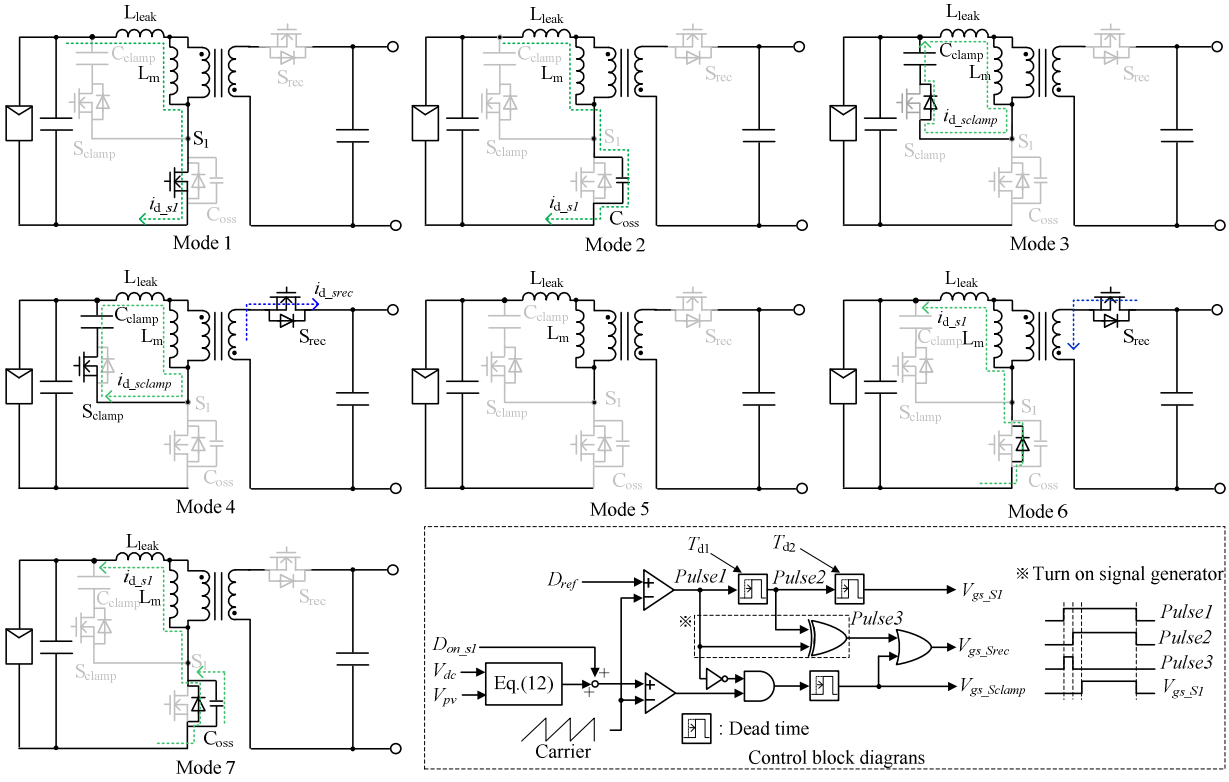


Fig.7. Operation modes and the control block diagrams of flyback converter. In order to achieve ZVS, mode 6 and 7 which discharge the parasitic capacitor are proposed.

$$D_{on\_sclamp} = \frac{NV_{pv}}{V_{dc}} D_{on\_s1} \quad (13)$$

The gate signals for S_{rec} is the sum of the active clamp switch gate signals V_{gs_sclamp} and the turn-on signals for ZVS (e.g. *Pulse 3*). Note that, pulse period is set by the dead-time of T_{d1}.

IV. SIMULATION RESULT

Table. 1 shows the simulation parameters. In this simulation, the leakage inductance L_{leak} and the parasitic capacitor C_{oss} is adopted to evaluate the ZVS operation. In order to suppress the surge voltage, the clamp capacitor is set to 10μF.

Fig. 8 shows the switching waveforms with the diode rectification and the proposed method. Firstly, the surge voltage is suppressed by the Active clamp circuit both condition. However, according to Fig. 8 (a), the drain-source voltage v_{ds_s1} does not zero when the S_1 is turned-on, and the magnetizing current becomes positive value. It is meaning that the hard-switching condition occurs, and the parasitic capacitor cannot be discharged by the magnetizing current.

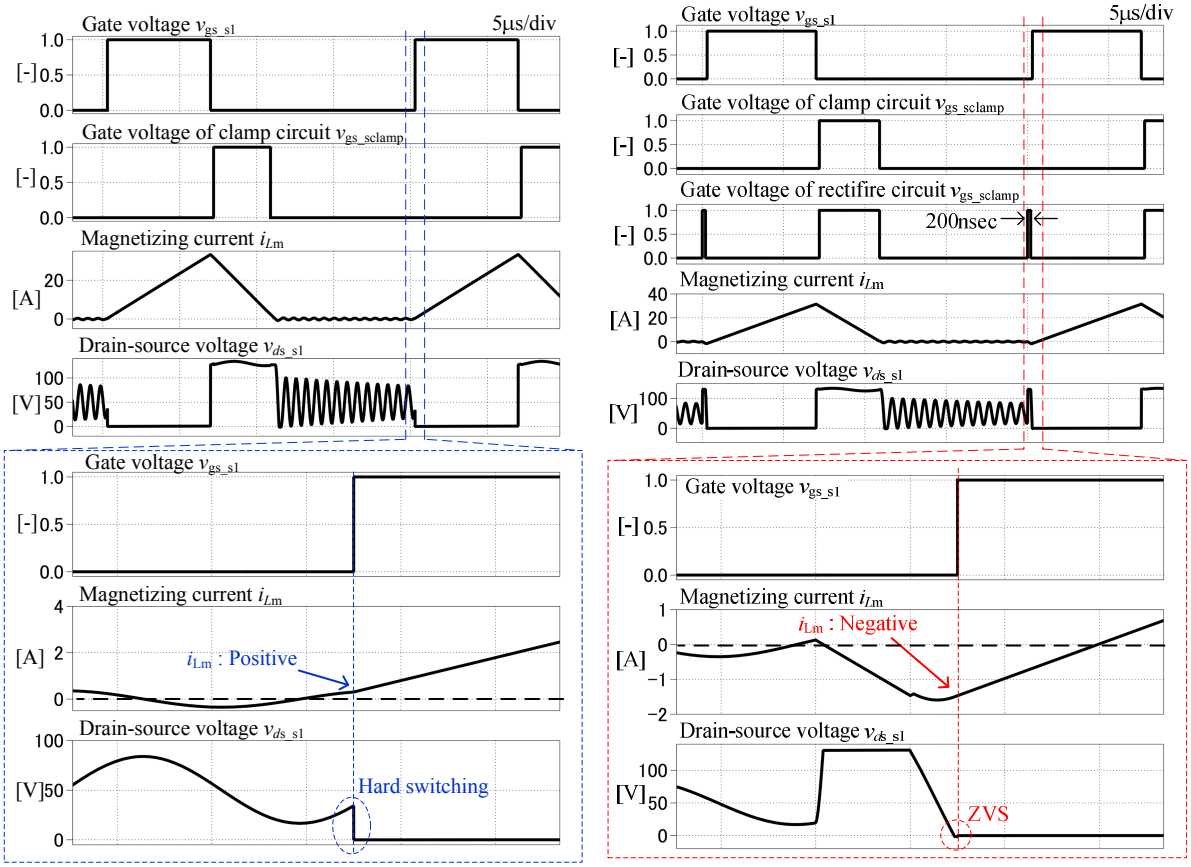
On the other hand, according to Fig. 8 (b), the v_{ds_s1} becomes zero before the turn-on of S_1. In addition, it is confirmed that the magnetizing current becomes negative value at dead-time period. From these result, the operation of the proposed method is confirmed. Note that, the conduction mode of the rectifier circuit is necessary in order to achieve ZVS, and the conduction losses becomes increase on the synchronous rectifier circuit without the ZVS operation. However, the additional conductive period is short, and the secondary current is small in comparison with the primary current. Thus, the increase of conduction losses is small.

V. EXPERIMENTAL RESULT

Table. 2 shows the experimental parameters. This chapter presents experimental results using 300 W prototype drawn in Fig. 2 to confirm the active power decoupling operation and the proposed ZVS method. Note that VSI is operated under the open loop control with R-L load. Besides, the duty command compensation is applied to the VSI control. This is because the DC link voltage

Table.1 Simulation parameters

Symbol	Quantity	Value
V_{in}	Input voltage	50 V
P_{in}	Input power	300 W
f_{sw}	Switching frequency	50 kHz
L_m	Magnetizing inductance	10 μH
L_{leak}	Leakage inductance	100 nH
C_{oss}	Parasitic capacitor	1000 pF
C_{dc}	DC link capacitor	50 μF
C_{clamp}	Clamp capacitor	10 μF



(a) Diode rectifier (b) Proposed method

Fig.8. Simulation result with switching waveforms both diode rectifier and proposed method

fluctuates by the power decoupling operation. The switching frequency is set to 50 kHz, and the decoupling capacitor is selected to 33μF in order to apply the small film capacitor.

Fig. 9 shows the input and output waveforms with proposed method. According to Fig. 9 (a), the DC input current is regulated under the constant value, and the DC link capacitor voltage fluctuates at the double-line frequency as 100 Hz owing to compensate the single-phase AC power ripple. In addition, the sinusoidal waveforms of the inverter output voltage and current are obtained. According to Fig. 9 (b), the second order harmonics of 100 Hz is 0.4% by the DC components. From this result, the power decoupling operation with 33μF is confirmed by experiment.

Fig. 10 shows the experimental results which does not use the snubber circuit and the proposed method. Note that the evaluation of the surge voltage suppression and the ZVS operation is confirmed by light load condition because the huge surge voltage occurs by snubber less condition. As shown in Fig. 10, the surge voltage occurs when the S_1 is turned-off due to the leakage inductance of the transformer. In addition, the current oscillation also occurs at turn-on period by the hard switching operation. In order to improve these waveforms, the active clamp circuit and the proposed method is applied in Fig. 11.

Fig. 11 shows the switching forms with active clamp circuit and proposed method at light load condition. Note that, Fig. 11 (a) is the diode rectifier condition, and the synchronous rectifier is constantly turned-off. According to Fig.11 (a), the surge voltage is suppressed by 50% using the active clamp circuit. However, the current oscillation cannot improve due to the hard switching operation as shown in Fig. 11(c).

According to Fig. 11 (b), the surge voltage suppression and the ZVS are achieved by the active clamp circuit and the proposed method. As shown in Fig. 11 (d), the drain-source voltage of S_1 becomes zero before the S_1 is turned-on. From these results, the active power decoupling and the ZVS operation are confirmed by the experiment.

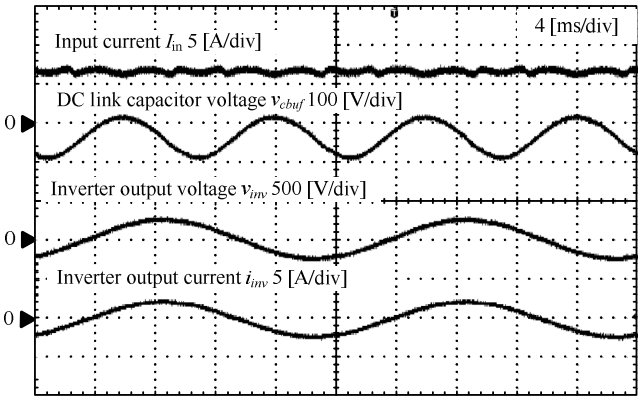
VI. CONCLUSION

This paper discussed ZVS operation method of the flyback converter with the active power decoupling capability. The proposed method converter is operated under constant frequency and duty command for the active power decoupling, and the synchronous rectifier is applied in order to achieve ZVS for the flyback converter. From the experimental result, the second-order harmonics in the DC input current becomes 0.4% of the DC average current. Finally, the surge voltage suppression and the ZVS operation are confirmed by the experiment.

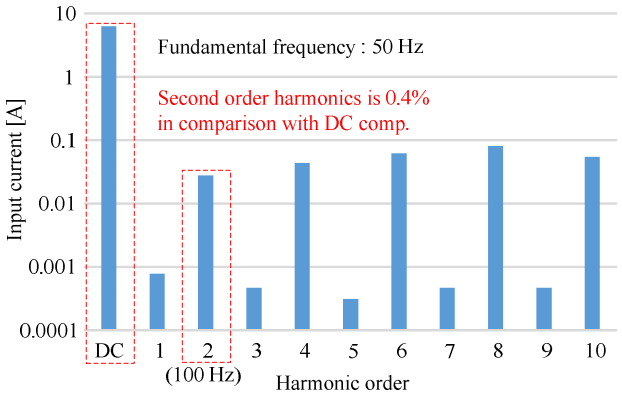
In the future work, the circuit design and operation optimization will be considered in order to improve the conversion efficiency.

Table.2 Experimental parameters

Symbol	Quantity	value
V_{in}	Input voltage	50 V
P_{in}	Input power	300 W
f_{sw}	Switching frequency	50 kHz
D_{ref}	On duty command	0.5
L_m	Magnetizing inductance	11 μH
L_{leak}	Leakage inductance	250 nH
C_{oss}	Parasitic capacitor of S_1	1100 pF
C_{clamp}	Clamp capacitor	6 μF
C_{buf}	Decoupling capacitor (DC link cap.)	33 μF
R_{load}	Road	120 Ω



(a) Input and output waveforms



(b) DC input current harmonic analysis result

Fig.9. Experimental results with over all operation waveforms and DC input current harmonic analysis result.

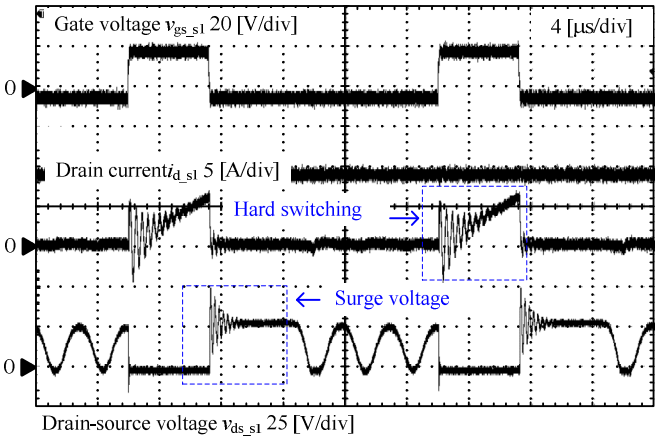


Fig.10. Experimental results with snubber less and diode rectifier condition.

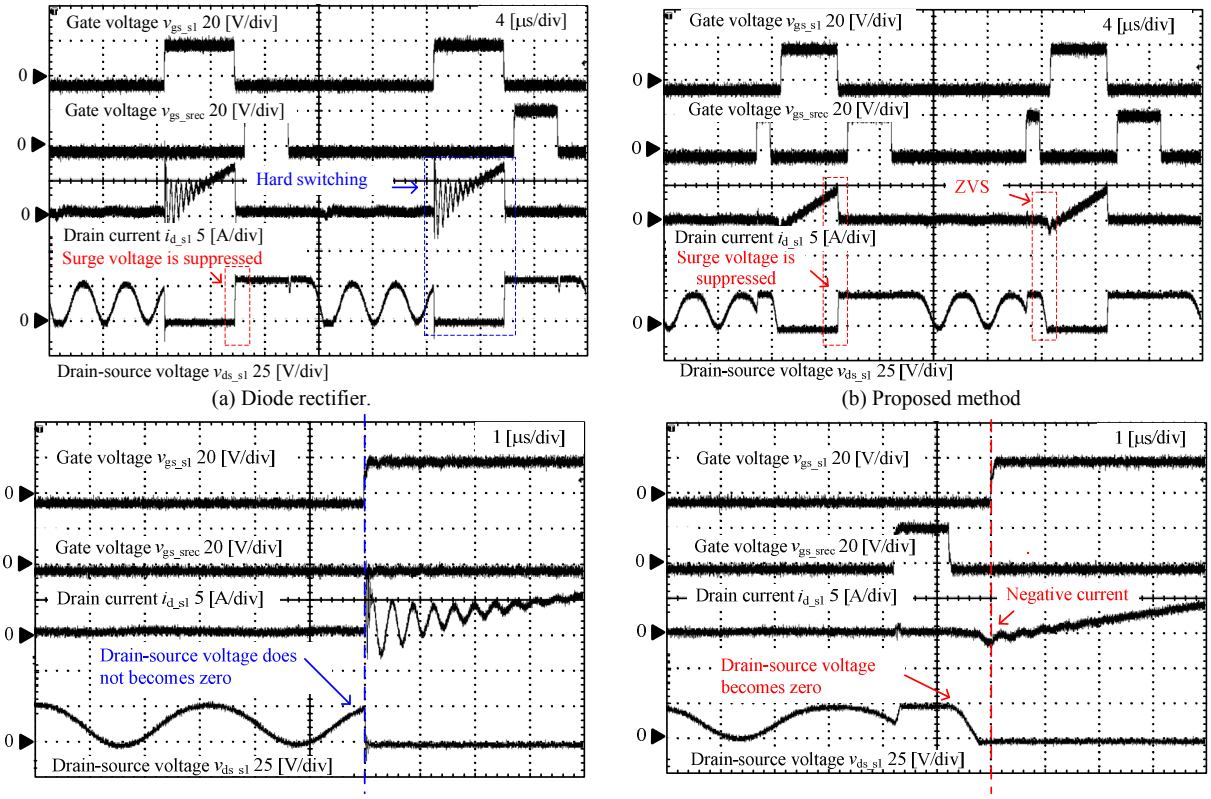


Fig.11 Experimental result with switching waveforms both hard switching condition and ZVS condition.

VII. ACKNOWLAGEENT

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REFERENCES

[1] H-I Hsieh, and J. Hou, "Realization of Interleaved PV Microinverter by Quadrature-Phase-Shift SPWM Control", *IEEJ Journal of Industry Applications*, Vol.4, No.5, pp.643-649, (2015)

[2] C.-T. Lee; Y.-M. Chen; L.-C. Chen; P.-T. Cheng;" Efficiency improvement of a DCAC converter with the power decoupling capability" *IEEE Appl. Power Electron. Conf Expo.*,pp. 1462-1468, (2012)

[3] C. B. Barth; I. Moon; Y. Lei; S. Qin; C. N. Robert; Pilawa-Podgurski;" Experimental evaluation of capacitors for power buffering in single-phase power converters" *IEEE Energy Conversion Congr. Expo.*,pp. 6269-6276, (2015)

[4] W. Liu; K. Wang; H. S.-h. Chung; S. T.-h. Chuang;"Modeling and Design of Series Voltage Compensator for Reduction of DC-Link Capacitance in Grid-Tie Solar Inverter" *IEEE Trans. Power Electron.* Vol. 30, No.5, pp. 2534-2548, (2015)

[5] C. Y. Wu; C. H. Chen; J. W. Cao; M. T. Liu; " Power control and pulsation decoupling in a single-phase grid-connected voltage-source inverter" Tencon 2013., pp. 475-479, (2013)

[6] K. H. Chao, P.T. Cheng: "Power decoupling methods for single-phase three-poles AC/DC converters", *IEEE Energy Conversion Congr. Expo.*, pp.3742-3747, Sep. (2009)

[7] Shota Yamaguchi, and Toshihisa Shimizu,"Single-phase Power Conditioner with a Buck-boost-type Power Decoupling Circuit,"*IEEJ. Journal of Industry Applications*, vol. 5, no. 3, pp. 191-198, (2016)

[8] R. Wang, F. Wang, R. Lai, P. Ning, R. Burgos, D. Boroyevich : "Study of Energy Storage Capacitor Reduction for Single Phase PWM Rectifier" *2009 Twenty-Fourth Annu. IEEE Appl. Power Electron. Conf. Expo.*, pp1177-1183, Feb. (2009)

[9] C.-T. Lee, Y.-M. Chen, L.-C. Chen, P.-T. Cheng: "Efficiency Improvement of a DC/AC Converter with the Power Decoupling Capability", *2012 Twenty-Fourth Annu. IEEE Appl. Power Electron. Conf Expo.*, pp1462-1468, Feb. (2012)

[10] H. Watanabe, J. Itoh: "Highly-reliable Fly-back-based PV Micro inverter Applying Power Decoupling Capability without Additional Components", PCIM2017, pp. 681-688 (2017)

[11] M. A. Rezaei, K-J Lee, A, Huang "A High-Efficiency Flyback Micro-inverter With a New Adaptive Snubber for Photovoltaic Applications", *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 318-327, (2016)

[12] X. Xie, J. Li, K. Peng, C. Zhao, Q. Lu: "Study on the Single-Stage Forward-Flyback PFC Converter With QR Control", *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 430-442, (2016)

[13] T. Tanaka, K. Hirachi, J. itoh: "A novel control strategy for active clamping single ended forward DC/DC converter", IEEJ, Vol.36, pp.41-47 (2011) (Japanese).

[14] C.-Y. Liao, W.-S. Lin, C-Y- Chou: "A PV Micro-inverter with PV Current Decoupling Strategy", *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6544-6557 (2016)

[15] R. Hasan, S. Mekhilef: "A Resonant Double Stage Microinveters for PV Application", *IEEE Appl. Power Electron. Conf Expo.*, pp2051-2056, (2017)