T-type NPC Inverter with Active Power Decoupling Capability using Discontinuous Current Mode

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Keywords

«DC power supply», «Single phase system», «Microgrid»

Abstract

This paper proposes a power decoupling control method based on a discontinuous current mode for a T-type NPC inverter. In general, additional components such as buffer capacitors and inductors are required in order to provide a power decoupling circuit to inverters. These components lead an increase in circuit volume and weight. In the proposed current control method, the power decoupling capability is achieved without any additional components. Furthermore, the grid-tied inductor, which is connected to the output side, is minimized because the discontinuous current mode (DCM) is used for the current control. As a simulation result, the second order harmonic component of the input current is reduced by 90.2% compared to that without power decoupling control. Then, the proposed power decoupling control is confirmed with a T-type NPC inverter as a prototype. Consequently, the second order harmonic component of the input current is reduced by 77.1% compared to that without power decoupling control, whereas the output current THD is 3.13% at 200-W load.

I. Introduction

In recent years, DC micro grid and DC power supply systems have been actively studied [1–7]. However, most of the household electronic equipment still use only AC input voltage. Therefore, the DC-AC converter is needed to be connected as an interface between the DC grid and the AC equipment. When connecting the DC grid to the single-phase AC grid, a power decoupling stage is usually required in the converter. The reason is that the input of the DC-AC converter is the DC power, whereas the output power of the DC-AC converter oscillates at twice the grid frequency. As a result, a power ripple at twice the grid frequency occurs at the DC-link of the DC-AC converter. In order to absorb this power ripple, bulky electrolytic capacitors are generally used for the power decoupling capability. However, the electrolytic capacitor limits the lifetime of the system [8–9].

As an alternative power decoupling method, active power decoupling methods, which use buffer capacitors, inductors, and switching devices in order to eliminate the use of the electrolytic capacitor, have been proposed [10–13]. In general, film capacitors or ceramic capacitors are used as the buffer capacitors, so the converter with a long lifetime is achieved. However, additional components for the power decoupling circuit lead to an increase in circuit volume and weight.

In order to avoid the additional components, the power decoupling method using the T-type NPC inverter is proposed [14]. This method uses only the grid-tied inductor to carry out the control of the grid current to the sinusoidal waveform, and the control of the neutral point current, which helps to achieve the power decoupling method, at the same time. Note that the neutral point current is defined as the current, which flows into the neutral point. In the conventional method, the continuous current mode (CCM) is employed, so the two current controls have an interference with each other. Because the

flexibility of current control decreases, either the output current or the neutral point current is impossible to be controlled. The period which those current are not simultaneously controlled is called “current uncontrollable period” in this paper.

In this paper, the novel active power decoupling method for T-type NPC inverter is proposed in order to eliminate the interference between the decoupling control and the grid current control. In particular, CCM is used instead of DCM to independently control two currents at the same time without additional magnetic component. Furthermore, the grid-tied inductor can be minimized by the use of DCM. The contribution of this paper is that both the elimination of the electrolytic capacitors and the minimization of the system can be achieved simultaneously. This paper is organized as follows; first, the principle of the active power decoupling method is explained, second, the circuit configuration and the conventional active power decoupling control for T-type NPC inverter is explained. Then, the proposed active power decoupling control based on DCM is introduced.

As the simulation result, the current ripple of the input current is reduced by 90.2% compared to that without the power decoupling control, whereas the output current THD is 1.87%.

Finally, as the experimental result, the current ripple of the input current is reduced by 77.1% compared to that without the power decoupling control, whereas the output current THD is 3.13%.

II. Principal of Active Power Decoupling Method

In this chapter, the reason why the power ripple occurs in a DC-AC circuit is explained. The output voltage and the output current of the inverter are respectively presented by

$$v_{out} = \sqrt{2}V_{out}\sin(\omega t) \quad (1),$$

$$i_{out} = \sqrt{2}I_{out}\sin(\omega t) \quad (2),$$

where V_{out} is the RMS value of v_{out}, I_{out} is the RMS value of i_{out}, and ω is the grid angular frequency. Thus, the instantaneous output power is expressed by

$$\begin{aligned} p_{out} &= v_{out}i_{out} = V_{out}I_{out} - V_{out}I_{out}\cos(2\omega t) \\ &= P_{const} + p_{fluct} \end{aligned} \quad (3),$$

where P_{const} is the constant value and p_{fluct} is the fluctuation value. Equation (3) shows that the inverter produces a power ripple at twice the grid frequency whereas the input power is constant.

Figure 1 shows the relationship among the input power, the instantaneous output power, and the buffer power. The DC input power should be constant, whereas the instantaneous output power oscillates at twice the grid frequency. In order to absorb the power ripple, the difference between the instantaneous input power and the instantaneous output power should be compensated by the charge and discharge of the buffer capacitor as shown in Fig. 1(b). The relationship of the compensation power and the charge and discharge energy of the capacitor is given by

$$\Delta E = \frac{1}{2}C\left(V_{\max}{}^2 - V_{\min}{}^2\right) \quad (4),$$

where ΔE is the buffer energy, which is absorbed by the capacitor, C is the capacitance, V_{max} and V_{min} are the maximum and minimum value of the oscillated voltage of the buffer capacitor. As shown in (4), the compensation energy is proportional to the capacitance. In the conventional method, a large electrolytic capacitor is connected between the DC grid and the DC-AC converter in order to absorb the power ripple.

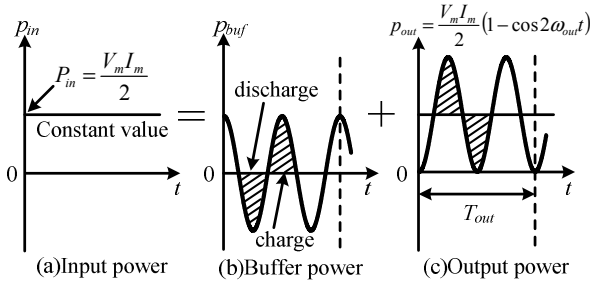


Fig. 1. Single-phase power ripple compensation.

On the other hand, in the active power decoupling circuit, the additional switching devices, inductors, small capacitors are used for the active buffer circuit instead of adopting a bulky electrolytic capacitor in the DC-link [10–13]. The voltage of the buffer capacitor is oscillated by the control of the current on the additional inductor. As a result, the buffer capacitor absorbs the same power ripple with a small capacitance due to the increase of voltage ripple V_{max}^2-V_{min}^2. Thus, a film or ceramic capacitors can be used instead of the electrolytic capacitor to increase the lifetime of the system.

III. Circuit Configuration and Conventional Method

Figure 2 shows the circuit configuration of the single-phase T-type NPC inverter. The T-type NPC inverter is possible to operate in both the directions. In this paper, the power flow from the DC side to the AC side is considered. In the conventional method in [14], the active power decoupling control is achieved by the oscillation of the voltages of two capacitors C_1 and C_2.

Figure 3 shows the waveforms of the DC-link voltage and the two capacitor voltages. The two capacitor voltages V_{C1} and V_{C2} are given by

$$V_{C1} = \frac{V_{dc}}{2} + V_m \sin(\omega t + \delta) \quad (5),$$

$$V_{C2} = \frac{V_{dc}}{2} - V_m \sin(\omega t + \delta) \quad (6),$$

where V_{dc} is the DC-link voltage, V_m is an amplitude of the capacitor voltage, ω is the angular grid frequency, and δ is the phase difference to the output voltage. As shown in Fig. 3 and (5–6), because the power decoupling control is achieved by oscillating the two capacitor voltages in opposite phases, the DC-link voltage is the sum of the two capacitor voltages, which is constant. From (5–6), the capacitor currents i_{C1} and i_{C2} are represented as

$$i_{C1} = C\frac{dV_{C1}}{dt} = C\omega V_m \cos(\omega t + \delta) \quad (7),$$

$$i_{C2} = C\frac{dV_{C2}}{dt} = -C\omega V_m \cos(\omega t + \delta) \quad (8),$$

where C is the capacitance of the buffer capacitor C_1 and C_2. From Kirchhoff's law, neutral point current is represented as

$$i_n = i_{C1} - i_{C2} = 2C\omega V_m \cos(\omega t + \delta) \quad (9),$$

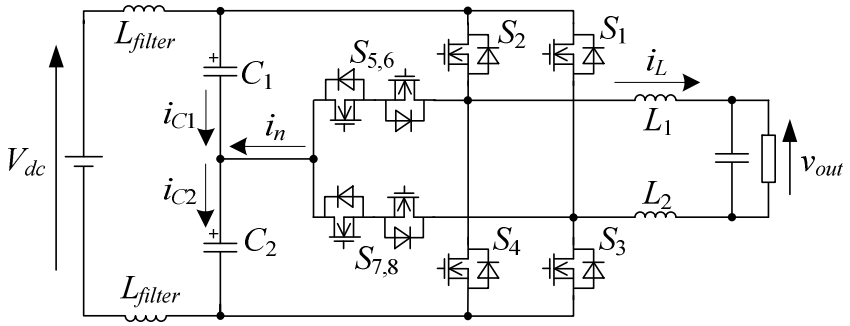


Fig. 2. DC to single-phase AC T-type NPC inverter.

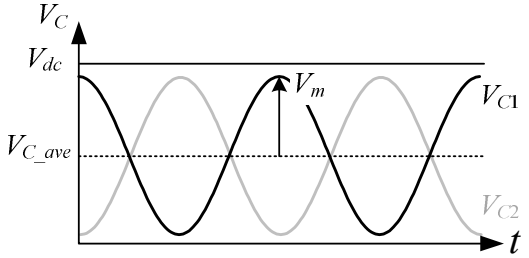


Fig. 3. Waveforms of ideal capacitor voltage and DC-link voltage. The two capacitor voltages oscillate in opposite phases.

From (5–9), capacitor voltages are controlled by flowing neutral point current. In addition, from (5–8), the instantaneous capacitor power is represented as

$$p_C = C\omega V_m^{\,2}\sin(\omega t+\delta)\cos(\omega t+\delta) = \frac{1}{2}C\omega V_m^{\,2}\sin(2\omega t+2\delta) \quad (10).$$

In order to absorb the power ripple, (10) has to be same as p_{fluct} in (3). In (10) and p_{fluct} in (3), the variation is only sinusoidal function term. Thus, the constant value and the variation can be compared respectively. The constant value, which means amplitude, and the variation, which indicates phase, are respectively compared in (11–12)

$$-\cos(2\omega t) = \sin(2\omega t+2\delta) \quad (11)$$

$$V_{out}I_{out} = C\omega V_m^{\,2} \quad (12).$$

From (11), the initial phase difference of neutral point current δ is determined. Furthermore, from (12), the amplitude of the capacitor voltage V_m is determined. Then, V_m is expressed by

$$V_m = \sqrt{\frac{V_{out}I_{out}}{C\omega}} \quad (13).$$

Note that V_m should not exceed the half of V_{dc} because the DC-link voltage is the sum of the two capacitor voltages,

$$V_m \le \frac{V_{dc}}{2} \quad (14).$$

According to (9) and (13), the neutral point current which flows to the neutral point is expressed by

$$i_n = 2\sqrt{V_{out}I_{out}C\omega}\cos\left(\omega t-\frac{\pi}{4}\right) \quad (15).$$

Through the control of the neutral point current, the capacitor voltages are oscillated as (5–6) to absorb the power ripple.

Figure 4 shows the relationship of the absolute value of the current commands between the grid current and the neutral point current. If the single-phase T-type NPC inverter employs with CCM as in the conventional method [14], the neutral point current control and the output current control are interfered with each other during the period where the command value relationship becomes $|i_n^*|>|i_{out}^*|$ as shown in the shaped area in Fig. 4. When the neutral point current flows during that period, the current which is larger than the output current command value, flows to the grid-tied inductor. Thus, the output current is affected by the neutral point current. In the conventional method, only the output current is controlled in the period in order to prevent interference. As a result, the power ripple remains in the DC-link since the neutral point current is different from command value.

IV. Proposed Active Power Decoupling Method

In the proposed method, DCM is employed to the current controls of the single-phase T-type NPC inverter drawn in Fig. 2. In DCM, there is zero-current interval, where the inductor current becomes zero and all the switching devices are turned off. For this reason, the interference of the two current control is solved by flowing each current during the zero-current interval of the other current. In

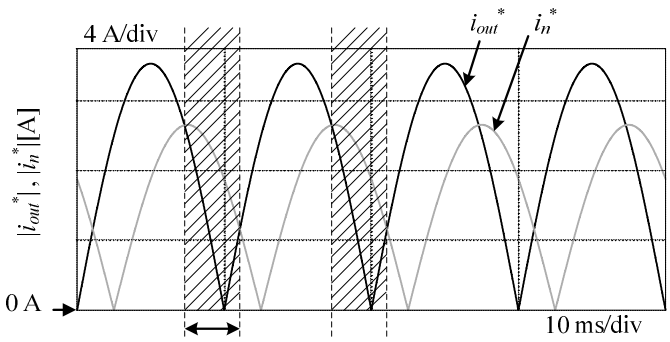


Fig. 4. Absolute current command value of output current and neutral point current. In the shaped area of Fig. 4. The neutral point current control and the output current control are interfered with each other in the conventional CCM method.

particular, the neutral point current flows during the zero-current interval of the grid current and vice versa. If the zero-current interval of each current is designed to be long enough to flow the other current, two currents can be independently controlled at the same time.

Figures 5 and 6 show the current waveform of the neutral point current and the output current of the T-type NPC inverter drawn in Fig. 2 with DCM. As shown in Fig. 5, the neutral point current i_n flows in DCM, resulting in the zero-current interval.

By the control of this neutral point current according to (15), the capacitor voltages oscillate according to (5–6), achieving the power decoupling control. As shown in Fig. 6, the inductor current i_L flows during the zero-current interval of the neutral point current so that the sum of i_L and i_n results in the sinusoidal grid current. Thus, two currents are simultaneously controlled using only grid-tied inductors, leading to the achievement of the power decoupling control and the sinusoidal grid current control at the same time.

Figures 7 and 8 show the switching patterns, which are used for the control of the neutral point current and the output current. The neutral point current is controlled using a grid-tied inductor as shown in Fig. 7(a–d). In addition, the output current is controlled after the neutral point current becomes zero. Note that the output current does not flow through the current path of the neutral point current.

Figure 9 indicates the proposed control block diagram for the T-type NPC inverter with the power decoupling operation. The upper block diagram of Fig. 9 controls the output current and the output voltage. Note that $i_{n\_pol}^*$ is a polarity of the neutral point current which flows to the grid-tied inductor. The lower block diagram of Fig. 9 controls the average voltage of the capacitor and the neutral point current. Therefore, the average voltage of the capacitor is controlled to the half value of the DC-link voltage with the PI controller. Note that the cutoff frequency of the PI controller is configured low to avoid the interference with output voltage PI controller. Meanwhile, the capacitor voltage is oscillated by the feed forward of i_L^*, which follows (7). Then, the duty ratios are calculated from the current commands to generate the switching signals. As these results, the proposed method with DCM achieves a compensation of the remaining power ripple on DC-link and controlling the output current.

Figure 10 (a) shows the relationship between the ideal compared capacitor voltage $V_{C\_large}^*$ and the ideal absolute value of the output voltage $|v_{out}^*|$. Note that the capacitor voltage indicates only the larger voltage of V_{C1} and V_{C2}. Since the circuit is buck type, the $V_{C\_large}^*$ must be higher than $|v_{out}^*|$ during the output period. For this reason, the maximum voltage $|v_{out}^*|$ is $V_{dc}/\sqrt{2}$, the maximum RMS value of v_{out}^* is $V_{dc}/2$. In this paper, the modulation rate is defined as 1.0 when the configured RMS value of v_{out}^* is $V_{dc}/2$.

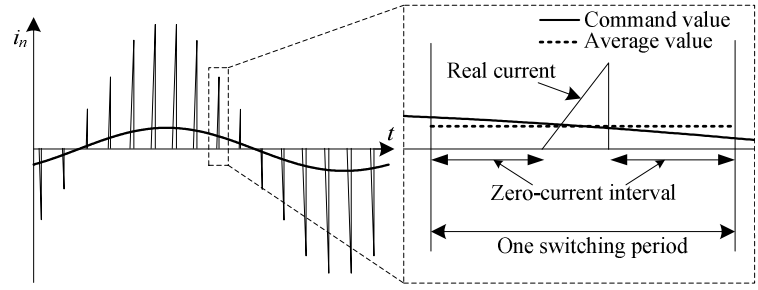


Fig. 5. Waveform of i_n operated in the DCM

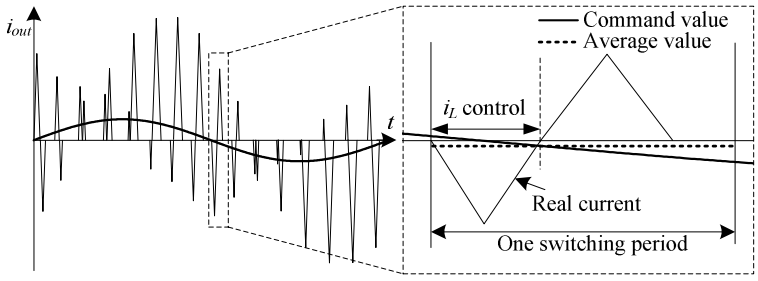
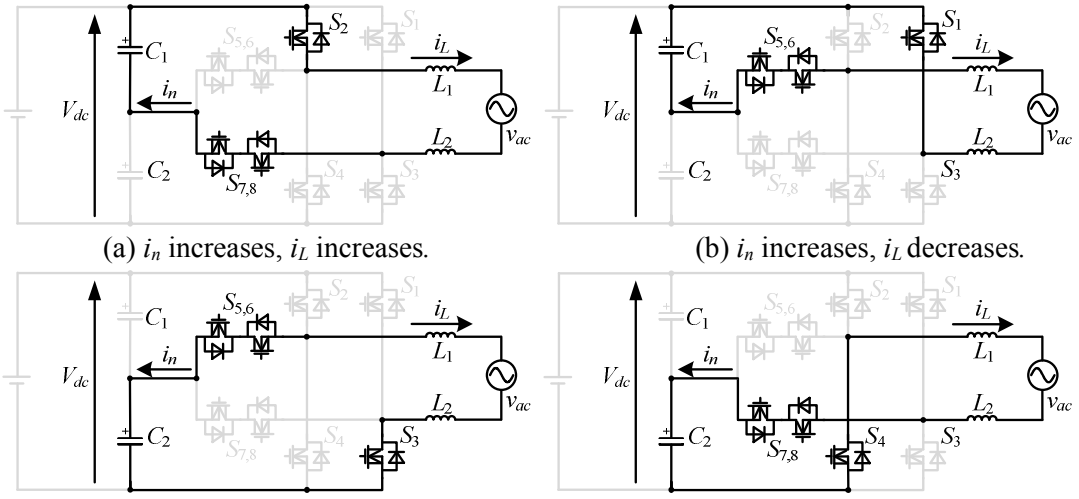


Fig. 6. Waveform of i_L operated in the DCM

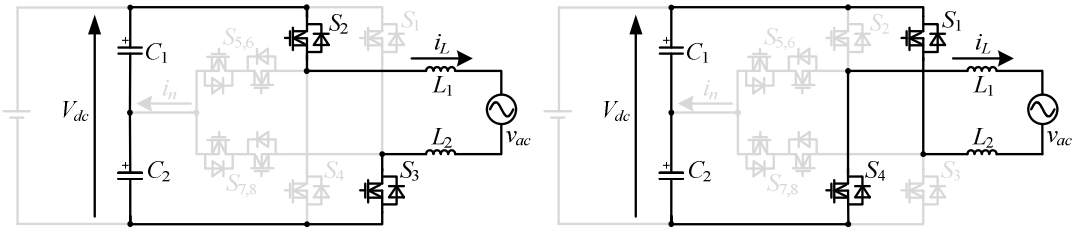
Figure 10 (b) shows the relationship between the ratio of the RMS value of i_n and i_{out} and the modulation rate. Note that C / C_{min} is defined as 100% when the V_m of (13) is V_{dc} / 2. In the proposed method, the sum of the neutral point current i_n and the output current i_{out} flows to the inductor and the switching devices. Thus, the conduction loss increases as i_n increases. As shown in Fig. 10 (b), the ratio, I_{n_rms} / I_{out_rms} decreases as the modulation ratio decreases or C / C_{min} decreases. As a result, the circulating current is low in the applications requiring low modulation ratio and low capacitance.



(a) i_n increases, i_L increases. (b) i_n increases, i_L decreases.

(c) i_n decreases, i_L increases. (d) i_n decreases, i_L decreases.

Fig. 7. Switching patterns of neutral point current i_n control. i_n and i_L are controlled simultaneously.



(a) i_L increases. (b) i_L decreases.

Fig. 8. Switching patterns of output current i_L control. Only i_L flows by using those switching patterns whereas i_n is zero.

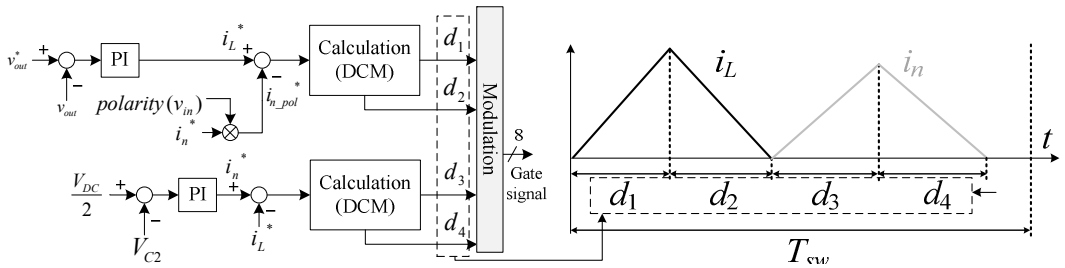
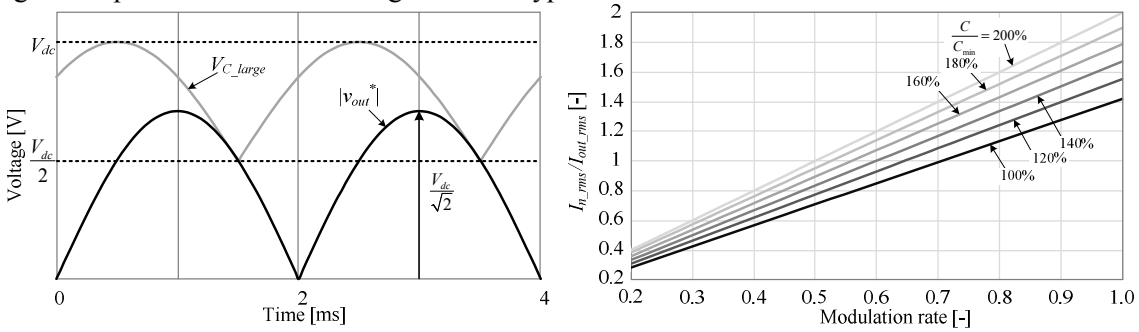


Fig. 9. Proposed control block diagram for T-type NPC inverter.



(a) Relation of V_{C_large} and $|v_{out}^*|$ (b) Relation of current ratio and modulation rate

Fig. 10. Relation of voltages, current ratio and modulation rate.

V. Simulation Results

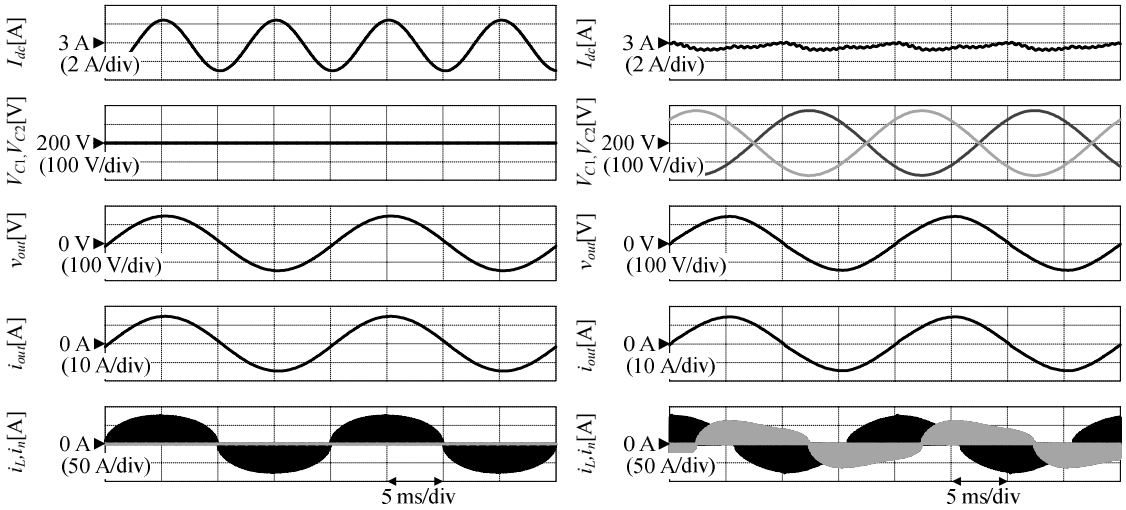
Table I shows the simulation conditions, whereas Fig. 11(a) and (b) show the waveforms of the input current, the capacitor voltages, the output voltage, the output current without/with the proposed power decoupling capability respectively.

As shown in Fig. 11(a), the input current oscillates at twice the grid frequency because the use of the small capacitance of C leads to the high current ripple on DC-link according to (3). On the other hand, as shown in Fig. 11(b), the current ripple of the input current is reduced significantly compared to that in Fig. 11(a) because the capacitor voltages V_{C1}, V_{C2} oscillate to absorb the power ripple in the proposed power decoupling method.

Figure 12 shows the harmonic analysis of the input current. By the proposed method, the component of 100 Hz, i.e., twice the grid frequency is reduced by 90.2% compared to that result without the power decoupling method whereas the THD of the output current is 1.87%.

Table I: Simulation parameters

Parameter	Symbol	Value
Rated power	P_{out}	1 kW
Output voltage	v_{ac}	100 V
Output frequency	f_{out}	50 Hz
DC link voltage	V_{dc}	400 V
Capacitor	C_1,C_2	120 μF
Inductor	L_1,L_2	25 μH



(a) Operation without power decoupling control. (b) Operation with power decoupling control.

Fig. 11. Waveforms of input current, capacitor voltages, output voltage and output current.in steady state.

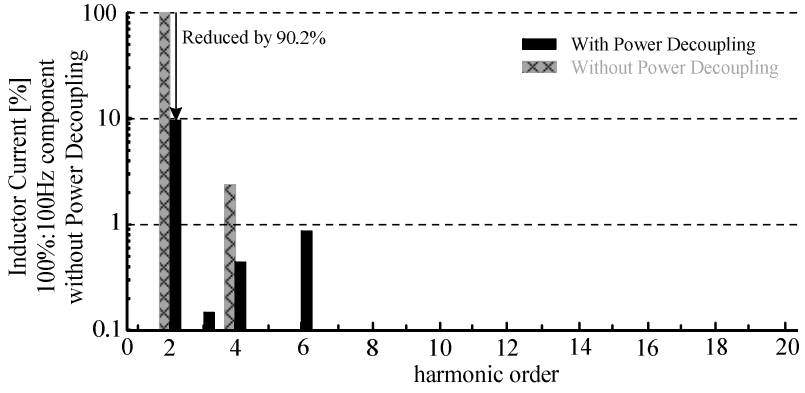


Fig. 12. Harmonic component of input current.

VI. Experimental Results

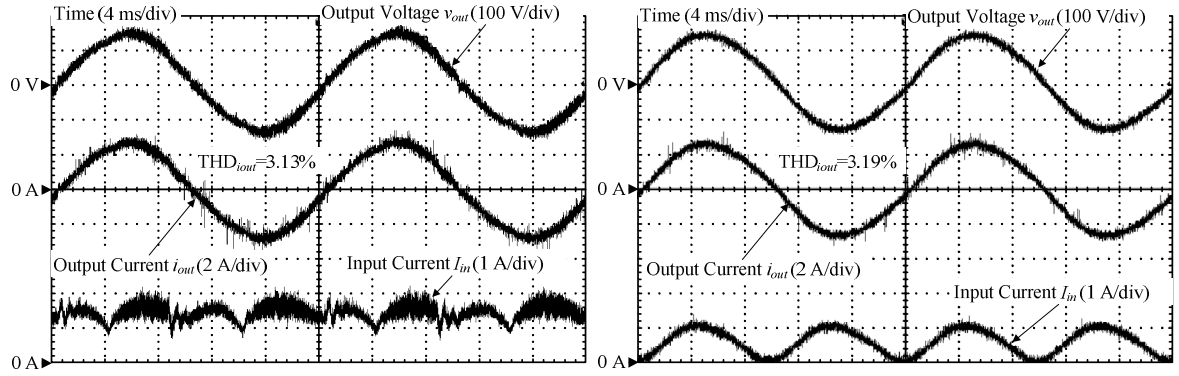
Table II shows the experimental parameters. The experiments have been done with an open-loop. In general, percent impedance $\%Z_L$ of grid-tied inductor is designed around 5%. However, as shown in Table II, the grid-tied inductor of the prototype is 50μH (the two inductors 25μH are connected in series). Hence, the $\%Z_L$ is 0.16%. Furthermore, the additional inductor which is required for conventional power decoupling control is not needed.

Figure 13 (a) and (b) show the waveforms of the output voltage, the output current, and the input current with/without the proposed power decoupling method at 200-W load respectively. From Fig. 13 (a), the output voltage is controlled in sinusoidal waveform at 50 Hz whereas the input current is compensated by the proposed method. The THD of the output current is 3.13%.

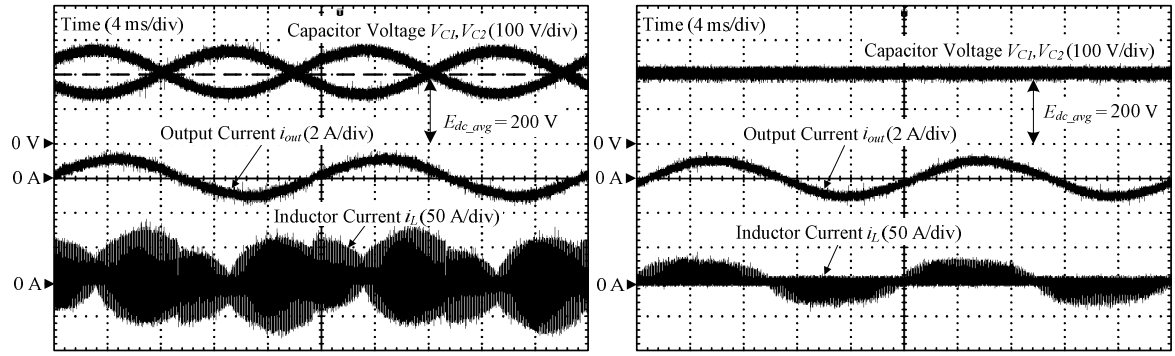
Figure 14 (a) and (b) show the waveforms of the two capacitor voltages, the output current, and the inductor current (DCM current) with/without the proposed power decoupling method at 200-W load respectively. Note that the output current is republished to confirm the phase relationship between

Table II: System parameters

Parameter	Symbol	Value
Output power	P_{out}	200 W
Output voltage	v_{ac}	100 V
Output frequency	f_{out}	50 Hz
DC link voltage	V_{dc}	400 V
Capacitor	C_1, C_2	166 μF
Inductor	L_1, L_2	25 μH



(a)Operation waveforms (w/ power decoupling) (b)Operation waveforms (w/o power decoupling)
Fig. 13. Measured output voltage, output current and input current. Due to the proposed DCM current control method, the power decoupling control is achieved whereas the output current THD is 3.13% at 200W load.



(a)Operation waveforms (w/ power decoupling) (b)Operation waveforms (w/o power decoupling)
Fig. 14. Measured capacitor voltage, output current and inductor current. Due to the proposed DCM current control method, the two capacitor voltages are fluctuated in opposite phases.

fluctuated two capacitor voltages and the output current.

From Fig. 14 (a), the two capacitor voltages are fluctuated in opposite phase by controlling neutral point current. From (2) and (5), the theoretical phase difference between the fluctuation component of capacitor voltage and the output current is $\pi/4$. However, the real phase difference is smaller than the theoretical phase difference. The reason is that the increases of the power loss due to the circulation current by applying the power decoupling control. In the theoretical consideration, the power loss of the capacitor and the inductor is assumed as zero. However, the power loss cannot be ignored in the experiment. Thus, the conditions of the neutral point current command is changed.

Figure 15 shows the enlarged view of the inductor current. From Fig. 15, the output current and the neutral point current are controlled simultaneously in one switching period.

Figure 16 shows the harmonic analysis of the input current. By applying the proposed method, the component of 100 Hz, i.e., twice the grid frequency is reduced by 77.1% compared to that result without the power decoupling control.

Figure 17 shows the fluctuated capacitor voltages and the relationship of the current command values $|i_n^*|$ and $|i_{out}^*|$. As shown in Fig. 4, the power decoupling control cannot be applied when $|i_n^*|$ is higher than $|i_{out}^*|$ in the conventional method. Because of the current uncotrollable period, the two capacitor voltages are distrorted. However, from Fig. 17. the fluctuation conponents of the capacitor voltage are

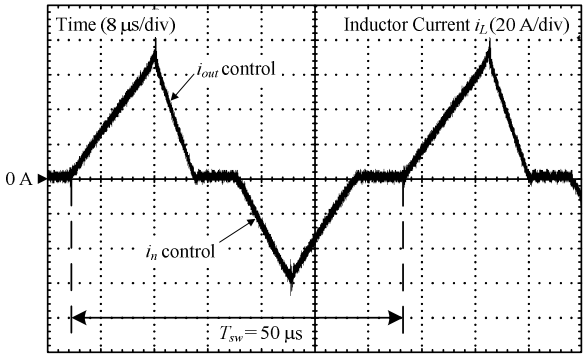


Fig. 15. Measured enlarged view of inductor current. Output current and neutral point current are controlled simultaneously in one switching period.

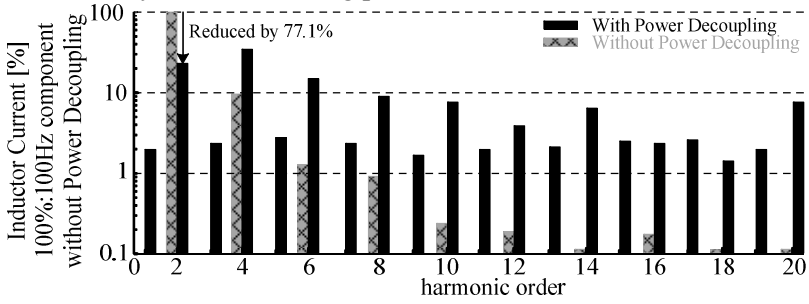


Fig. 16. Harmonic component of input current.

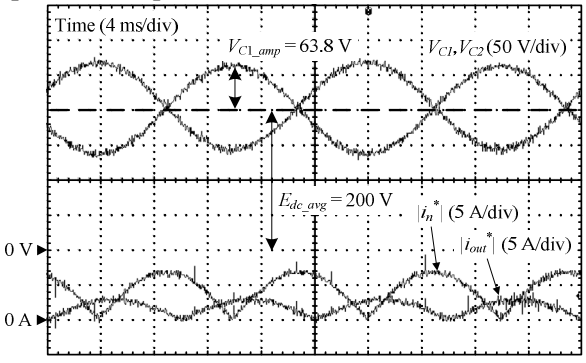


Fig. 17. Measured capacitor voltages and absolute value of current commands. Power decoupling control is achieved when $|i_n^*|$ is higher than $|i_{out}^*|$

controlled in sinusoidal waveform when $|i_n^*|$ is higher than $|i_{out}^*|$, i.e., the proposed power decoupling method can be applied in all time.

From (13) and Table II, the ideal amplitude of the two capacitor voltages is calculated as 61.9 V. From Fig. 17, the amplitude of the two capacitors is mesured as 63.8 V. Note that the amplitude is calculated by half of peak to peak of the capacitor voltage. The Error rate of the capacitor voltage amplitude is 3.08%. Thus, the proposed control method is employed correctly.

VII. Conclusion

This paper proposed the power decoupling method based on DCM for T-type NPC inverter without any additional passive components. The proposed control method achieved the low ripple current at the DC-link and the low grid current THD. Thus, the reduction of the system size and the long lifetime are expected from the proposed method. In particular, the current ripple of the input current at twice the grid frequency is reduced by 90.2%. Moreover, the output current THD is 1.87%.

In the proposed method, the ratio of the neutral point current to the output current decreases with the decrease of the modulation rate and DC-link capacitor. Therefore, the circulating current is low in the case of applications requiring low modulation rate and low capacitance.

As the experimental result, the two capacitor voltages are fluctuated by flowing the neutral point current. The output voltage and power decoupling control are achieved without additional component. As a result, the second harmonics component of the input current is reduced by 77.1% compared to that result without the power decoupling control whereas the THD of output current is 3.13%.

In the future work, applying feed-back control, operation at rated load 1-kW, and formulation of the neutral point current command which include the influence of the power loss due to the circulation current will be considered in order to improve the efficiency.

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