ZVRT Capability of Single-phase Grid-connected Inverter with High-speed Gate-block and Minimized LCL Filter Design

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***Abstract* -- This paper proposes a Zero-Voltage Ride-Through (ZVRT) method and an LCL filter design method to meet the Fault Ride-Through (FRT) requirements for a single-phase grid-connected inverter with a minimized LCL filter. A high inverter-output-current overshoot occurs at a grid voltage sag and a grid voltage recovery, when a low-inductance LCL filter design is employed in order to minimize the filter volume. In order to suppress the current overshoot, a high-speed gate-block operation and the design method of the minimized LCL filter are proposed. In particular, the filter design considers the delay time in the gate-block operation in order to clarify the reduction limitation of the inductance in the LCL filter. As a result, the maximum inverter-output-current overshoot is suppressed to 146% by the high-speed gate-block operation and the designed LCL filter, where the impedances of an interconnected inductor and a filter inductor are 1.0% and 0.78% of the inverter normalized impedance, respectively. Therefore, it is possible to meet the FRT requirements with the proposed ZVRT method even with the minimized LCL filter.**

***Index Terms*—Grid-connected inverter, Zero-voltage ride-through, Minimized LCL filter, High-speed gate-block, Output current overshoot**

I. INTRODUCTION

In recent years, grid-connected inverters in photovoltaic, fuel cell, and wind turbine systems, have been actively studied for energy saving [1]-[3]. The grid-connected inverter is required to meet the Fault-Ride-Through (FRT) requirements of the grid code [4]-[9]. During a grid fault such as a short circuit occurs, the inverter has to continue to flow the current into the grid in order to assist the recovery of the grid. Moreover, at the grid voltage recovery, the fluctuation of the grid voltage might cause the current overshoot. In order to prevent the overcurrent flowing to the grid and load, the transitional maximum inverter output current is required to less than 150%, if the rated inverter output current peak value is considered as 100% [10]. Generally, high-inductance filters, e.g. L or LC filters, can simply meet the FRT requirements. For instance, the interconnected inductor impedance is designed at 2.1% of the inverter impedance to carry out the FRT operation in [4]. However, such high-inductance filters lead to a large filter volume.

The inverter is desired to have a small volume to increase power density [11]-[12]. In particular, the interconnected inductor that occupies a majority of the inverter size is highly demanded to reduce the size. By reducing the inductance, it is possible to reduce the volume of the inductor. A high switching frequency with SiC or GaN devices is applied in the term of a same current ripple in order to reduce the inductance of the interconnected inductor. Moreover, in order to effectively reduce the current ripple components of the inverter output current, the grid-side inductor is employed in order to form the LCL filter which has a high attenuation rate [13]-[14].

Figure 1 shows a circuit configuration of a single-phase grid-connected inverter with an LCL filter, where L_1 is the interconnected inductor, L_f is the filter inductor, C_f is the filter capacitor, S1 to S4 are switching devices, and v_{conv} is the inverter output voltage. In this paper, an H-bridge single-phase two-level inverter is employed due to its simplicity. The inverter output current overshoot significantly increases due to the high grid voltage fluctuation at grid short-circuit faults when the inductance of the filter is reduced with the LCL filter design; consequently, the inverter is stopped by the over current protection and disconnected from the grid. Therefore, if the inductance is reduced by increasing the switching frequency when considering only the suppression for the output current harmonics in the grid code, it is impossible to suppress the inverter output current overshoot due to the low inductance, i.e. the violation of the FRT requirements.

In [4], the FRT operation with the constant peak current strategy has been demonstrated in the experiment; however, the method of [4] does not consider the Zero-Voltage Ride-Through (ZVRT) operation and the low-inductance filter. In

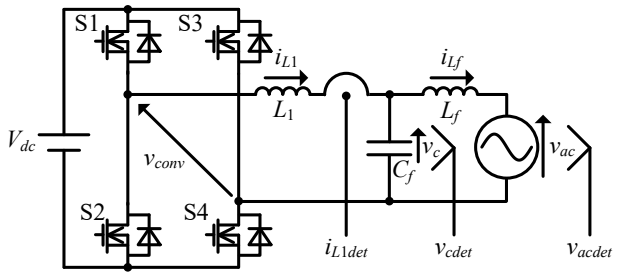


Fig. 1. Single phase inverter circuit with LCL filter. The interconnected inductor L_1 and the filter inductor L_f are reduced by increasing the switching frequency.

[6], the FRT operation with the voltage amplitude and the output power control has been proposed. Nevertheless, this method introduces a long delay time for the control. Thus, the high inverter-output-current overshoot occurs with the low-inductance filter. In [9], the FRT operation with the peak value control method has been proposed to detect the voltage fault. In particular, the detection value of the grid voltage is used to suppress the current overshoot. However, the high inverter-output-current overshoot still occurs due to the long delay time of the computation. In [15], the ZVRT operation for minimized LC filter with a momentary high-speed gate-block method is proposed. The gate-block operation is carried out when the inverter output current reaches a current threshold. However, the ZVRT operation has been not considered for the minimized LCL filter. Thus, it is necessary to achieve the ZVRT operation with the minimized LCL filter.

In this paper, the ZVRT operation method meeting the FRT requirements is proposed with a high-speed gate-block operation and a design method of the LCL filter. Moreover, the suppression of the maximum inverter output current overshoot at the voltage sag is aimed to less than 150%, if the rated inverter output current peak value is considered as 100%, in order to meet the FRT requirements. In [16], the ZVRT operation with the minimized LCL filter is demonstrated when the voltage drop and recovery occur at the voltage phase of 90 degree. In this paper, additional experimental results with a Low-Voltage Ride-Through (LVRT) operation and when the voltage drop and recovery occur at different voltage phase are demonstrated. The original idea of this paper is follow; the high-speed gate-block operation that is reduced the detection and the control delay time is applied with the minimized LCL filter to suppress the inverter output current overshoot. The gate-block operation is carried out when the grid voltage fluctuation such as voltage drop or recovery is detected. In addition, in order to suppress the output current overshoot and meet the FRT requirements, it is necessary to design the LCL filter considering the delay time of the grid fault detection. The LCL filter is designed by deriving the equation of the inverter output current at the grid voltage recovery with the gate-block operation. This ensures that the inverter output current overshoot which includes the resonance current of the grid-side LC filter is less than 150% of the rated output current peak at the voltage recovery. The ZVRT operation meeting FRT requirements is demonstrated with a 1-kW prototype.

II. Zero-voltage Ride-through Method for Minimized-LCL-Filter Grid-Connected Inverter

A. Conventional FRT Method

In order to minimize the LCL filter, the inductance and capacitance are reduced by increasing the switching frequency of the inverter. Due to the reduction of the inductance in the LCL filter, the high inverter-output-current overshoot occurs at the grid voltage drop and recovery.

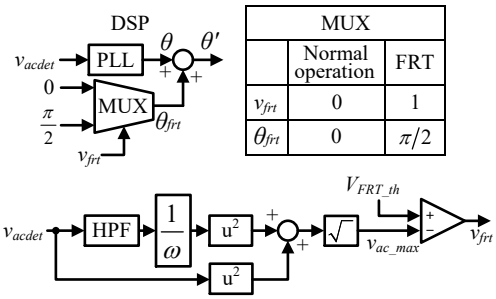


Fig. 2. Reactive current control method for FRT operation. When voltage sag occurs, the phase θ' is advanced by $\pi/2$ from θ.

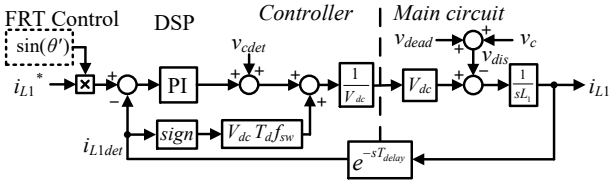


Fig. 3. Control block diagram of conventional FRT operation. In the conventional method, the current controller is implemented by DSP.

Consequently, the grid-connected inverter is stopped by the over current protection, and cannot continue the operation with the reduced inductance.

Figure 2 shows a reactive current control method for an FRT operation. The grid voltage phase θ is locked by phase-locked-loop (PLL) based on the grid voltage detection value v_{acdet}. During the voltage sag, the voltage sag detection signal v_{frt} becomes one, and the inverter output current command phase θ' is the sum of the present grid voltage phase θ and $\pi/2$. The reactive current control is achieved by generating a current command value with the current phase θ'. Note that the voltage sag is detected by the detection of the grid voltage maximum value v_{ac_max}. After that, the grid voltage peak threshold for the reactive current control V_{FRT_th} is compared with v_{ac_max}; when v_{ac_max} is dropped to less than V_{FRT_th}, the reactive current command is generated. Note that HPF stands for the high pass filter, and ω is the grid angler frequency.

Figure 3 shows the control block diagram of the conventional FRT operation where i_{L1}^* is the interconnected inductor current command, v_{cdet} is the filter capacitor voltage detection value, V_{dc} is the input DC voltage, T_d is the dead-time period, i_{L1det} is the interconnected-inductor current detection value, f_{sw} is the switching frequency and T_{delay} is the delay time of the inductor current detection, v_{dead} is the dead-time error voltage, v_c is the filter capacitor voltage, v_{dis} is the disturbance voltage, i_{L1} is the interconnected inductor current. The current controller is implemented by digital signal processor (DSP). Moreover, a dead-time error voltage of the inverter output is compensated by using the dead-time error voltage feedforward compensation at a steady-state operation. The grid current is distorted by the grid disturbance due to the increasing disturbance gain, when the inductance of the interconnected inductor becomes low. This also leads to the

greatly increase in the inverter output current overshoot at the voltage sag.

Figure 4 shows the control block diagram of the conventional FRT operation with a disturbance observer (DOB) [17]-[23]. DOB is implemented by digital hardware in field-programmable gate array (FPGA) to construct a high-gain DOB. Thus, the disturbances such as dead time error voltage and voltage drop of switching devices are compensated at high speed. The disturbance voltage $\hat{v}_{dis}$ is estimated from the inter-connected-inductor current i_{L1} and the output of the PI controller v_L^* as

$$\hat{v}_{dis} = \frac{\omega_c}{\omega_c + s} v_L^* - \frac{s\omega_c L_1}{\omega_c + s} i_{L1det} \quad (1),$$

where ω_c is the cutoff angular frequency of DOB, and s is the Laplace operator. Moreover, the current controller is added with the detected voltage of the filter capacitor v_{cdet} for a voltage-feedforward compensation. Consequently, the dead-time voltage error is compensated by the high-gain DOB, whereas the grid voltage is compensated by the voltage feedforward. However, the overshoot of the inverter output current becomes significantly fast at the grid voltage drop and recovery with the low-inductance LCL filter. The disturbance compensation with the voltage feedforward and the high-gain DOB cannot detect the grid fault immediately due to the delay time of the detection and the sampling; consequently, when the short grid failure occurs, the maximum inverter output current overshoot of higher than 150% occurs with the minimized LCL filter. Therefore, the high-speed current-overshoot suppression is necessary in order to suppress the overshoot of the inverter output current i_{Lf} at the grid faults.

B. Proposed ZVRT Method

Figure 5 shows the control block diagram of the high-speed gate-block operation with the high-gain DOB for the ZVRT operation. In order to suppress the inverter output current overshoot, the gate-block operation is carried out by the detection of the grid voltage fluctuation. By filtering the grid voltage with a voltage-sag detection circuit, the gate-block signal OC_L is generated by the gate-block signal generator. After that, the gate-block operation is carried out at the grid voltage drop or the voltage recovery. By using the gate-block operation, the ZVRT operation is achieved. Furthermore, in order to achieve the ZVRT operation at high speed response, the gate-block control is implemented by digital hardware in FPGA, whereas the voltage-sag detection is constructed by analog circuit. Therefore, the detection delay time of the gate-block operation is minimized, i.e. one of the main factors to reduce the overshoot. In addition, the proposed method is implemented with the high-gain DOB as in Fig. 4 in order to reduce the inverter output current distortion with the low inductance of the interconnected inductor [23]. The reason is because the effect of the dead-time error voltage significantly increases due to the decrease

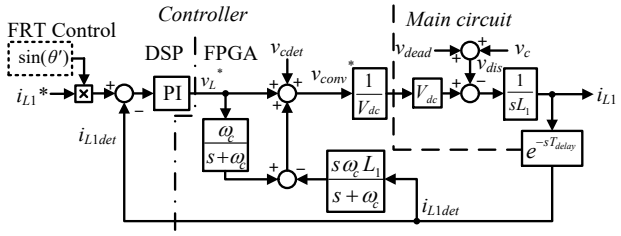


Fig. 4. Control block diagram of conventional FRT operation with DOB. In this method, DOB is implemented by FPGA to compensate wideband disturbances.

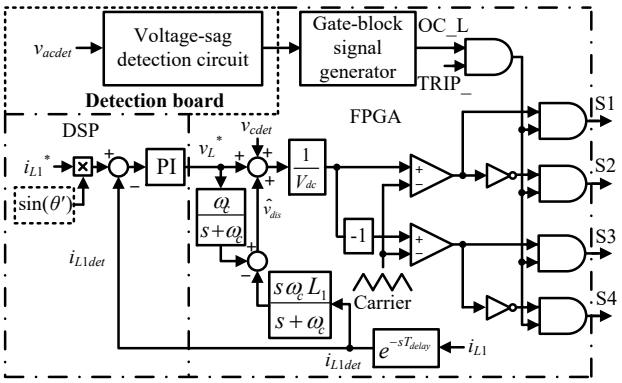
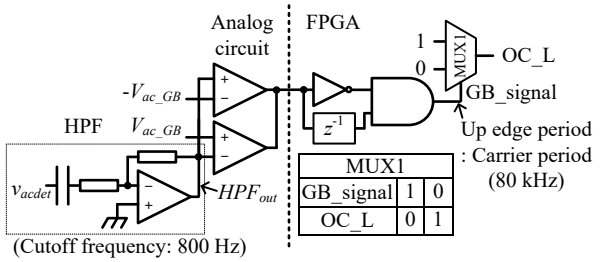


Fig. 5. Control block diagram of ZVRT operation with high-speed gate-block operation. By using the gate-block operation, the inverter output current overshoot is suppressed at the grid voltage drop and recovery.



MUX1		
GB_signal	1	0
OC_L	0	1

Fig. 6. Block diagram of voltage-sag detection circuit and gate-block signal generator. In order to detect the voltage sag, the HPF is implemented in the analog circuit.

of the disturbance suppression performance with the low inductance.

C. High-speed Gate-block Operation

Figure 6 shows the construction of the voltage-sag detection circuit and the gate-block signal generator, where HPF_{out} is the output of HPF, V_{ac_GB} is the gate block threshold. In the high-speed gate-block operation that is applied to the proposed method, it is necessary to generate the gate-block signal to carry out the gate-block operation at the detection time of the grid voltage drop and recovery. The output of the high-pass filter (HPF), which filters the grid voltage, overshoots at the grid voltage drop and recovery. The HPF cutoff frequency is designed to be higher than the grid frequency, in order to operate HPF as a differentiator at the voltage sag. In particular, the HPF cutoff frequency is designed to approximately 800 Hz in this paper. Moreover,

the grid fault signal is generated by comparing the HPF output overshoot HPF_{out} and the gate-block threshold V_{ac_GB}. At the comparison step between the HPF output and the gate-block threshold V_{ac_GB}, the comparator output is low when the HPF output exceeds the threshold V_{ac_GB}. The threshold V_{ac_GB} is determined so that the gate-block operation is not carried out in the normal operation as following simple consideration. In the normal operation, the HPF output becomes the maximum at the zero-crossing points of the grid voltage. Meanwhile, the HPF output at the grid voltage drop and recovery greatly exceed the HPF output during the normal operation. Thus, the threshold V_{ac_GB} is set higher than the HPF output at the zero-crossing points of the grid voltage. In this paper, the threshold V_{ac_GB} is set to 5 times of the HPF output at the zero-crossing points of the grid voltage. Furthermore, the gate-block period is same as carrier period. Therefore, it is possible to continue the inverter output by the momentary gate-block operation. After that, the gate-block signal OC_L is input to AND circuit.

Figure 7 shows the simulation result of the voltage-sag detection and the gate-block signal generation at the grid voltage drop and recovery. The HPF output overshoots at the grid voltage drop and recovery. After that, the gate-block signal is generated when the HPF output overshoots. Thus, the gate-block operation for the ZVRT operation is carried out by the proposed control.

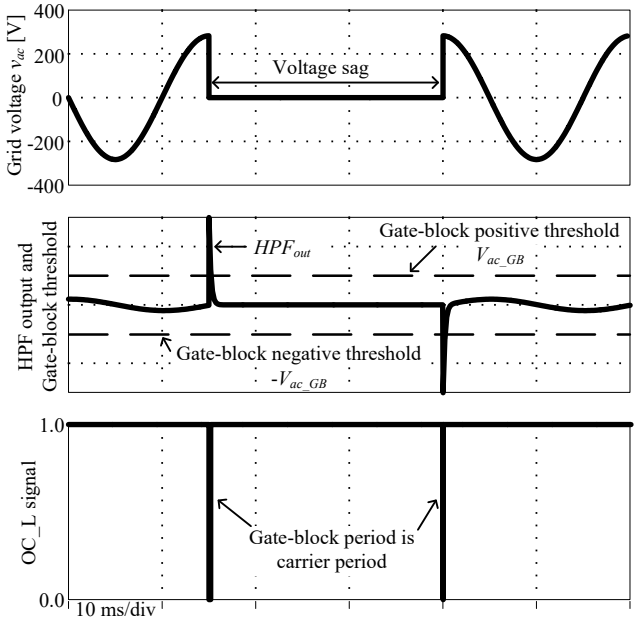


Fig. 7. Voltage-sag detection and gate-block signal generation during voltage sag. The gate-block signal is generated at the grid voltage drop and recovery.

III. Optimal Design of Minimized LCL Filter

A. Derivation of Output Current at Grid Voltage Recovery

A current resonance occurs in the grid-side LC filter when a grid voltage sag occurs. The inverter output current overshoots due to the combination of the resonance current and the steady-state current. The ability of the gate-block operation in H-bridge inverter to suppress resonances in the grid-side LC filter depends on the LCL filter design. Thus, it is necessary to design the parameters of the LCL filter with the grid-side LC filter resonance to meet the FRT requirements. The equation of the inverter output current at the voltage recovery is derived to design the LCL filter.

Figure 8 shows the transient phenomenon of the inverter output current with the LCL filter at the grid voltage recovery. Area (i) of Fig. 8 shows the time from the voltage recovery to when the gate-block operation is carried out ($0 \le t \le t_{bd}$). Area (ii) shows the time after the gate-block operation ($t \ge t_{bd}$). Note that t_{bd} is the delay time from the voltage sag to when the gate-block operation is carried out. In the area (i), the delay time t_{bd} is the sum of the delay time of the gate-block operation such as the detection delay time of the analog circuit and the control delay time of the gate-block operation in the FPGA. The inverter-output-current maximum value $i_{Lf\_\max}$ and the time reaching the maximum current $t_{i\max}$ are calculated in area (ii). In addition, the LCL filter is designed in order that the inverter output current maximum value is less than the maximum inverter output current overshoot of 150% i_{th}.

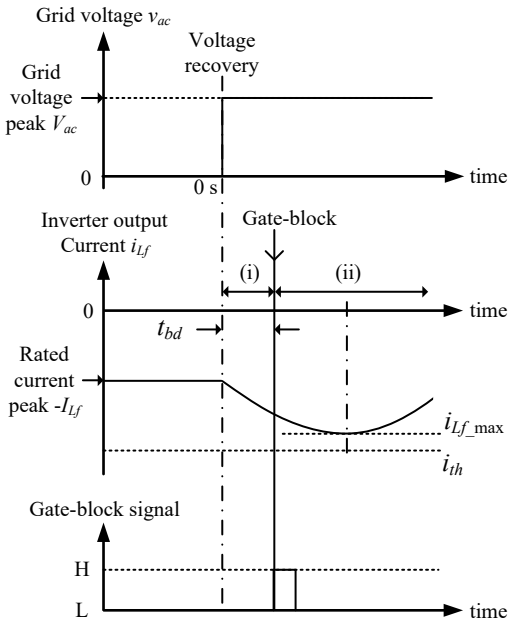


Fig. 8. Transient phenomenon of inverter output current i_{Lf} with LCL filter during voltage recovery. The LCL filter has to be designed in order that the maximum current $i_{Lf\_\max}$ is less than the limitation i_{th} of the current overshoot according to FRT requirements.

Figure 9 shows the circuit model with the LCL filter after the gate-block operation ($t \ge t_{bd}$) in the area (ii) of Fig. 8. The equation of the inverter output current during the transient interval is derived by considering the LCL filter circuit from the viewpoints of the inverter and the grid separately. After the gate-block operation, the inverter output voltage V_{conv} is applied to the inverter-side LC filter to inject the current of

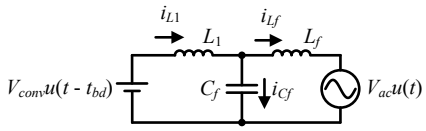


Fig. 9. Circuit model with LCL filter after gate-block operation. The transient phenomenon of Inverter output voltage and grid voltage are considered.

the reverse vector to the inverter output current. The inverter output voltage equals to the input DC voltage V_{dc}. When considering the inverter output side, the rated inverter output current peak $-I_{Lf}$ flows until the gate-block operation is carried out. Thus, the positive inverter output voltage V_{conv} is applied after the gate-block operation to flow the current with the positive direction. In Fig. 9, the circuit equations are derived as shown in (2)-(4)

$$\frac{V_{conv}}{s}e^{-st_{bd}} = sL_1 I_{L1}(s) + sL_f I_{Lf}(s) + \frac{V_{ac}}{s} \tag{2}$$

$$\frac{I_{Cf}(s)}{sC_f} = sL_f I_{Lf}(s) + \frac{V_{ac}}{s} \tag{3}$$

$$I_{L1}(s) = I_{Lf}(s) + I_{Cf}(s) \tag{4},$$

where $I_{L1}(s)$ is Laplace transform of the interconnected inductor current i_{L1}, $I_{Lf}(s)$ is Laplace transform of the filter inductor current i_{Lf}, $I_{cf}(s)$ is Laplace transform of the filter capacitor current i_{cf}, and V_{ac} is the grid voltage peak. By using (2)-(4) and the rated inverter output current peak I_{Lf}, the filter inductor current i_{Lf} is expressed as

$$\begin{aligned} i_{Lf} &= -I_{Lf} + \frac{V_{conv}(t-t_{bd}) - V_{ac}t}{L_1 + L_f} \\ &\quad - \frac{1}{L_1 + L_f}\sqrt{\frac{L_1 C_f L_f}{L_1 + L_f}}\left\{\frac{L_1}{L_f}V_{ac}\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}t\right)\right. \\ &\quad \left. + V_{conv}\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}(t - t_{bd})\right)\right\} \end{aligned} \tag{5}.$$

It is obvious that the timing of the voltage recovery in the short grid failure is unknown. Thus, by considering the grid voltage phase at the voltage recovery ϕ_v and the inverter output current phase ϕ_i, (5) is converted to (6)

$$\begin{aligned} i_{Lf} &= I_{Lf}\sin(\omega t + \phi_i) \\ &\quad - \frac{sign\left(\sin(\omega t + \phi_i)\right)V_{conv}(t - t_{bd}) + V_{ac}\sin(\omega t + \phi_v)t}{L_1 + L_f} \\ &\quad - \frac{1}{L_1 + L_f}\sqrt{\frac{L_1 C_f L_f}{L_1 + L_f}}\left\{\frac{L_1}{L_f}V_{ac}\sin(\omega t + \phi_v)\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}t\right)\right., \\ &\quad \left. - sign\left(\sin(\omega t + \phi_i)\right)V_{conv}\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}(t - t_{bd})\right)\right\} \end{aligned}$$

$$sign(x) = \begin{cases} 1 & (x > 0) \\ 0 & (x = 0) \\ -1 & (x < 0) \end{cases} \tag{6}.$$

Where ω is the angular frequency of the grid. The worst case at the voltage recovery is when the output current reaches the negative peak and the grid voltage returns to the positive peak. Therefore, the minimized LCL filter is designed from (5). In order to design the LCL filter meeting the inverter output current overshoot less than 150%, the period until the inverter output current reaches maximum entitled $t_{i\max}$ as shown in Fig. 8 is derived as follows. First, considering (7) as the filter inductor resonance voltage component $v_{Lf\_res}(t)$,

$$\begin{aligned} v_{Lf\_res}(t) &= \frac{L_1}{L_f}V_{ac}\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}t\right) \\ &\quad + V_{conv}\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}(t - t_{bd})\right) \end{aligned} \tag{7}.$$

When the differentiate equation for (7) becomes zero, the time reaching the maximum inverter output current $t_{i\max}$ is derived as

$$\begin{aligned} t_{i\max} &\approx \frac{t_{bd}}{\left(\frac{L_1}{L_f}\frac{V_{ac}}{V_{conv}} + 1\right)} \\ &\quad + \frac{\sqrt{\left(\frac{L_1}{L_f}\frac{V_{ac}}{V_{conv}} + 1\right)\left(\frac{2L_1 C_f L_f}{L_1 + L_f} + \frac{2{L_1}^2 C_f}{L_1 + L_f}\frac{V_{ac}}{V_{conv}}\right) - \frac{L_1}{L_f}\frac{V_{ac}}{V_{conv}}{t_{bd}}^2}}{\left(\frac{L_1}{L_f}\frac{V_{ac}}{V_{conv}} + 1\right)} \end{aligned}$$

(8),

where the approximation of $\sin(x) \approx x - x^3/6$ is applied to (7) to derive (8). By substituting $t_{i\max}$ in (8) to t in (5), the

maximum inverter output current after the gate-block operation $i_{Lf\_\max}$ is derived. Moreover, it is possible to meet the requirements with any damping resistor, when the LCL filter without the damping resistor is designed to meet the requirements. Thus, the consideration of the over-current suppression with a damping resistor is omitted in this paper. In addition, the maximum inverter output current at the voltage drop is also derived by the circuit model of Fig. 9. The maximum inverter output current at the voltage drop $i_{Lf\_\max\_dp}$ is expressed as

$$i_{Lf\_\max\_dp} = I_{Lf} + \frac{V_{conv}(2t_{bd} - t_{i\max\_dp})}{L_1 + L_f} + \frac{1}{L_1 + L_f}\sqrt{\frac{L_1 C_f L_f}{L_1 + L_f}}\left\{2V_{conv}\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}\left(t_{i\max\_dp} - t_{bd}\right)\right) + \left(\frac{L_1 + L_f}{L_f}V_{ac} - V_{conv}\right)\sin\left(\sqrt{\frac{L_1 + L_f}{L_1 C_f L_f}}t_{i\max\_dp}\right)\right\} \quad (9),$$

where $t_{i\max\_dp}$ is the duration from the voltage drop to when the output current reaches the maximum value. Note that (9) is considered under the condition that the voltage drop occurs at the grid voltage peak as a worst case of the inverter output current overshoot. Moreover, $t_{i\max\_dp}$ is derived as

$$t_{i\max\_dp} \approx \frac{t_{bd}}{\frac{1}{2}\left(\frac{L_1 + L_f}{L_f}\frac{V_{ac}}{V_{conv}} + 1\right)} + \frac{\sqrt{{t_{bd}}^2 + \frac{1}{2}\left(\frac{L_1 + L_f}{L_f}\frac{V_{ac}}{V_{conv}} + 1\right)\left(\frac{L_1 C_f V_{ac}}{V_{conv}} - {t_{bd}}^2\right)}}{\frac{1}{2}\left(\frac{L_1 + L_f}{L_f}\frac{V_{ac}}{V_{conv}} + 1\right)} \quad (10).$$

B. Flowchart of LCL filter design

Figure 10 shows the flowchart of the LCL filter design method. Inputs of the LCL filter design flowchart are the specifications of the inverter, such as the grid voltage v_{ac}, the switching frequency f_{sw}, the gate-block delay time t_{bd}, the DC-link voltage V_{dc}, the inverter output power P_{out}, and the maximum inverter output current overshoot of 150% i_{th}. First, the inverter side LC filter is designed from the specification of the inverter. The interconnected inductor L_1 is designed from the normalized value %Z of the inverter output impedance. The inductance of the interconnected inductor L_1 is derived as shown in (11)

$$L_1 = \frac{\%Z_{L1}}{\omega}\frac{{v_{ac}}^2}{P_{out}} \quad (11),$$

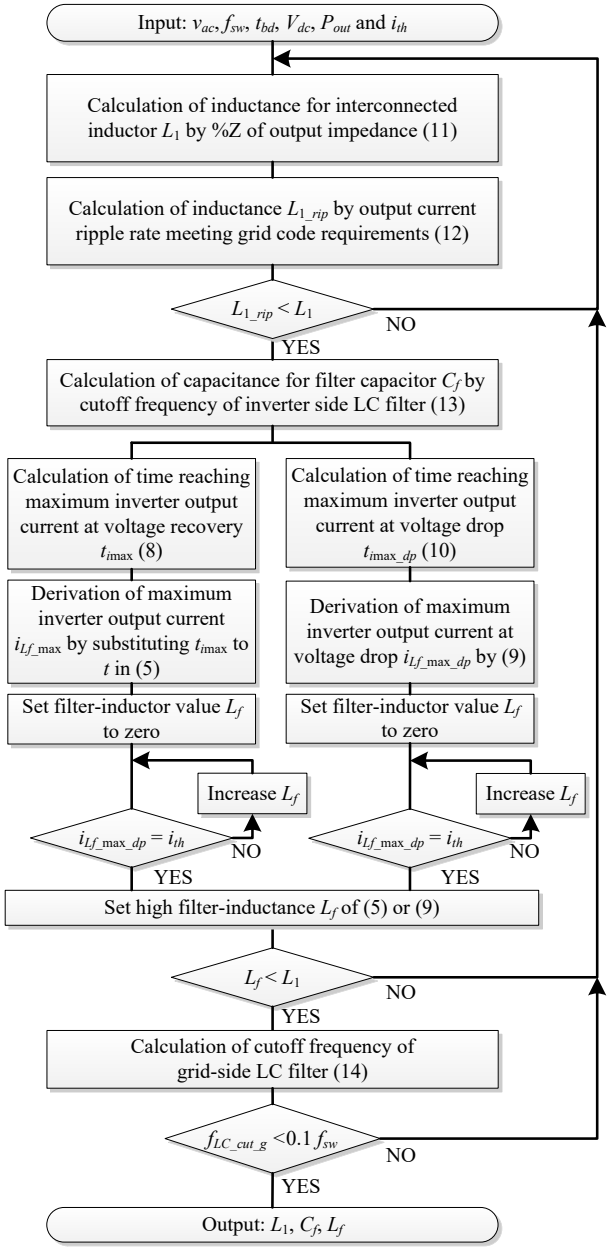


Fig. 10. Flowchart of LCL filter optimized design for grid-connected inverter. The LCL filter is designed to meet the FRT requirements and reduce the inverter output current overshoot less than 150%.

where $\%Z_{L1}$ is the normalized impedance of the interconnected inductor, v_{ac} is rms value of the grid voltage and P_{out} is inverter output power. The output current ripple is defined in the grid code. The inductance to meet the required current ripple L_{1_rip} is expressed as

$$L_{1\_rip} = \frac{V_{ac}}{\Delta I_{L1} f_{sw}}\frac{V_{dc} - V_{ac}}{V_{dc}} \quad (12),$$

where ΔI_{L1} is the required current ripple. If the inductance L_1 is less than L_{1_rip}, the interconnected inductor L_1 should be redesigned. Moreover, the interconnected inductor is

designed to reduce the switching ripple components of the inverter output current less than 0.3%, in order to meet the current quality [24]. The filter capacitor C_f is determined from the cutoff frequency of the inverter-side LC filter $f_{LC\_cut\_inv}$. The filter capacitor C_f is expressed as

$$C_f = \frac{1}{\left(2\pi f_{LC\_cut\_inv}\right)^2 L_1} \quad (13).$$

After that, the filter inductor L_f is determined to meet the inverter output current overshoot less than 150% at the voltage recovery according to (5) and (8). Furthermore, the filter inductor L_f is determined to meet the inverter output current overshoot less than 150% at the voltage drop according to (9) and (10). The filter inductance L_f is set to higher one which is derived in (5) or (9). If the interconnected inductor L_1 is less than the filter inductor L_f, the inverter side LC filter should be redesigned when determining the filter inductor. In addition, considering the suppression of the switching-frequency-order harmonic, if the cutoff frequency of the grid-side LC filter $f_{LC\_cut\_g}$ is higher than 10% of the switching frequency, the inverter side LC filter should be redesigned. The cutoff frequency of the grid-side LC filter $f_{LC\_cut\_g}$ is expressed as

$$f_{LC\_cut\_g} = \frac{1}{2\pi\sqrt{L_f C_f}} \quad (14).$$

Outputs of the LCL filter design flowchart are the interconnected inductance L_1, the filter capacitance C_f, and the filter inductance L_f. The difference between the proposed LCL filter design and the conventional LCL filter design such as [25] is the consideration of the suppression of the inverter output current overshoot at the voltage sag. Note that the consideration of the reduction for the harmonic components is same in both the proposed and conventional LCL filter design.

Table I shows the calculation result of the LCL filter design based on the flowchart of Fig. 10. The interconnected inductor impedance is 1.0% of the inverter normalized impedance, whereas the filter inductor is 0.78%. The filter capacitor is determined to let the cutoff frequency of inverter side LC filter be 10 kHz (one sixteenth of equivalent switching frequency). In the calculation result with the designed LCL filter, the maximum output current overshoot is suppressed less than 150%. Furthermore, the LCL filter in Table I is designed with a margin in order to ensure the maximum inverter output current overshoot less than 150%. Moreover, in order to reduce the resonance current in the LCL filter, a damping resistor R_f is connected to the filter capacitor in series. The resistance of the damping resistor is selected to consume below 0.1% of the inverter output power; therefore, the voltage drop of the damping resistor is ignored. Considering only the normal operation, it is possible to further reduce the total inductance of the LCL filter in the conventional LCL filter design [26] compared with the proposed LCL filter design. However, when considering the delay time for the gate-block operation in the ZVRT, the reduction of the total inductance is restricted in order to meet the FRT requirements. Therefore, the proposed LCL filter design clarifies this reduction limitation of the total inductance.

TABLE I. INITIAL CONDITION AND CALCULATION RESULT OF LCL FILTER DESIGN.

Initial condition	
Grid voltage V_{ac}	283 V
DC-link voltage V_{dc}	380 V
Output power P_{out}	1 kW
Rated inverter output current I_{Lf}	7.07 A
Inverter output voltage V_{inv}	380 V
Carrier frequency f_{cry}	80 kHz
Equivalent switching frequency f_{sw}	160 kHz
Gate-block delay time t_{bd}	3.0 μs
Inverter output current limit by FRT requirement i_{th}	I_{Lf}×1.5
Calculation result	
Interconnected inductor L_1	1.29 mH
Filter capacitor C_f	0.2 μF
Filter inductor L_f	0.99 mH
Maximum inverter output current at voltage recovery i_{Lf_max}	-10.3 A (145%)
Maximum inverter output current at voltage drop $i_{Lf\_max\_dp}$	10.1 A (143%)

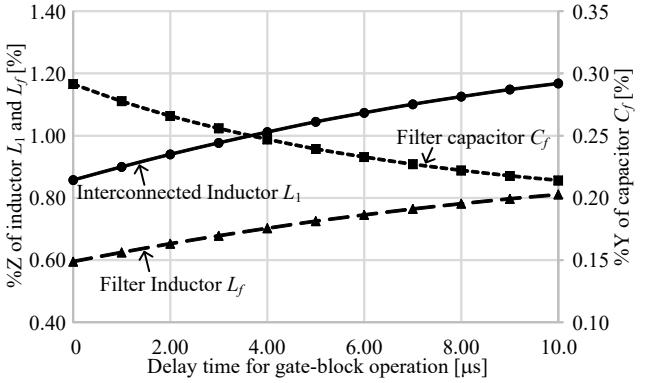
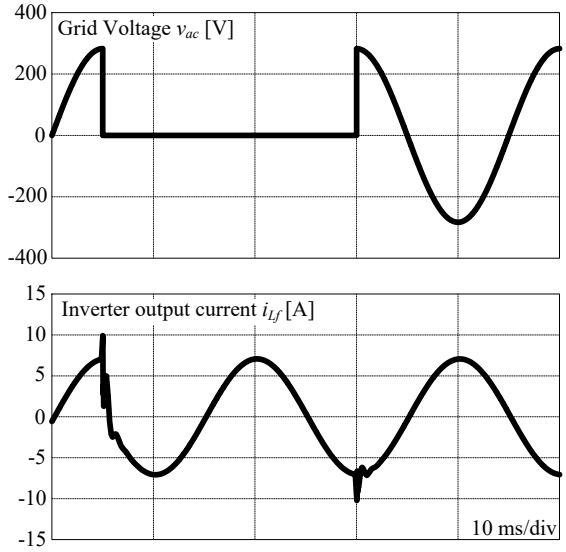
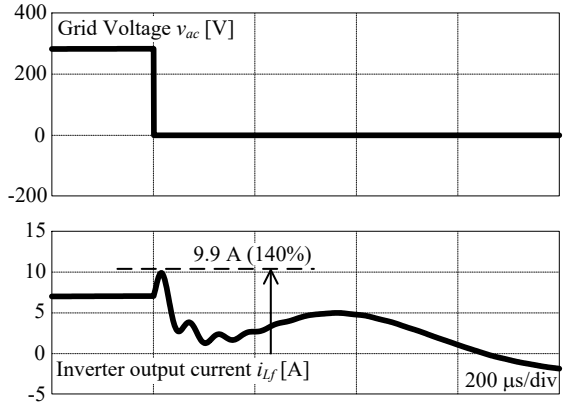


Fig. 11. Relationship between delay time of gate-block operation and design parameters of minimized LCL filter in 1-kW system. The LCL filter parameter is designed in order that the maximum inverter output current overshoot is 150%.

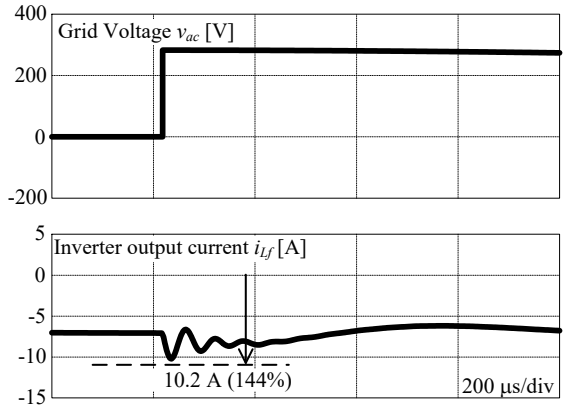
Figure 11 shows the characteristics of the delay time for the gate-block operation and the minimized LCL filter parameter when the maximum inverter output current overshoot is 150%. In this design, the LCL filter is designed as follows; the cutoff frequency of the inverter side LC filter is 10 kHz, the cutoff frequency of the grid-side LC filter is 12 kHz, and the maximum inverter output current overshoot becomes 150% at the voltage recovery. In Fig. 11, when the delay time for the gate-block operation is short, the interconnected inductor and the filter inductor are possible to



(a) Waveform of ZVRT operation.



(b) Voltage drop operation.



(c) Voltage recovery operation.

Fig. 12. Simulation result of grid failure with minimized LCL filter by using proposed design method. The maximum inverter output current overshoot is suppressed to become less than 150%.

minimize. This is because when the delay time for the gate-block operation is short, the effect of the inverter output current overshoot caused by the short grid failure is small. On the other words, the interconnected-inductor value and the filter-inductor value are limited by the delay time for gate-block operation.

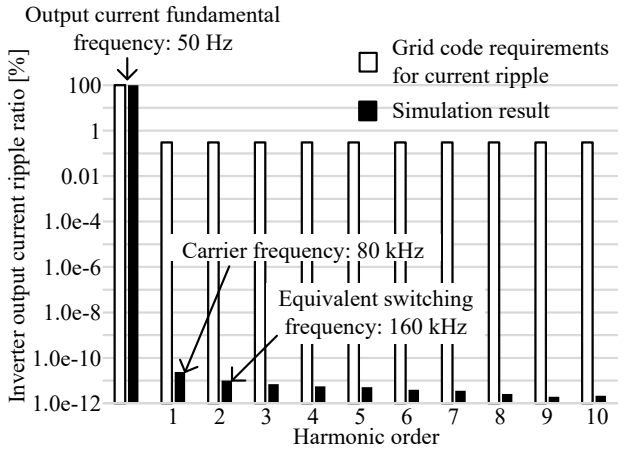


Fig. 13. Simulation result of harmonic analysis for switching frequency components with designed LCL filter. The switching components are enough low compared with the output current frequency.

C. Simulation of ZVRT with designed LCL filter

In order to confirm validity of the designed LCL filter in Table I, the ZVRT operation with the designed LCL filter is evaluated in simulation. Figure 12 shows the simulation results of the ZVRT with the proposed high-speed gate-block method. By using the proposed high-speed gate-block method, the inverter output current is suppressed to 9.9 A at the grid voltage drop as shown in Fig. 12 (b) (Overshoot: 140%). Moreover, at the grid voltage recovery, the inverter output current overshoot is suppressed to 10.2 A as shown in Fig. 12 (c) (Overshoot: 144%). Thus, the grid-connected inverter with the minimized LCL filer meets the inverter output current overshoot less than 150% by using the proposed high-speed gate-block method. Comparing the inverter output current overshoot between the calculation value and the simulation value at the voltage recovery and drop, the error rates are 2.2% and 2.1%. Thus, the validity of the LCL filter design method meeting the FRT requirements is confirmed. Moreover, the error between the calculation value and the simulation value occurs due to the damping resistor, the precision of approximation and the steady-state current at the grid voltage recovery is constant value in the calculation. Therefore, by using the high-speed gate-block method and the optimized LCL filter design method, it is possible to minimize the LCL filter and still meet the FRT requirements.

Figure 13 shows the simulation result of the harmonic analysis for the output current with the designed LCL filter in the normal operation in order to confirm the effect of the harmonic component, e.g. switching frequency. In Fig. 13, the switching-frequency-order harmonic components of the output current are very low compared with the output current fundamental frequency component (50 Hz). In particular, the simulation result of the switching ripple components meets less than 0.3% for the standard such as IEEE Std. 1547 [24]. Note that the switching ripple components are greatly lower than the grid code requirement values, because the total inductance of the filter which meets the FRT requirements is

higher than that which meets the harmonic restraint.

D. Consideration of inverter maximum output current overshoot with grid impedance

Figure 14 shows the circuit diagram considering a grid inductor connected to the LCL filter at the grid-side. The effect of the grid impedance for the FRT capability by using the proposed high-speed gate-block method is confirmed under the condition that there is grid impedance in the actual grid. As shown in Fig. 14, it is impossible to directly detect the grid voltage v_{ac}, because the detection point of the grid voltage is between the grid inductor L_g and the filter inductor L_f.

Figure 15 shows the simulation results of the relationship between the maximum inverter output current overshoot at the grid voltage recovery and the ratio between grid impedance and filter inductance L_g/L_f. Note that the filter-inductor value L_f is 0.99 mH (%Z of 0.78%) which is designed in Table I. The grid impedance L_g is changed from zero to the filter-inductor value L_f. As shown in Fig. 15, the maximum inverter output current overshoot decreases when the grid impedance L_g increases, the inverter output current variation is reduced by the increase in the grid impedance L_g.

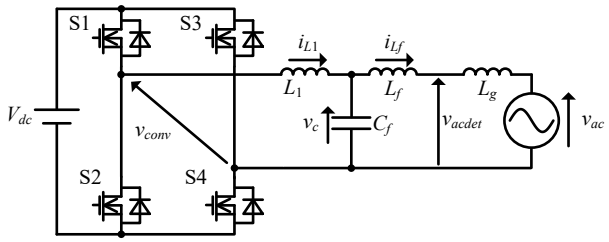


Fig. 14. Circuit configuration with grid impedance L_g. In actual grid connection, there is grid impedance between the inverter output and the grid voltage.

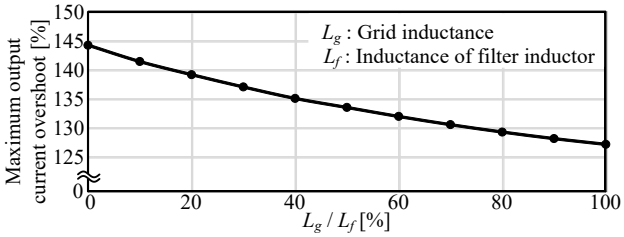


Fig. 15. Simulation results of maximum inverter output current overshoot at grid voltage recovery and ratio between grid inductance L_g and filter inductance L_f. When the grid impedance is low, the maximum output current overshoot becomes high.

IV. Experimental Result

Table II shows the experimental condition. The LCL filter that designed in Table I is used. Note that in the experiment, in order to consider the worst case of the grid, the ZVRT operation is confirmed without the grid inductor. The designed LCL filter is tested under three FRT methods; the conventional FRT method I in which the controller is shown in Fig. 3 with the grid voltage feedforward, the conventional FRT method II in which the controller is shown in Fig. 4 with both the grid voltage feedforward and the high-gain DOB, and the proposed FRT method in which the controller is shown in Fig. 5 with the grid voltage feedforward, the high-gain DOB and the high-speed gate-block function.

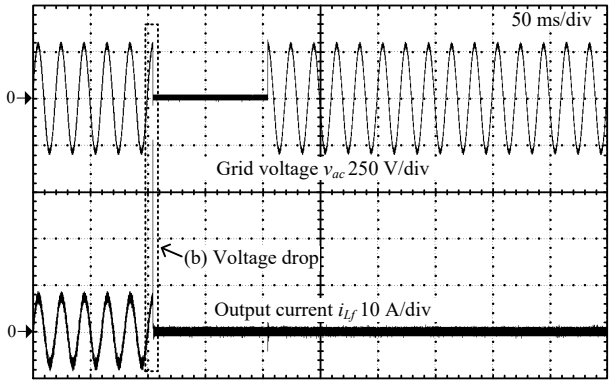
TABLE II. Experimental condition.

Output power	P_{out}	1 kW	Filter cap.	C_f	0.2 μF
DC link vol.	V_{dc}	380 V	Carrier fre.	f_{cry}	80 kHz
Grid voltage	v_{ac}	200 V_{rms}	Ang. fre. of ACR	ω_n	6000 rad/s
Inter. Induc. (%Z)	L_1	1.29 mH (1.0%)	Samp. fre. of ACR	f_{samp}	20 kHz
			Samp. fre. of DOB	f_{so}	80 kHz
Filter Induc. (%Z)	L_f	0.99 mH (0.78%)	Cutoff fre. of DOB	f_c	2 kHz
			GB delay time	t_{delay}	< 3 μs

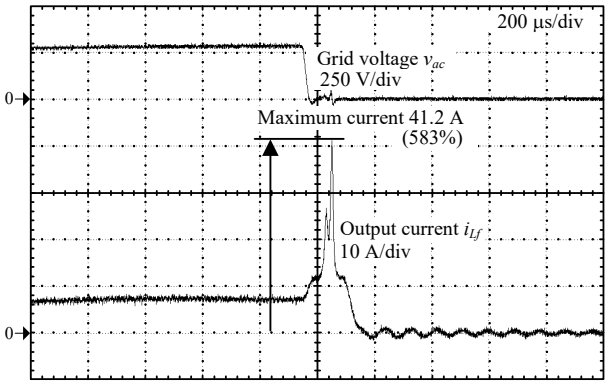
	Conventional FRT method I	Conventional FRT method II	Proposed FRT method
Voltage Feedforward	○	○	○
High-gain DOB		○	○
High-speed Gate-block			○
Block diagram	Fig. 3	Fig. 4	Fig. 5

Figure 16 shows the experimental result of the ZVRT operation with the conventional FRT method I with only the grid voltage feedforward. After the grid voltage drop, the inverter output current overshoots to 41.2 A (Overshoot: 583%). After that, the inverter operation is halted owning to the over current protection. Due to the detection and the sampling delay, the inverter output current overshoot with the minimized LCL filter is large. As a result, the inverter output current reaches the over current threshold. Thus, it is impossible to continue the inverter output during the voltage sag with the minimized LCL filter by using the conventional FRT method I.

Figure 17 shows the experimental result for the ZVRT operation of the conventional FRT method II with both the grid voltage feedforward and the high-gain DOB. In Fig. 17 (a), it is possible to continue the operation after both the voltage drop and the voltage recovery because the high-gain DOB suppresses the current overshoot. However, in Fig. 17 (b)-(c), the inverter output current maximum values at the voltage drop and the voltage recovery are 13.2 A (Overshoot: 187) and 12.3 A (Overshoot: 174%), respectively. Thus, it is impossible to reduce the maximum inverter output current overshoot less than 150% at the voltage recovery. If the sampling frequency for the disturbance compensation increases in order to reduce the computation time of the high-gain DOB, it might be possible to suppress the inverter output current overshoot less than the threshold value of over current protection. However, due to the delay time of the detection and the sampling, the maximum inverter output current overshoot exceeds 150% with the minimized LCL filter that is composed by the minimized interconnected inductor (%Z of 1.0%) and filter inductor (%Z of 0.78%). As a conclusion, it is necessary to reduce the detection delay time to reduce the

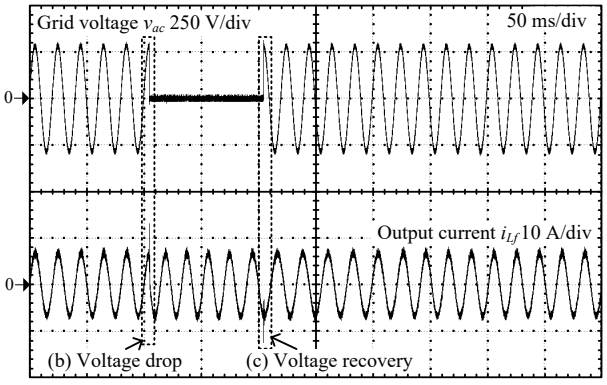


(a) Waveform of ZVRT operation.

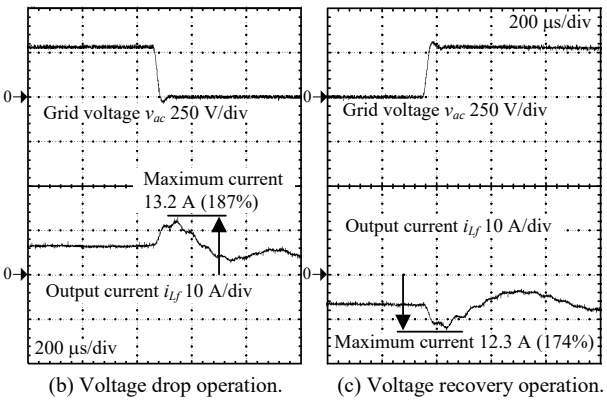


(b) Voltage drop operation.

Fig. 16. Experimental results of grid failure with conventional FRT method I with only grid voltage feedforward. The inverter output current overshoot is large due to the detection and the sampling delay at the voltage drop.



(a) Waveform of ZVRT operation.



(b) Voltage drop operation. (c) Voltage recovery operation.

Fig. 17. Experimental results of grid failure with conventional FRT method II by applying DOB. The inverter output current overshoot exceeds 150% due to the delay for disturbance compensation caused by the detection and the sampling delay.

inverter output current overshoot less than 150% with the minimized LCL filter and meet the FRT requirements.

Figure 18 shows the experimental result of the ZVRT operation with the proposed FRT method in which the high-speed gate-block method is applied, under the conditions when the voltage drop and recovery occur at the grid voltage phase of 90 degree. By using the proposed FRT method, the inverter output current overshoot at the grid voltage drop in Fig. 18 (b) is 10.3 A (Overshoot: 146%) , whereas the inverter output current overshoot at the grid voltage recovery in Fig. 18 (c) is 10.3 A (Overshoot: 146%). Moreover, the gate-block operation is confirmed at the voltage drop and recovery in Fig. 18 (d). Therefore, it is confirmed that the grid-connected inverter with the minimized LCL filter meets the FRT requirements and the inverter output current less than 150% by the proposed high-speed gate-block method and the designed LCL filter. There is an error of 1.1% between the maximum current overshoot of the calculation result and the experimental result at the grid voltage recovery. The error is caused by the approximation when deriving the equation, and the inconsideration of the damping resistor. In addition, the active power recovery operation after the grid voltage recovery is considered. After the grid voltage recovery, the output current phase which is added to the PLL phase is decreased gradually from $\pi/2$ to zero. The reduction speed is approximately 10/9 ms/deg. In Fig. 18 (e), the output power recovery period is 95 ms after the grid voltage recovery. Therefore, the output power recovery operation is also confirmed to meet the FRT requirements.

Figure 19 shows the experimental result of the ZVRT operation with the proposed FRT method, under the conditions when the voltage drop and recovery occur at the grid voltage phase of 0 degree. When the grid faults occur at the voltage phase of 0 degree, the momentary voltage fluctuation does not occur and the gate-block operation is not carried out. However, the inverter output current overshoot does not occur in this case. Thus, the inverter output current overshoot is suppressed without the proposed gate-block operation during the grid fault at the grid voltage phase of 0 degree. As a conclusion, the main contribution of the proposed FRT method is the high-speed gate-block operation and the low-inductance LCL filter design method. Meanwhile, the detection of the grid faults can be achieved by several separate or combined methods, e.g. the use of HPF to detect the rapid change of the grid voltage, or the overshoot current detection, in which the current detection values is compared with a threshold by an analog circuit. By considering the delay time of each grid fault detection method, the same high-speed gate-block operation and the low-inductance LCL filter design method proposed in this paper can be applied.

Figure 20 and 21 show the experimental results of the LVRT operation with the proposed FRT method. The experimental results are considered with the grid voltage down from 100% to 20% at the grid phase of 90 degree and 0 degree. In Fig. 20, the maximum inverter output current overshoot is suppressed to less than 150% with the gate-block operation at the voltage drop and recovery. Similarly to Fig. 19, in Fig. 21, it is possible to continue the operation of the inverter without the gate-block operation. Therefore, it is confirmed that the LVRT operation is also achievable with the proposed method.

V. CONCLUSION

In this paper, the ZVRT operation of the single-phase grid-connected inverter with the minimized LCL filter was verified. In particular, the high-speed gate-block method that is implemented in analog circuit and FPGA was proposed; moreover, the minimized LCL filter design method was presented in order to satisfy the FRT requirements and reduce the inverter output current overshoot less than 150%. It was confirmed through the experimental results that the maximum inverter output current overshoot during the voltage sag was suppressed to become less than 150% by the proposed high-speed gate-block method and the design of the LCL filter. In particular, the interconnected inductor was minimized to 1.0% of %Z and the filter inductor is minimized to 0.78% of %Z in the 1-kW prototype. Therefore, by applying the proposed method, it is possible to reduce the size of LCL filter and still meet the FRT requirements.

In future, the ZVRT operation for the three-phase grid-connected inverter with the minimized output filter will be considered. Furthermore, the design of the minimized output filter will be also evaluated.

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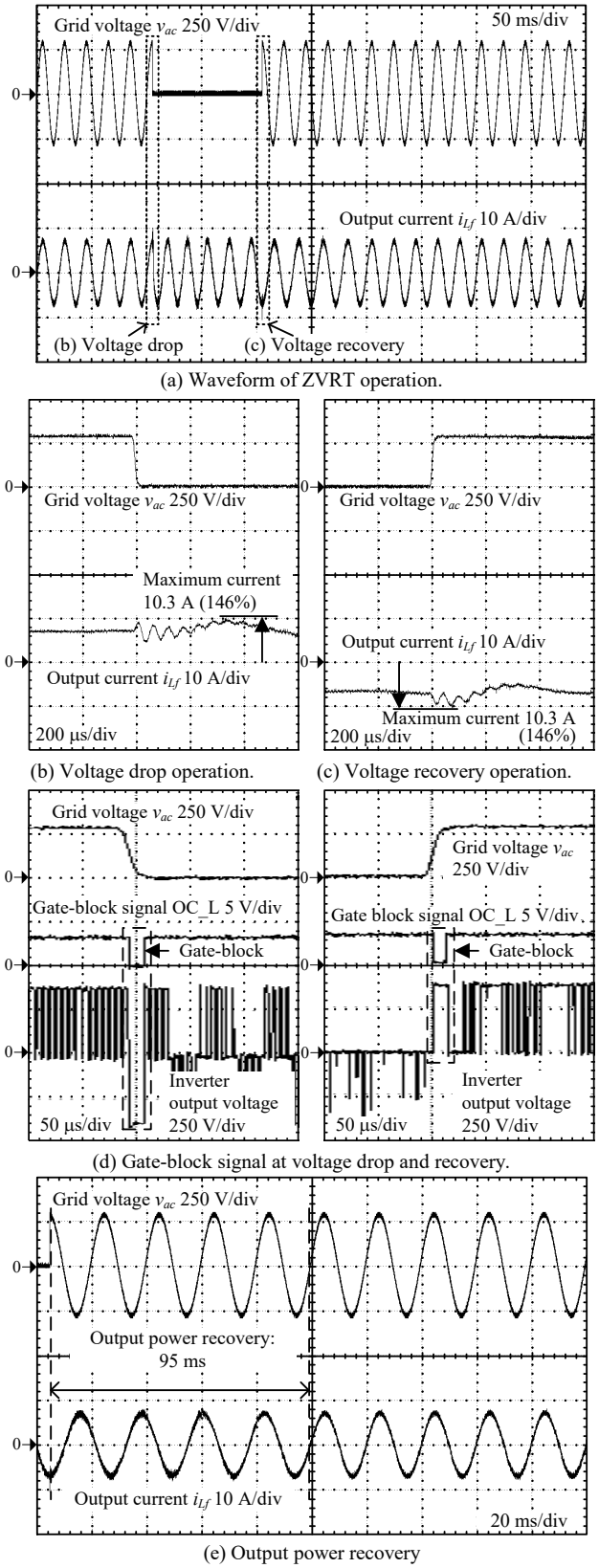
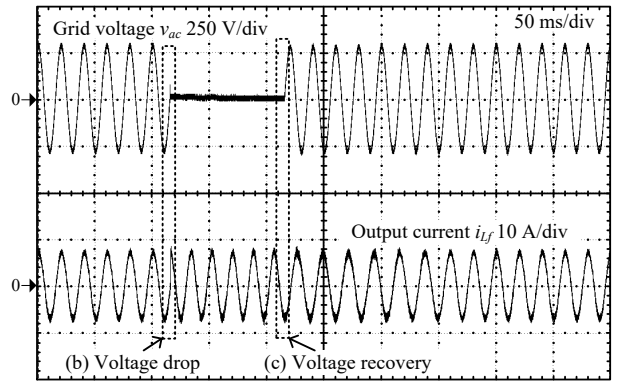
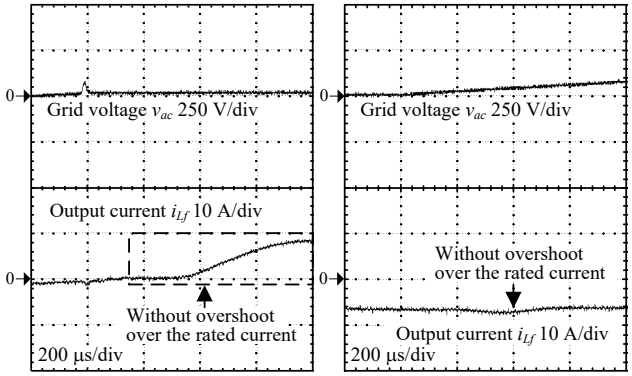


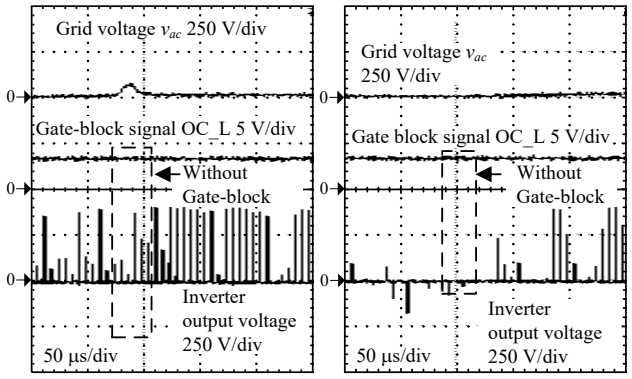
Fig. 18. Experimental results of grid failure at grid phase of 90 degree with proposed ZVRT method. By applying the proposed method, it is possible to continue the operation of the inverter, and satisfy the FRT requirements.



(a) Waveform of ZVRT operation.

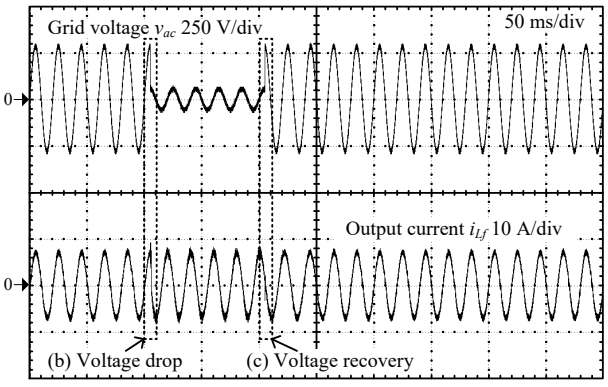


(b) Voltage drop operation. (c) Voltage recovery operation.

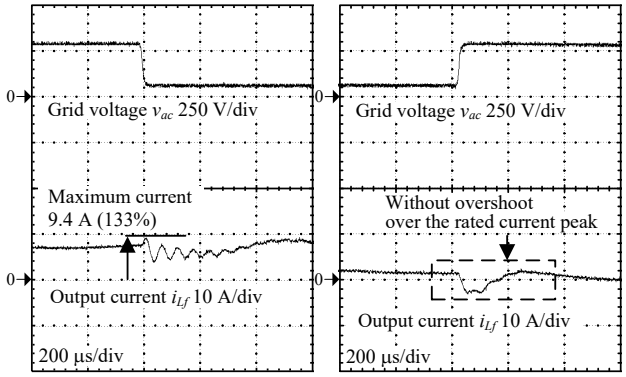


(d) Gate-block signal at voltage drop and recovery.

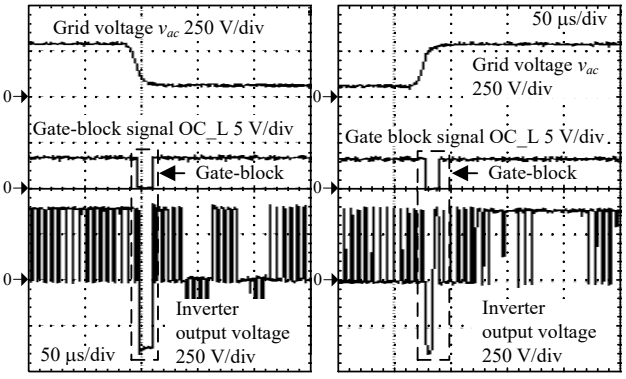
Fig. 19. Experimental results of grid failure at grid phase of 0 degree with proposed ZVRT method. Without the gate-block operaiton, it is possible to continue the operation of the inverter, and satisfy the FRT requirements.



(a) Waveform of LVRT operation.



(b) Voltage drop operation. (c) Voltage recovery operation.



(d) Gate-block signal at voltage drop and recovery.

Fig. 20. Experimental results of grid failure at grid phase of 90 degree with proposed method in LVRT operation (Grid voltage down to 20%). The maximum inverter output current overshoot is suppressed to less than 150%

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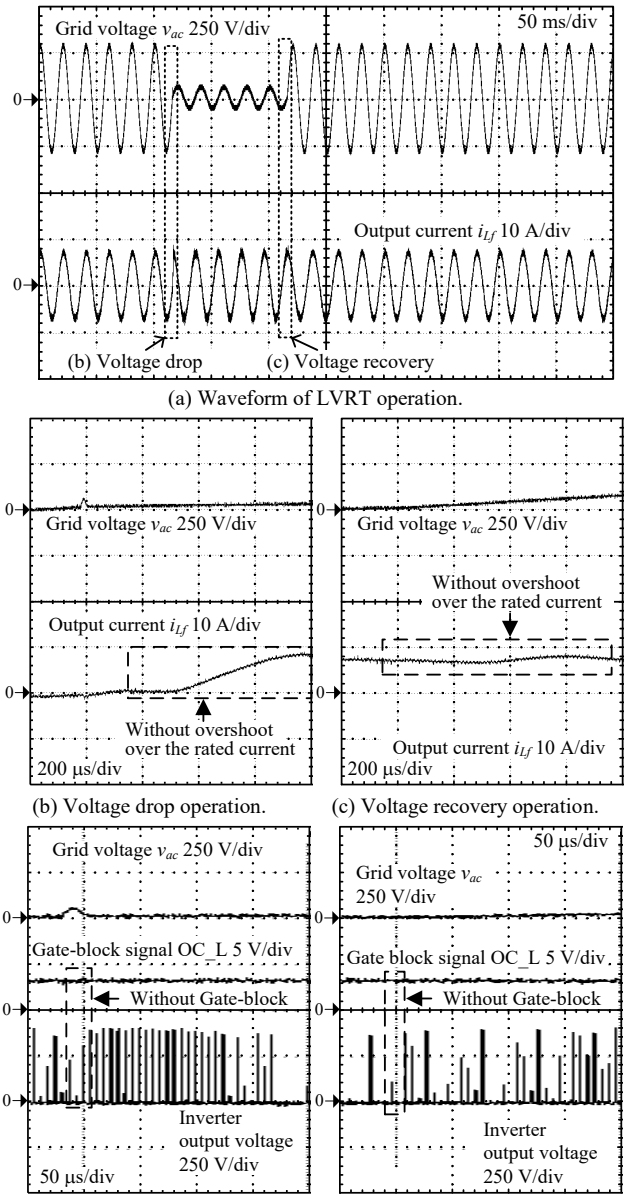

Fig. 21. Experimental results of grid failure at 0 degree of grid phase with proposed method in LVRT operation (Grid voltage down to 20%). Without the gate-block operaiton, it is possible to continue the operation of the inverter, and satisfy the FRT requirements.

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