# Dead-time Compensation with DC Offset Current Elimination Method using Three-level Operation for Dual Active Bridge DC-DC Converter

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Abstract—This paper proposes a compensation method of a non-liner transmission power error caused by a dead-time for a dual active bridge (DAB) converter with three-level operation. This power error is compensated by the zero-voltage period longer than the dead-time in three-level mode. In addition, the mode change sequence between two-level and three-level is also proposed to suppress a dc offsets on the transformer current. The validity of the proposed method is confirmed by a 2.5-kW prototype. As the experimental results, the transmission-power error is reduced by 80.7%. In addition, the peak value of the magnetizing current at the transient state is reduced by 56% because the dc offset is eliminated. Moreover, the mode changing is achieved within two switching periods.

#### Keywords—DC-DC converter, Dual Active Bridge, Deadtime, Three-level operation, DC offset

#### I. INTRODUCTION

In recent years, energy storage systems for DC microgrid systems and electric vehicles have been actively researched [1-6]. In order to satisfy the requirements of energy storage systems such as, e.g. a bidirectional operation and a galvanic isolation, a bi-directional isolated DC-DC converter is necessary. A dual active bridge (DAB) converter is generally employed for these application [7-9], and the transmission power and a power flow are controlled by a single phase shift (SPS) control [10]. In addition, the DAB converter obtains high efficiency because of achieving zero voltage switching (ZVS) without additional component.

However, the transmission power error occurs due to the dead-time at light load, although the DAB converter is required wide operating range between light and heavy load condition [11-12]. In order to reduce the error of the transmission power, the dead-time compensation method has been proposed [12]. In this paper, the dead-time error is compensated by the feedforward compensation that subtracts the dead-time phase from the reference of phase difference. However, this conventional method is only applied when the transmission-power error is liner. Moreover, the inverteroutput-voltage polarity is reversed, which is called a voltagepolarity-reversal phenomenon, inducing a strong nonlinear behavior when inductor current becomes zero during the dead-time. Consequently, the non-liner transmission power error due to the dead-time is not compensated by the conventional compensation method [11]. Meanwhile, a three-level operation has been proposed in order to improve light-load efficiency with achieving ZVS against the voltage fluctuation at the DC bus [13-16]. In [16], the power range of the converter operation with high efficiency is extended using three-level operation. However, the mode changing between the two-level operation and the three-level operation induces a dc offset in an inductor current and a magnetizing current. This is because the inductor current and the magnetizing current is not accurately estimated to alternate the operation due to the transmission power error owing to the dead-time. Moreover, the dc offset in the magnetizing current is not eliminated in spite of matching voltage time product around the changing mode points because waveforms of the magnetizing current are different, i.e. triangular waveform and trapezoidal waveform.

This paper proposes a dead-time compensation method in order to accomplish the following objectives; the reduction of the transmission-power error at light load, and the mode changing between the two-level operation and the three-level operation without inducing the dc offsets. In particular, the voltage-polarity-reversal phenomenon is eliminated by adjusting the phase difference of the three-level operation at light load. Consequently, the dc offset in the magnetizing current is eliminated by estimating the magnetizing current, whereas the dc offset in the inductor current is eliminated by equaling the voltage time product around the changing mode points.

This paper is organized as follows; firstly, proposed three-level operation modes and non-liner dead-time compensation method are proposed. Secondly, the elimination method of the dc offset in the inductor current and magnetizing current is introduced. Finally, experiments are conducted in order to verify the compensation method of non-liner dead-time error and the elimination method of dc offset in the inductor current and the magnetizing current when the operation mode is changes.

#### II. CONVENTINAL CONTROL METHOD

Fig. 1 shows the circuit configuration of the DAB converter. The DAB converter consists of two H-bridge inverters, an additional inductor, and a high frequency transformer. The primary and the secondary inverters generate the square-wave voltage, and transmission power is controlled by a phase difference between each inverter output voltage using the SPS control. The transferred power is expressed by (1) [12].

$$P = \frac{NV_{in}V_{out}}{\omega L} \delta \left( 1 - \frac{|\delta|}{\pi} \right)$$
(1)

where,  $\omega$  is switching angular frequency, *L* is additional inductor. *N* and  $\delta$  are turn ratio and phase difference between primary inverter output voltage  $v_{pr}$  and secondary inverter output voltage  $v_{se}$ .

Fig. 2 shows the conventional operation waveform with and without the dead-time. In the case of taking no account of the dead-time, the transmission power is controlled by the phase difference without the transmission power error. However, in an actual system, the dead-time is needed in order to prevent two switching devices to avoid the short circuit. In this case, the transmission-power error occurs at light load when the inductor current becomes zero during the dead-time. The inductor current is clamped to zero because current does not conduct primary inverter during the deadtime. As the result, polarity of primary inverter output voltage is reversed by the clamped inductor current. Consequently, the transmission-power error occurs due to the dead-time [12].

Fig.3 shows the influence of the voltage-polarity-reversal phenomenon for the transmission power at the condition of  $V_{in} = NV_{out}$ . The transmission power error caused by the voltage-polarity-reversal phenomenon is not compensated by conventional feedforward method because the the transmission power error due to the dead-time varies depending on the width of the voltage-polarity-reversal. Meanwhile, the period of the voltage-polarity reversal depends on the relationship between the inductor current and the dead-time period [12]. At the period between  $2\delta_{dt}$  and  $\delta_{dt}$ , the transmission power error is varied in according with the width of the voltage-polarity-reversal. After  $\delta_{dt}$ , the transmission-power error becomes constant value of the dead-time without the voltage-polarity reversal. In the area where the phase difference  $\delta$  is smaller than the dead-time  $\delta_{dt}$ , power is not transferred because the phase difference is canceled by the dead-time.

#### III. PROPOSED DEAD-TIME CONPENSATION METHOD

Fig. 4 shows the operation principle of controlling the phase difference and the zero voltage phases. The three-level mode is operated by the phase difference and the zero-voltage phases with controlling switches of each leg independently [8]. In order to control switching devices independently, phase-shift carriers for each leg are controlled. The phase difference and zero-voltage phases are generated as follows. First, the phase difference is controlled by advancing the phase-shift carriers of the primary inverter by a half of the phase difference and delaying the phase-shift carriers of each inverter are shifted by zero-voltage phases of primary and secondary side. Amounts of the phase-shift of each carrier on the basis of the top of the base carrier are expressed by (2).

$$\begin{cases} \theta_A = 0.25\delta + 0.75\varepsilon - 0.25\gamma \\ \theta_B = 0.25\delta - 0.25\varepsilon - 0.25\gamma \\ \theta_R = 0.25\delta - 0.25\varepsilon - 0.25\gamma \\ \theta_S = 0.25\delta - 0.25\varepsilon + 0.75\gamma \end{cases}$$
(2)



where,  $\varepsilon$  and  $\gamma$  are the zero voltage phase of primary inverter output voltage and secondary inverter output voltage.

Fig. 5 shows operation waveforms of the proposed threelevel mode. In the proposed operation method, the zero voltage phases of each inverter are controlled identically with the phase difference  $\delta$  as a constant. In order to transfer the power over wide load range, the three-level operation is further divided into the three-level mode I for very light load operation and the three-level mode II for light load operation. The specification of three-level modes under the condition of  $V_{in} = NV_{out}$  and  $\varepsilon = \gamma$  as follows. Note that the parasitic capacitance and the magnetizing current are not considered in this calculations.

#### 1) Three-level mode I for very light load

Under the steady state condition, the inductor current  $i_{LI}$  at the switching moment as follows,

$$i_{LI}(\theta) = \begin{cases} \frac{V_{in}}{\omega L} (\theta - \delta + \varepsilon) & (0 \le \theta \le \delta - \varepsilon) \\ 0 & (\delta - \varepsilon \le \theta \le \varepsilon) \\ \frac{V_{in}}{\omega L} (\theta - \varepsilon) & (\varepsilon \le \theta \le \pi - \varepsilon) \\ \frac{V_{in}}{\omega L} (\pi - 2\varepsilon) & (\pi - \varepsilon \le \theta \le \delta + \varepsilon) \\ \frac{V_{in}}{\omega L} (\pi - \theta - \varepsilon + \delta) & (\delta + \varepsilon \le \theta \le \pi) \end{cases}$$
(3)

According to (3), the transmission power  $P_I$  is calculated by (4),

$$P_{I} = \frac{2}{2\pi} \int_{0}^{\pi} v_{pr}(\theta) i_{LI}(\theta) d\theta = \frac{V_{in}^{2}}{2\pi\omega L} (\pi - 2\varepsilon)^{2}$$
(4)

In order to be operated by the three-level mode I, PWM pulses of each inverter output voltage need to be overlapped. The condition of the three-level mode I is expressed by (5),

$$2\varepsilon \ge \pi - \delta \tag{5}$$

#### 2) Three-level mode II for light load

Under the steady state condition, the inductor current  $i_{LII}$  at the switching moment as follows,

$$i_{LII}(\theta) = \begin{cases} 0 & (0 \le \theta \le \varepsilon) \\ \frac{V_{in}}{\omega L} (\theta - \varepsilon) & (\varepsilon \le \theta \le \varepsilon + \delta) \\ \frac{V_{in}}{\omega L} \delta & (\varepsilon + \delta \le \theta \le \pi - \varepsilon) \\ \frac{V_{in}}{\omega L} (\pi - \varepsilon + \delta - \theta) & (\pi - \varepsilon \le \theta \le \pi - \varepsilon + \delta) \\ 0 & (\pi - \varepsilon + \delta \le \theta \le \pi) \end{cases}$$
(6)

Then, the transmission power  $P_{II}$  is given by (7) using (6),

$$P_{II} = \frac{2}{2\pi} \int_0^{\pi} v_{pr}(\theta) i_{LII}(\theta) d\theta = \frac{V_{in}^2}{2\pi\omega L} \delta(2\pi - 4\varepsilon - \delta)$$
(7)

In order to be operated by the three-level mode II, pulses of each inverter output voltage are not overlapped. The condition of the three-level mode II is expressed by (8),

$$2\varepsilon < \pi - \delta \tag{8}$$



#### *B.* Non-liner Dead-time Error Compensation

## *1)* Dead-time influence and compensation of three-level mode

Fig. 6 shows the dead-time influence of the primary inverter output voltage and the inductor current of the threelevel mode. The voltage-polarity-reversal phenomenon is eliminated by designing the clamped phase  $\lambda$  to become longer than the dead-time because the voltage-polarityreversal phenomenon occurs when the inductor current becomes zero during the dead-time. The condition that the clamped phase is longer than the dead-time is given by (9),

$$2\varepsilon \ge \delta_{dt} + \delta \tag{9}$$

However, the duty of the primary inverter output voltage is reduced by the dead-time because diodes of the B-phase leg is not conducted during the dead-time instead of designing clamped phase to be longer than the dead-time. Therefore, the duty of primary inverter output voltage is needed to be compensated. Fig. 7 shows the dead-time compensation for the threelevel mode. The duty error by the dead-time is compensated by (10) because the decrease of the duty affects the phase difference  $\delta$  and the zero voltage phase  $\varepsilon$ ,

$$\begin{cases} \delta_{ref} = \delta + \delta_{dt} / 2\\ \varepsilon_{ref} = \varepsilon - \delta_{dt} / 2\\ \gamma_{ref} = \varepsilon \end{cases}$$
(10)

where,  $\delta_{ref}$ ,  $\varepsilon_{ref}$  and  $\gamma_{ref}$  are reference of the phase difference, reference of zero voltage phase of the primary inverter, and zero voltage phase of the secondary inverter.

### 2) Decision of phase difference $\delta$

In this chapter, the phase difference  $\delta$  is chosen as transferring maximum power in order to compensate wide load range.

#### a) Three-level mode I for very light load

According to (4), the maximum transmission power is given by minimizing the zero voltage phase  $\varepsilon$ . Therefore, the phase difference of maximum transmission power  $\delta_{max_{I}}$  is given by (11) under the condition: right-hand side of (5) and (9) are equal.

$$\delta_{\max I} = \frac{1}{2} \left( \pi - \delta_{dt} \right) \tag{11}$$

Therefore, the range of the zero voltage phase  $\varepsilon$  and the transmission power of mode I  $P_I$  are expressed by (12) and (13) using (4), (5) and (9).

$$\frac{1}{4} \left( \pi + \delta_{dt} \right) \le \varepsilon \le \frac{1}{2} \pi \tag{12}$$

$$0 \le P_I \le \frac{V_{in}^2}{4\pi\omega L} (\pi - \delta_{dt})^2 \tag{13}$$

#### b) Three-level mode II for light load

The transmission power becomes maximum when (13) holds equation because the zero current phase is the shortest. Thus, the transmission power  $P_{II}$  is expressed by (14) from (7) and (9),

$$P_{II} = \frac{V_{in}^2}{2\pi\omega L} \left\{ -\delta^2 + \left( -\delta_{di} + 2\pi \right) \delta \right\}$$
(14)

According to (14), the phase difference  $\delta$  of transferring the maximum power is derived by finding the minimal value of the phase difference  $\delta$ . The minimal value of the phase difference  $\delta$  is introduced by (15),

$$\frac{d}{d\delta} \left\{ -\delta^2 + \left( -\delta_{dt} + 2\pi \right) \delta \right\} = 0$$
(15)

Hence, the phase difference  $\delta_{max\_II}$  of the maximum transmission power of mode II is given by (16),

$$\delta_{\max II} = \frac{1}{3} \left( \pi - \delta_{dI} \right) \tag{16}$$

Therefore, the range of the zero voltage phase  $\varepsilon$  and the transmission power of the mode II  $P_{II}$  are expressed by (17) and (18) using (8) and (9).





$$\frac{1}{6} \left( \pi + 2\delta_{dt} \right) \le \varepsilon \le \frac{1}{6} \left( 2\pi + \delta_{dt} \right) \tag{17}$$

$$\frac{V_{in}^2}{18\pi\omega L} (\pi - \delta_{dt})^2 \le P_{II} \le \frac{V_{in}^2}{6\pi\omega L} (\pi - \delta_{dt})^2$$
(18)

#### 3) Determination of operation modes

Fig .8 shows the operation range of the proposed methods. The two-level mode is applied at the linear region of the transferred power. The three-level mode I is adopted when the load is very light with the dead-time influence. In addition, the three-level mode II is applied between the twolevel mode and the three-level mode I.

Fig. 9 shows the flowchart for the determination of operation modes. the operation mode is determined as follows; the phase difference  $\delta$  is calculated with the transmission power  $P_{ref}$  by (19) from (1).

$$\delta = \frac{1}{2} \left( \pi - \sqrt{\pi^2 - \frac{4\pi\omega LP_{ref}}{V_{in}^2}} \right)$$
(19)

The operation mode is decided by the reference of the phase difference  $\delta_{ref}$  and the dead-time  $\delta_{dt}$ . Under the condition of  $\delta_{ref} > 2 \delta_{dt}$  as Fig. 3, the two-level operation is applied. In contrast, the three-level operation is used in the condition of  $\delta_{ref} \le 2 \delta_{dt}$ . The three-level operation with mode II is applied when the zero-voltage period  $\varepsilon$  satisfies (20),

$$\varepsilon \ge \frac{1}{6} \left( 2\pi + \delta_{dt} \right) \tag{20}$$

In the three-level mode II, the zero-voltage period  $\varepsilon$  is given by (7) in order to transfer the power  $P_{ref}$ .

$$\varepsilon = \frac{1}{4} \left( 2\pi - \delta - \frac{2\pi\omega L P_{ref}}{\delta V_{in}^2} \right)$$
(21)

If the condition (20) is not established, the DAB converter is operated by the three-level operation with mode I. In this mode, the zero-voltage phase  $\varepsilon$  is calculated by (22) from (4) in order to transfer the power  $P_{ref.}$ 

$$\varepsilon = \frac{1}{2} \left( \pi - \sqrt{\frac{2\pi\omega L P_{ref}}{V_{in}^2}} \right)$$
(22)

By applying the proposed three-level operation, the nonlinear transmission error due to the dead-time is compensated.

### IV. DC OFFSET ELIMINATION METHOD WITH OPERATION MODE CHANING

#### A. Mode-change from three-level mode to two-level mode

Fig. 10 shows relationship among each inverter output voltage, phase-shift carriers and switching signals of proposed method. The operation mode changing is divided into two phases, where the length of each step equals to a switching period. The dc offset in the inductor current is eliminated in first phase, whereas the dc offset in the magnetizing current is eliminated in second step. The carrier of each leg shown in Fig. 1 is adjusted in order to achieve the operation mode changing. In the first phase, the mode changing is implemented such that the voltage-time product around the mode changing points becomes equal, as shown in the shaded green and blue areas of Fig. 10, resulting no dc offset occurring in the inductor current [12]. However, the dc offset in the magnetizing current occurs during the first phase. In order to eliminate the dc offset in the magnetizing current, zero voltage phases are inserted into the inverter output voltage in the second phase in order to adjust the magnetizing current peak. The elimination of the dc offset in the magnetizing current is conducted by two steps. In the first step, the zero-voltage phase is inserted into each output voltage in order to keep peak value of two-level magnetizing current by controlling phase-shift carriers. Then, phase-shift carriers are modified in the second step in order to prevent the error of the phase difference due to carrier-control.

Fig. 11 shows the flowchart of the mode changing between three-level mode and two-level mode with dc offset elimination. The first phase is started at the top of the base



Fig. 10. Relationship between each inverter output voltage and phase-shift carriers of proposed method.



Fig. 11. Flowchart of dc offset elimination for mode changing.

carrier in order to make the voltage-time product around the mode changing points becomes equal, i.e. the elimination of the dc offset in the inductor current. At the end of the first phase, the magnetizing current is estimated by theoretical equation. The peak of the magnetizing current in the second phase needs to be adjusted in order to eliminate the dc offset in the magnetizing current. The adjustment of the increase in the magnetizing current is accomplished by inserting the zero voltage phase into the inverter output voltage. Assuming that the peak value of the magnetizing current at the end of the first step is an initial value, the transient magnetizing current  $i_{m\_tran}$  is estimated by (23).

$$i_{m\_tran} = -\frac{V_{out}}{\omega L_m} \theta + \frac{V_{out}}{2\omega L_m} (\pi - 2\varepsilon)$$
(23)

where,  $L_m$  is the magnetizing inductance. The peak value of the two-level magnetizing current  $i_{m_2Lv}$  is given by (24).

$$i_{m_2L\nu} = -\frac{V_{out}}{2\omega L_m}\pi$$
(24)

According to (23) and (24), the assumed period  $\alpha$  when the transient magnetizing current reaches the two-level peak is expressed by (25).

$$-\frac{V_{out}}{2\omega L_m}\pi = -\frac{V_{out}}{\omega L_m}\alpha + \frac{V_{out}}{2\omega L_m}(\pi - 2\varepsilon)$$

$$\alpha = \pi - \varepsilon$$
(25)

By inserting the zero voltage into secondary inverter output voltage at the timing of the two-level peak using (25), the magnetizing current keeps up the two-level peak. In addition, the zero voltage is inserted into the primary inverter output voltage in order to fit the phase difference to the secondary inverter output voltage. In the primary output voltage, the voltage-polarity-reversal phenomenon occurs at the inserted zero voltage phase because the phase difference is small due to the inserted zero voltage phase. Hence, the dead-time error due to the voltage-polarity-reversal phenomenon is compensated by adjusting the zero-voltage phase. Thus, the assumed period of primary side  $\alpha_{pr}$  is calculated as (26),

$$\alpha_{pr} = \pi - \varepsilon - \delta_{dt} \tag{26}$$

In order to insert the zero voltage phase at the assumed phase  $\alpha_{pr}$  and  $\alpha$ , the on-timing of switch S<sub>1</sub> and S<sub>5</sub> are controlled by the A-phase carrier and the R-phase carrier. In the digital controller, a carrier is generated by up-down count. Therefore, on timing of S<sub>1</sub> and S<sub>5</sub> is controlled by changing the value of the A-phase carrier counter and R-phase carrier counter. In order to insert the zero-voltage phase using the up-down count of carrier, the assumed phase  $\alpha$  and  $\alpha_{pr}$  are needed to be converted to carrier count as (27),

$$\begin{cases} \alpha_{cnt} = \alpha/\pi \times c \\ \alpha_{pr\_cnt} = \alpha_{pr}/\pi \times c \end{cases}$$
(27)

where,  $\alpha_{cnt}$  and  $\alpha_{pr\_cnt}$  are converted value to carrier count form angle. *c* is the peak value of carrier counter in the digital controller. The base point of counters are set at the point of *Y* and *Z* in Fig.10, i.e. just after the dc offset in the inductor current is eliminated. Next, zero-voltage periods are inserted when the zero-voltage-insert counter  $\alpha_{cnt}$  and  $\alpha_{pr\_cnt}$ becomes zero with the countdown by a clock. In the first step, the A phase-carrier counter  $A_{cnt}$  and R phase-carrier counter  $R_{cnt}$  are changed into 0.5 in order to insert zerovoltage phases by turned on S<sub>1</sub> and S<sub>5</sub>. Thus, the transient magnetizing current keeps up that of the two-level peak, i.e. the adjustment of the magnetizing current peak. After the first step, A and U phase-carrier counter  $A_{cnt}$  and  $R_{cnt}$  are adjusted in order to prevent the error of the phase difference. The phase difference error due to first step is avoided by



Fig. 12. Assumption of the peak value of three-level magnetizing current. returning the manipulated amount of carrier count of the first step. Manipulated amounts of A and U phase-carrier counter  $\Delta A_{cnt}$  and  $\Delta R_{cnt}$  are expressed as (28),

$$\Delta A_{cnt} = A_{cnt\_step1} - 0.5$$
  

$$\Delta R_{cnt} = R_{cnt\_step1} - 0.5$$
(28)

where  $A_{cnt\_step1}$  and  $R_{cnt\_step1}$  are the value of phase-shift carrier counter when the zero voltage counter  $\alpha_{cnt}$  and  $\alpha_{pr\_cnt}$ become zero. In addition,  $\Delta R_{cnt}$  and  $\Delta A_{cnt}$  are the difference between 0.5 and  $A_{cnt}$  and  $R_{cnt}$ . According to (28), each carrier counter is adjusted as (29),

$$A_{cnt\_step 2} = A_{cnt\_step 1} - \Delta A_{cnt}$$

$$R_{cnt\_step 2} = R_{cnt\_step 1} - \Delta R_{cnt}$$
(29)

where,  $A_{cnt\_step2}$  and  $R_{cnt\_step2}$  are the value of the counter of A and U phase-shift carrier at the second step. The error of phase difference due to first step is avoided by calculating as (29) when the carrier counters reach 0.5. Consequently, the three-level operation is changed to the two-level operation without introducing any dc offsets into both the inductor current and the magnetizing current.

#### B. Mode-change from three-level mode to two-level mode

Fig. 12 shows the assumption of the peak value of the three-level magnetizing current in order to eliminate the dc offset in the magnetizing current when the operation mode is changed from the three-level to the two-level mode. Unlike the mode-change from the two level operation, the dc offset in the inductor current is eliminated by utilizing the clamping of the inductor current. In addition, the carrier count value is not needed to adjust carrier value in the second step in the changing mode from two-level to three-level. Therefore, the dc offset in the magnetizing current is eliminated in a switching period. The current value of the point B in Fig. 12 is needed to assume the timing of inserting the zero voltage phase. The value of the point B is determined by the zero voltage phase  $\beta$  that depends on the amounts of the phaseshift of R-phase carrier between the mode-change. The zero voltage phase  $\beta$  is given by (30) using (2) and considering the lagging due to dead-time influence[12],

$$\beta = 0.5(\delta_{2Lv} - \delta_{3Lv}) + \varepsilon - 0.5\delta_{dt}$$
(30)

where,  $\delta_{2L\nu}$ ,  $\delta_{3L\nu}$  and  $\varepsilon$  are the phase difference of the twolevel mode, the phase difference of the three-level mode and the zero voltage phase of the three level mode. According to (30), the current value of the point B is expressed by (31),

$$i_{m_{B}} = -\frac{V_{out}}{\omega L_{m}} \left[ \pi - \left\{ 0.5 (\delta_{2L\nu} - \delta_{3L\nu}) + \varepsilon - \delta_{dt} \right\} \right] + \frac{V_{out}}{2\omega L_{m}} \pi$$

$$= -\frac{V_{out}}{2\omega L_{m}} \left( \pi - \delta_{2L\nu} + \delta_{3L\nu} + \delta_{dt} - 2\varepsilon \right)$$
(31)

From (31), the transient magnetizing current  $i_{m_{CD}}$  between the point C and D is introduced by (32),

$$i_{m_{-}CD} = \frac{V_{out}}{\omega L_m} \theta - \frac{V_{out}}{2\omega L_m} \left(\pi - \delta_{2Lv} + \delta_{3Lv} + \delta_{dt} - 2\varepsilon\right)$$
(32)

Therefore, the assuming angle  $\phi$  is given by (33) using (32) and the peak value of the three-level mode,

$$\frac{V_{out}}{2\omega L_m} (\pi - 2\varepsilon) = \frac{V_{out}}{\omega L_m} \varphi - \frac{V_{out}}{2\omega L_m} (\pi - \delta_{2L\nu} + \delta_{3L\nu} + \delta_{dt} - 2\varepsilon)$$

$$\varphi = 0.5 (2\pi - 4\varepsilon - \delta_{2L\nu} + \delta_{3L\nu} + \delta_{dt})$$
(33)

The dc offset in the magnetizing current is eliminated by inserting the zero voltage phase same as the three-level to two-level mode using assumed angle  $\phi$ .

#### V. EXPERIMENTAL RESULTS

Table I shows the experimental parameters. A 2.5-kW prototype of the DAB converter is tested in order to confirm the validity of the proposed method for the transmission-power error with the dc offset elimination. In this experimental parameters, the three-level mode I is applied when the reference transmission power is between 0p.u and 0.2p.u. The three-level mode II is also applied when the transmission power is between 0.2p.u and 0.6p.u.

Fig. 13 shows the operation waveforms with the twolevel operation and the three-level operation. The voltagepolarity-reversal phenomenon occurs with the 47.6% error of the transmission power when conventional two level mode is applied. In contrast, by applying the proposed method, the transmission power error is reduced by 45.6% without voltage-polarity-reversal phenomenon.

Fig. 14 shows the characteristics of the transmission power against the reference-transmission power. The transmission power at light load becomes 0 W because the



phase reference  $\delta$  is smaller than the dead-time-induced phase error  $\delta_{dt}$  when using only two-level operation. By applying the three-level operation, the transmission-power error at light load is significantly reduced compared to that of the two-level operation. This benefits both the transient response of the power control and the elimination of the dc offset when the operation mode alternates.

Fig. 15 shows the transient response of changing the operation mode from the three-level mode to the two-level mode. This changing mode is conducted when the transmission power is changed from 1.0 kW to 2.5 kW by a step change. Note that the steady state dc offset is included in the magnetizing current before the step change because of antisymmetric in the gate signals. No dc offset occurs in the



Fig.15 Transient response of changing operation mode from three-level mode to two level mode.



Fig. 16 Transient response of changing operation mode from two-level mode to three-level mode.

inductor current. Nevertheless, in the magnetizing current, the peak value of -1.3 A occurs due to the dc offset. In contrast, by applying the proposed method, the peak value of the magnetizing current is reduced by 34%. Furthermore, this dc offset is eliminated just after two switching periods.

Fig. 16 shows the transient response of changing the operation mode from the two-level mode to the three-level mode. The changing mode is operated when the transmission power is changed form 2.5 kW to 1.0 kW. Without the proposed method, the peak value of -0.96 A occurs in the magnetizing current at the transient state due to the dc offset. On the other hand, by applying the proposed method, the peak value of the magnetizing current is reduced by 56%. In this mode, this dc offset is eliminated within a switching period.

#### VI. CONCLUSION

This paper proposed the compensation method of transferred power error caused by dead-time with the dc offset elimination method at the mode changing operation in the DAB converter. The error of the transferred power was reduced by 80.7% because the voltage-polarity-reversal phenomenon was avoided. Moreover, the dc offset in the inductor current and the magnetizing current was eliminated by applying the proposed elimination method. In particular, the peak value of the magnetizing current at transient state is reduced by 56%.

In future work, the compensation method for the nonliner dead-time error under the condition of  $V_{in} \neq NV_{out}$  will be considered.

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