Reduction of DC-link Current Harmonics over Wide Power-Factor Range for Three-Phase VSI using Single-Carrier-Comparison Continuous PWM

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***Abstract*—This paper proposes a novel continuous PWM (CPWM) method to reduce DC-link current harmonics in voltage source inverters (VSIs) over wide range of load power factor. This modulation method contributes to a lifetime extension of smoothing capacitors in motor drive systems. Furthermore, a high cost digital hardware such as a field-programmable gate array (FPGA) is not necessary because this modulation is implemented with only one carrier. The DC-link current harmonics are reduced by shifting voltage references in every half control period to reduce a fluctuation of the DC-link current around its average value. Experimental results confirm that the application of the proposed CPWM reduces the DC-link current harmonics by 24.2% at most.**

Keywords—Motor drive system, DC-link capacitor, Inverter DC-link current harmonics, Continuous PWM

I. INTRODUCTION

Three-phase AC motors are widely used in both industrial and household applications [1-5]. A lifetime extension of the AC motor drive systems has been actively researched for a decade [6-11]. In general, electrolytic capacitors are employed as smoothing capacitors in a DC-link part of a PWM inverter due to their superior capacitance per volume ratio compared to film capacitors or ceramic capacitors. However, the AC motor drive system becomes less reliable due to the short lifetime expectancy of electrolytic capacitors. It is possible to extend the lifetime of the smoothing capacitors by reducing the dc-link current harmonics of voltage source inverters (VSIs).

So far, several modulation methods of VSI which reduce the DC-link current harmonics have been proposed [7-11]. With a space vector PWM (SVPWM) in [10], voltage space vectors are selected in order that the zero vector period is shortened to minimize the DC-link current harmonics. Furthermore, this SVPWM adapts to the variation of the load power factor by changing the voltage space vectors according to polarities of inverter output phase currents. However, the employment of the SVPWM leads to a constraint of digital hardware, i.e. the requirement of high cost hardware such as field-programmable gate array (FPGA).

As another approach to reduce the DC-link current harmonics, a new single-carrier-comparison discontinuous PWM (DPWM) has been proposed in [11]. In this DPWM, voltage references of the classic DPWM are shifted at both the positive-peak and negative-peak of a triangular carrier to reduce the DC-link current harmonics, and only one carrier is used for comparison. Thus, this DPWM can be implemented only with the general-purpose micro-computer. However, the DPWM strategy faces many challenging disadvantages compared to continuous PWM (CPWM); in particular, certain switch is clamped to on-state at all times. Therefore, load current continuously flows through the clamped switch and it leads to overheat in the switch depending on the conditions of modulation index and fundamental frequency. Furthermore, the number of switching per control period in the DPWM is less than that in the CPWM. This leads to an increase of the AC motor noises due to a high inverter output voltage harmonics. For the above reasons, the applications of the DPWM are limited.

This paper proposes a novel carrier-comparison CPWM which uses only one carrier to reduce the DC-link current harmonics. This modulation method contributes the lifetime extension of the smoothing capacitor in the motor drive system and can be implemented only with the general-purpose micro-computer. Three phase continuous voltage references are shifted in every half control period to reduce the fluctuation of the DC-link current around its average value. By optimizing the shifting manner of the voltage references, it is possible to reduce the DC-link current harmonics over entire region of the load power factor. One more contribution of this CPWM is to overcome the problems of the DPWM, such as heat concentration to specific switch and high inverter output voltage harmonics.

II. INVERTER DC-LINK CURRENT HARMONICS WITH CONVENTIONAL CONTINUOUS PWM

Fig. 1 shows the voltage references of CPWM and output phase currents at a modulation index of 0.7 and a load power factor of 0.707. Three phase voltage references $v^*_{x.CPWM}$ of the conventional CPWM are sine waves and expressed as [12]:

$$\begin{cases} v^*_{u.CPWM} = m \cdot \cos\left(2\pi ft\right) \\ v^*_{v.CPWM} = m \cdot \cos\left(2\pi ft - 2\pi/3\right) \\ v^*_{w.CPWM} = m \cdot \cos\left(2\pi ft + 2\pi/3\right) \end{cases} \quad (1)$$

where m is the modulation index, f is the fundamental frequency.

Fig. 2 shows zoomed-in waveforms of $v^*_{x.CPWM}$, switching functions and an ideal DC-link current at the modulation index of 0.7, a phase angle of 25 degrees and the load power factor

of 0.707. The DC-link current is the superposition summation of the switched current pulses from each leg and calculated as:

$$i_{DC.in} = \sum_{x=u,v,w} \left(s_x \times i_x \right). \tag{2}$$

The shaded area of the DC-link current waveform in Fig. 2 indicates the instantaneous root-mean-square (rms) value of the current flowing into the smoothing capacitor, which is calculated as:

$$i_{C.rms}\left(T_s\right) = \sqrt{i_{DC.in.rms}^2\left(T_s\right) - i_{DC.in\_ave}^2}$$

$$\text{and} \begin{cases} i_{DC.in.rms}\left(T_s\right) = \sqrt{\dfrac{1}{T_s}\int_0^{T_s} i_{DC.in}^2 dt} \\ i_{DC.in\_ave} = \dfrac{3}{4} m \cdot I_m \cos\varphi \end{cases} \tag{3}$$

where T_s is the control period, I_m is the maximum value of the output phase current and φ is the load power factor angle. Note that a smaller fluctuation of the DC-link current around its average value results in a smaller rms value of the smoothing capacitor current [13]. In the case of conventional CPWM, the center of the gate pulses are the same as the center of the control period, which results in the longest overlap period of the gate pulses. This leads to the large fluctuation of the DC-link current around its average value, i.e. the high DC-link current harmonics.

III. Proposed PWM Method to Reduce DC-link Current Harmonics of VSI

It is obvious from (2) and (3) that the DC-link current harmonics are highly influenced by the switching functions and output phase currents, i.e. the load power factor. Therefore, the proposed CPWM reduces the DC-link current harmonics by shifting output voltage references in every half control period and adjusting the location of the gate pulses in the control period. Furthermore, the proposed shifting rule of the voltage references changes depending on whether the polarities of the voltage references and the output phase currents are equal or not. In other words, the proposed modulation method can adapt the variation of the load power factor.

A. When Polarities of Voltage References and Output Phase Currents are Equal

In this section, the proposed shifting rule of the voltage references to reduce the DC-link current harmonics is introduced in case when the polarities of the voltage references and output phase currents are equal. In particular, the overlap period between the sector I ($v^*_{u.CPWM} > 0$, $v^*_{v.CPWM} < 0$, and $v^*_{w.CPWM} < 0$) and sector A ($i_u > 0$, $i_v < 0$, and $i_w < 0$), i.e. the phase angle period between 15~30 degrees in Fig. 1, is demonstrated as an example.

Fig. 3 shows the zoomed-in waveforms of the voltage references of the proposed CPWM, the switching functions, and the ideal DC-link current at the modulation index of 0.7, the phase angle of 25 degrees, and the load power factor of 0.707. Note that the proposed voltage references are realized based on the premise that the references can be updated at both

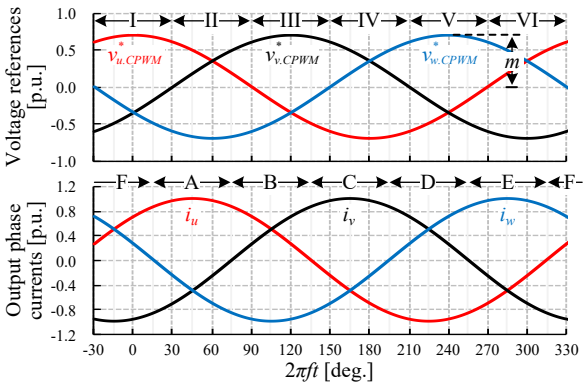

Fig. 1. Continuous voltage references and output phase currents at m = 0.7, cos φ = 0.707. The sectors I-VI and A-F are determined by the polarities of three-phase voltage references and output phase currents, respectively.

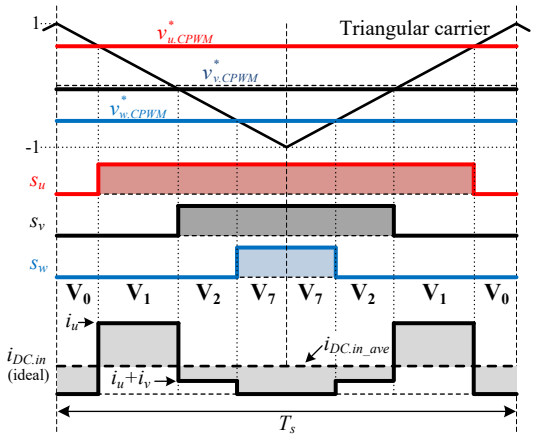

Fig. 2. Zoomed-in waveforms of voltage references of conventional CPWM $v^*_{x.CPWM}$, switching functions, and ideal $i_{DC.in}$ at m = 0.7, $2\pi ft$ = 25 deg., and cos φ = 0.707.

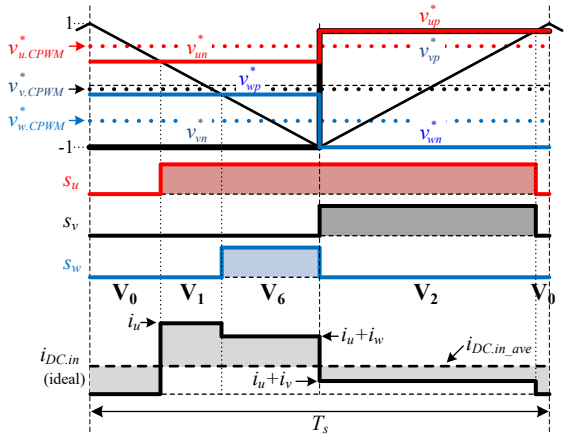

Fig. 3. Zoomed-in waveforms of voltage references of proposed CPWM $v^*_{x.PCPWM}$, switching functions, and ideal $i_{DC.in}$ at m = 0.7, $2\pi ft$ = 25 deg., and cos φ = 0.707. The divergence degree coefficients between the original voltage references and shifted references are set as A_u = 1.68, A_v = 2.00, and A_w = 2.00.

the positive-peak and negative-peak of the triangular carrier with the general-purposed micro-computer. The proposed voltage references are generated by shifting the original continuous voltage references alternately to positive-side and negative-side in every half control period as:

$$\begin{cases} v^*_{xp} = (2 - A_x)\cdot v^*_{x.CPWM} + A_x - 1 \\ v^*_{xn} = A_x \cdot (v^*_{x.CPWM} - 1) + 1 \end{cases} \quad (\text{if } v^*_{x.CPWM} \geq 0)$$
$$\begin{cases} v^*_{xp} = A_x \cdot (v^*_{x.CPWM} + 1) - 1 \\ v^*_{xn} = (2 - A_x)\cdot v^*_{x.CPWM} - A_x + 1 \end{cases} \quad (\text{if } v^*_{x.CPWM} < 0) \quad (4)$$

where v^*_{xp} is the positively-shifted voltage reference, v^*_{xn} is the negatively-shifted voltage reference, and A_x is the divergence degree coefficient between the original voltage references and shifted references. To reduce the DC-link current harmonics, first, the phase of which polarity is different from the other two phases' polarity, i.e. the *u*-phase in Fig. 3 for example, is focused. When only the *u*-phase current is positive as in Fig. 3, the *u*-phase voltage reference must be the maximum at all times during the control period in order to avoid the switching patterns which lead the large fluctuation of the DC-link current around its average value. Therefore, the *u*-phase voltage reference is shifted simultaneously with the larger phase voltage reference between the other two phases, i.e. the *v*-phase in Fig. 3. Besides, the overlap of the other two phase gate pulses must be shortened in order to reduce the fluctuation of the DC-link current around its average value. Thus, the other two phase voltage references are shifted alternately and maximally as long as they do not exceed the *u*-phase voltage reference.

Note that the divergence degree coefficient A_x between the original voltage references in the proposed CPWM can be calculated based on (4) and the shifting rule of the voltage references. This calculation might be a heavy computation load for the general-purposed micro-computer and thus should not be processed online. It is recommended to calculate these coefficients offline in advance.

B. *When Polarities of Voltage References and Output Phase Currents are Unequal*

Fig. 4 shows the zoomed-in waveforms of the voltage references, the switching functions, and the ideal DC-link current at the modulation index of 0.7, the phase angle of -20 degrees, and the load power factor of 0.707 in the case of the conventional CPWM and the proposed CPWM, respectively. The overlap period between the sector I ($v^*_{u.CPWM} > 0$, $v^*_{v.CPWM} < 0$, and $v^*_{w.CPWM} < 0$) and sector F ($i_u > 0$, $i_v < 0$, and $i_w > 0$), i.e. the phase angle period between -30~15 degrees in Fig. 1, is demonstrated as an example of the case when the polarities of the voltage references and output phase currents are not equal. Similar to the above section, the phase of which polarity is different from the other two phases' polarities, i.e. the *v*-phase in Fig. 4, is focused to reduce the DC-link current harmonics. When only the *v*-phase current is negative as in Fig. 4, the *v*-phase voltage reference must be the minimum at all times during the control period in order to avoid the switching patterns which lead the large fluctuation of the DC-link current around its average value. Therefore, the *v*-phase voltage reference is shifted simultaneously with the smaller phase voltage reference between the other two phases, i.e. the *w*-phase in Fig. 4. Besides, the overlap of the other two phase gate pulses must be also shortened in order to reduce the fluctuation of the DC-link current around its average value. Thus, the other two phase voltage references are shifted alternately and maximally as long as they do not become smaller than the *v*-phase voltage reference.

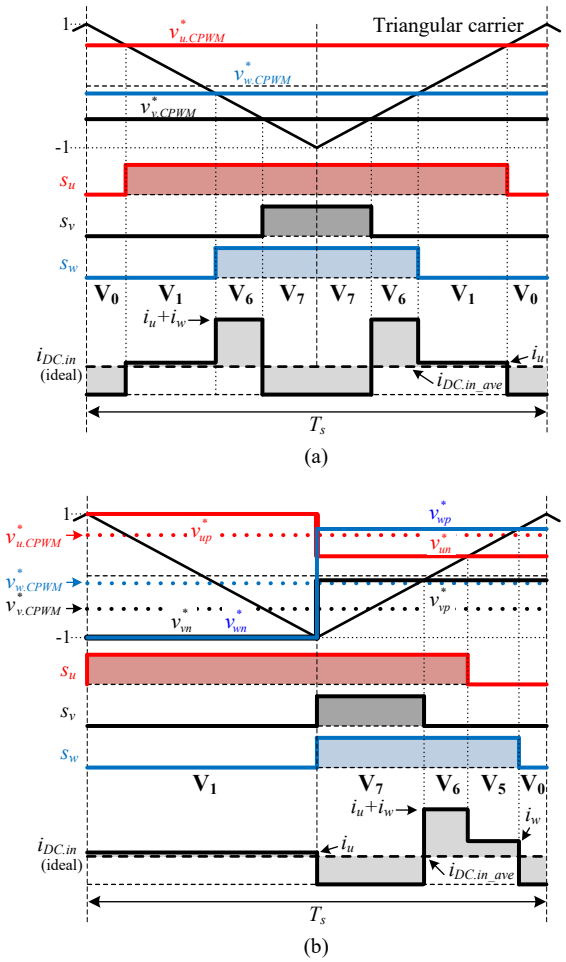

Fig. 4. Zoomed-in waveforms of voltage references, switching functions, and ideal $i_{DC.in}$ at $m = 0.7$, $2\pi ft$ = -20 deg., and cos $\varphi = 0.707$ (a) conventional CPWM (b) proposed CPWM with $A_u = 2.00$, $A_v = 2.00$, and $A_w = 2.00$.

On the other hand, at the phase angle period between 0~15 degrees in Fig. 1, the *v*-phase voltage reference could not be the minimum and the shifted voltage references generate the switching patterns which worsen the DC-link current harmonics. Therefore, the conventional CPWM is applied at these periods.

C. *Dead-time Consideration*

Fig. 5 shows the zoomed-in waveforms of the voltage references of the proposed CPWM, the switching functions, and the DC-link current with the consideration of the dead-time under the same conditions as in Fig. 3. During the dead-time period, especially from the falling edge of s_u and s_v, the large fluctuation of the DC-link current occurs.

Fig. 6 shows the zoomed-in waveforms of the modified voltage references of the proposed CPWM, the switching functions, and the DC-link current with the consideration of the dead-time under the same conditions as in Fig. 3. The *v*-phase divergence degree coefficient A_v is modified to insert the dead-time width margin between the falling edges of the s_u and s_v. In this manner, dead-time width margin at the position where gate pulse edges match is necessary for an avoidance of the large fluctuation of the DC-link current.

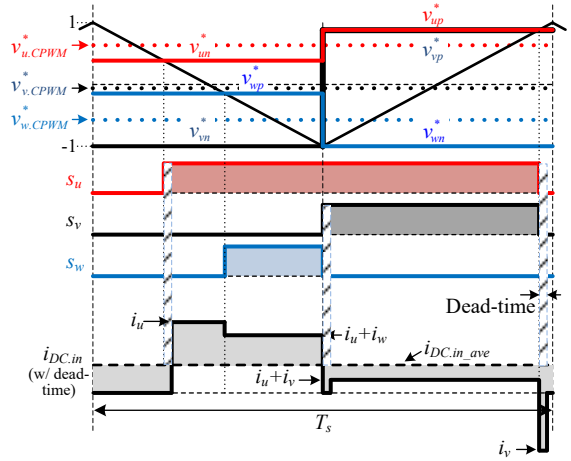

Fig. 5. Zoomed-in waveforms of voltage references of proposed CPWM $v^*_{x.PCPWM}$, switching functions, and $i_{DC.in}$ with consideration of dead-time at m = 0.7, $2\pi ft$ = 25 deg., and cos φ = 0.707 (under same conditions as in Fig. 3). The divergence degree coefficients are set as A_u = 1.68, A_v = 2.00, and A_w = 2.00.

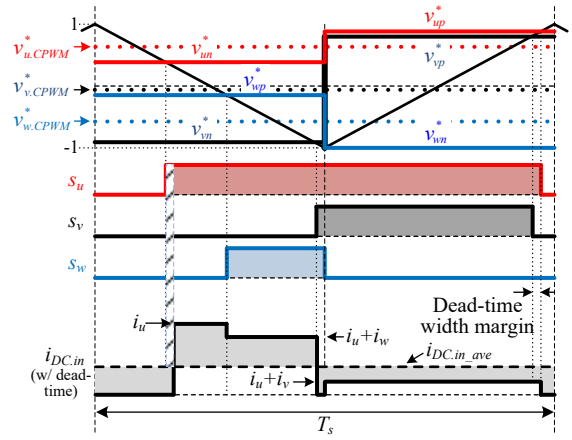

Fig. 6. Zoomed-in waveforms of modified voltage references of proposed CPWM $v^*_{x.PCPWM}$, switching functions, and $i_{DC.in}$ with consideration of dead-time at m = 0.7, $2\pi ft$ = 25 deg., and cos φ = 0.707 (under same conditions as in Fig. 3). The v-phase divergence degree coefficient A_v is changed from 2.00 to 1.96 in order to insert the dead-time width (1% of T_s) margin between the falling edges of the s_u and s_v.

D. Load Current Quality

In order to evaluate the load current quality, the concept of harmonic flux presented in [14] is used. When the switching frequency model of the load motor is assumed as an inductance L, the harmonic load current vector $\mathbf{I_h}$ has a proportional relationship between the harmonic flux vector $\boldsymbol{\lambda_h}$ (time integral of the instantaneous error voltage vector), as:

$$\boldsymbol{\lambda}_\mathbf{h} = L\mathbf{I}_\mathbf{h} = \int_{NT_s}^{(N+1)T_s} \left(\mathbf{V}_\mathbf{k} - \mathbf{V}^*\right) \cdot dt \qquad (5)$$

where $\mathbf{V_k}$ (k = 0~7) is the output voltage space vector of the VSI, and $\mathbf{V}^*$ is the voltage reference vector, respectively.

Fig. 7 shows the harmonic flux trajectories at the modulation index of 0.7, and the phase angle of 25 degrees. With the rms value of the harmonic flux, calculated as follows, the load current quality characterized by the modulator can be evaluated without any load information.

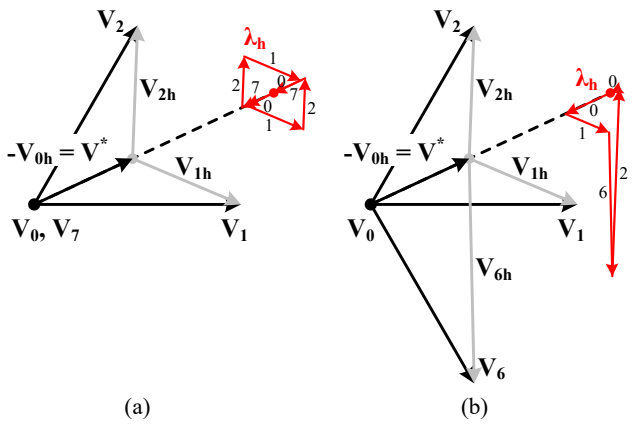

Fig. 7. Harmonic flux trajectories at m = 0.7, and $2\pi ft$ = 25 deg. (a) conventional CPWM (b) proposed CPWM.

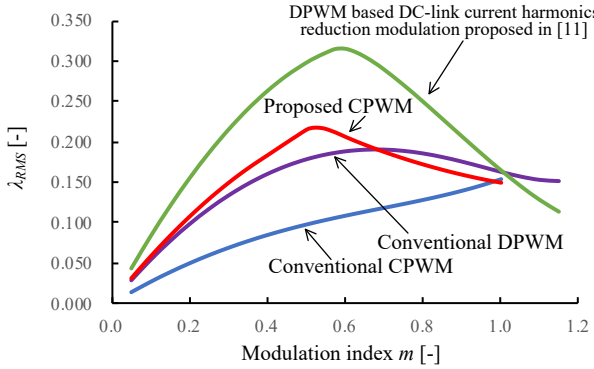

Fig. 8. Comparison of harmonic flux rms values.
In the proposed CPWM calculations, the load power factor is set to 1.

$$\lambda_{RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\int_{NT_s}^{(N+1)T_s} \left\|\boldsymbol{\lambda}_\mathbf{h}\right\|^2 dt.d\theta}. \qquad (6)$$

Fig. 8 shows the harmonic flux rms values of several modulator. With the proposed CPWM, the VSI output voltage has large instantaneous voltage error between the voltage references, as shown in Fig. 7, as a result of the switching patterns to reduce the DC-link current harmonics. Therefore, the application of the proposed CPWM worsens the harmonic flux rms value compared to those with the conventional CPWM. On the other hand, the proposed CPWM is superior to the DPWM based DC-link current harmonics reduction modulation method proposed in [11].

IV. Simulation and Experimental Results

The performances of the conventional and proposed CPWM are verified in simulation and experiment. In the experiment, the three-phase VSI (7MBP50RA120, Fuji Electric Co., Ltd.) is operated at the switching frequency of 10 kHz. A three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.), the rated power of which is 3.7 kW, is used as a test motor.

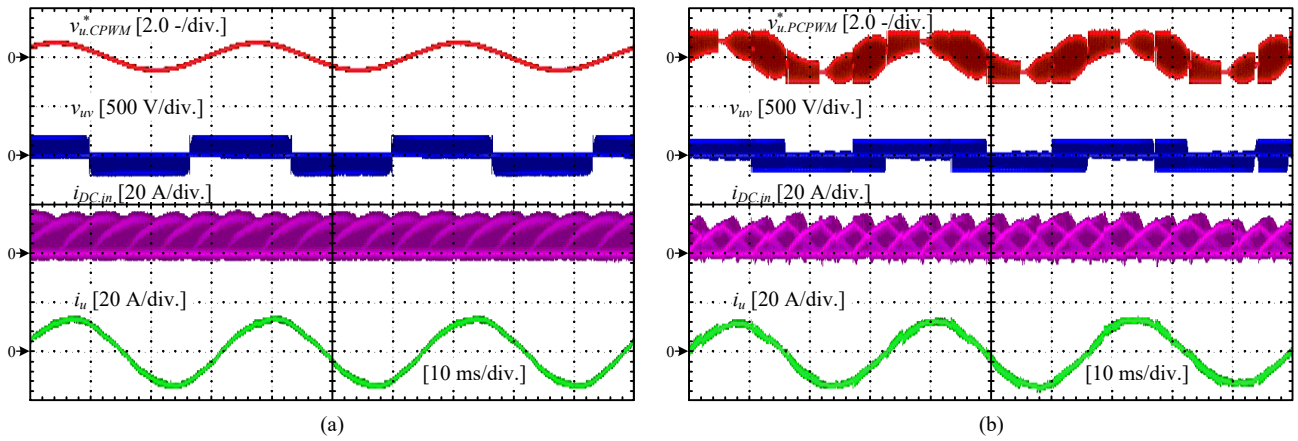

Fig. 9. *u*-phase voltage reference, line-to-line voltage, DC-link current, and output *u*-phase current at $m = 0.550$ and $\cos\varphi = 0.866$ (a) conventional CPWM (b) proposed CPWM.

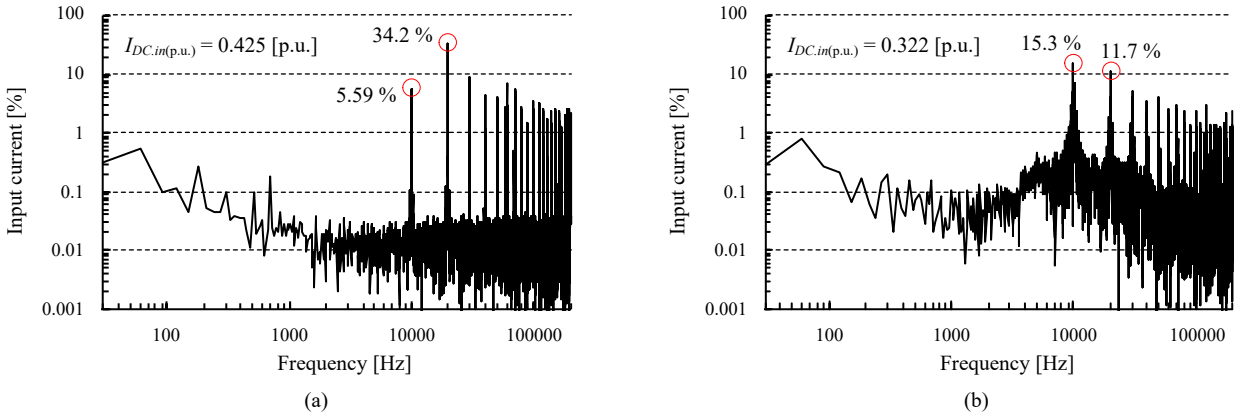

Fig. 10. Harmonic components of DC-link current at $m = 0.550$ and $\cos\varphi = 0.866$ (under same conditions as in Fig. 9) (a) conventional CPWM (b) proposed CPWM.

A. DC-link Current Harmonics

Fig. 9 shows the *u*-phase voltage reference, the line-to-line voltage, the DC-link current, and the output *u*-phase current with each modulation method at the modulation index of 0.550 and the load power factor of 0.866. When the load power factor is 0.866, both periods, where the polarities of the voltage references and output phase currents are equal or not equal, occurred. Note that the voltage references of the proposed CPWM are shifted in every half control period as shown in Fig. 9(b).

Fig. 10 shows the harmonic components of the DC-link current under the same conditions as in Fig. 9. The maximum value of the vertical axis (100%) indicates the maximum value of the output phase currents. Even though the employment of the proposed CPWM worsens the 1st switching-frequency harmonic component of the DC-link current, the integer multiple components of the switching frequency are reduced compared to those with the conventional CPWM. Consequently, the proposed CPWM reduces the DC-link current harmonics by 24.2%. Note that the DC-link current harmonics is evaluated as $I_{DC.in(p.u.)}$, which is the rms value of the DC-link current ($i_{DC.in.rms}$) normalized by the maximum value of the output phase current.

$$I_{DC.in(p.u.)} = \frac{i_{DC.in.rms}}{I_m} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(\frac{1}{\sqrt{2}} i_{DC.in.n}\right)^2} \qquad (7)$$

where n is the harmonic order and $i_{DC.in.n}$ is the n-order component of the DC-link current harmonics. The harmonic components of the DC-link current up to 20th-order of the switching frequency are considered in this evaluation.

Fig. 11 shows the VSI operating waveforms at the modulation index of 0.550 and the load power factor of 0.643, i.e. low load power factor condition. When the load power factor is 0.643, the period where the polarities of the voltage references and output phase current are not equal is longer compared to that at the load power factor of 0.866. Furthermore, the periods where the proposed shifted voltage references are not adequate for reduction of the DC-link current harmonics arise. Therefore, the conventional sinusoidal voltage references are partially applied in these periods.

Fig. 12 shows the harmonic components of the DC-link current under the same conditions as in Fig. 11. The proposed CPWM reduces the DC-link current harmonics by 10.2%. These results demonstrate that the proposed CPWM is effective in terms of reducing the DC-link current harmonics, even when the load power factor is low.

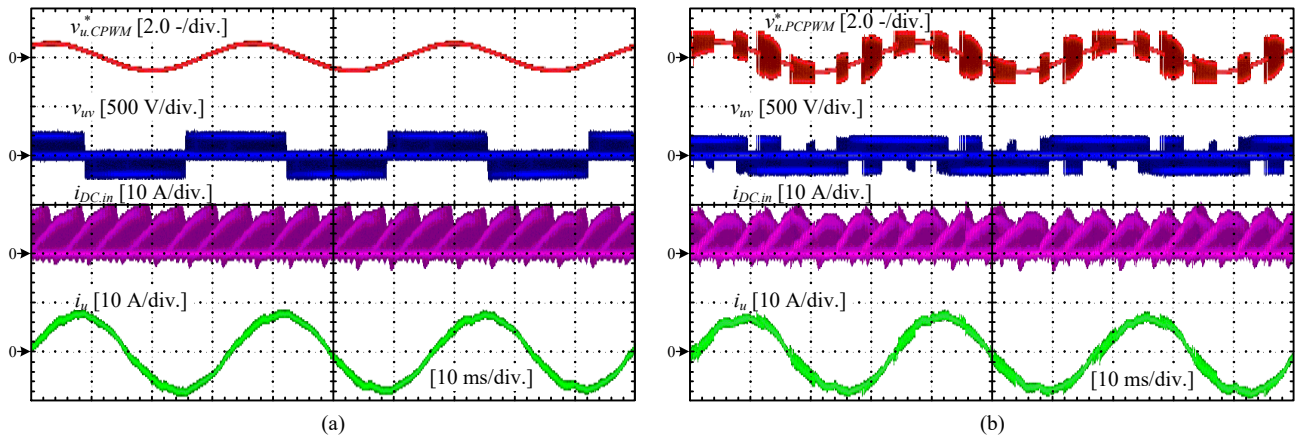

Fig. 11. u-phase voltage reference, line-to-line voltage, DC-link current, and output u-phase current at m = 0.550 and cos φ = 0.643, i.e. low load power factor condition (a) conventional CPWM (b) proposed CPWM.

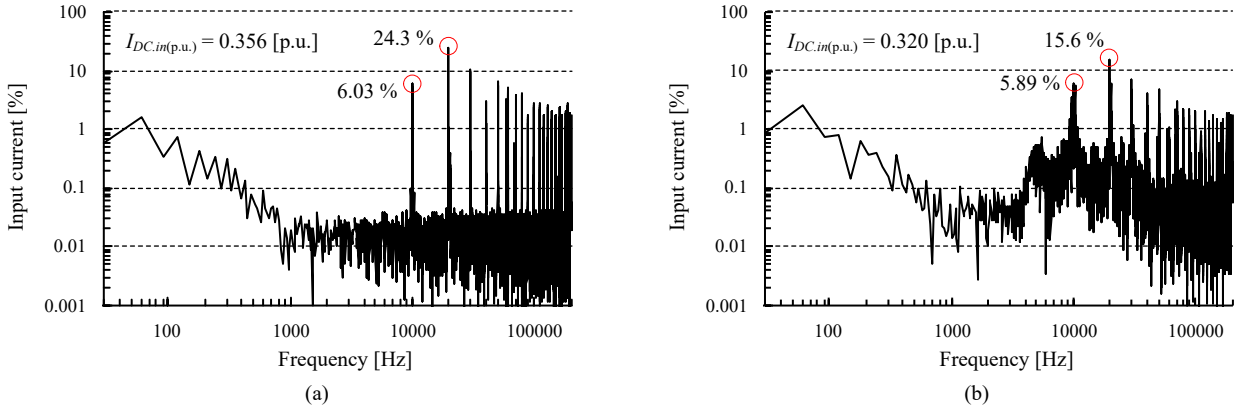

Fig. 12. Harmonic components of DC-link current at m = 0.550 and cos φ = 0.643 (under same conditions as in Fig. 11) (a) conventional CPWM (b) proposed CPWM.

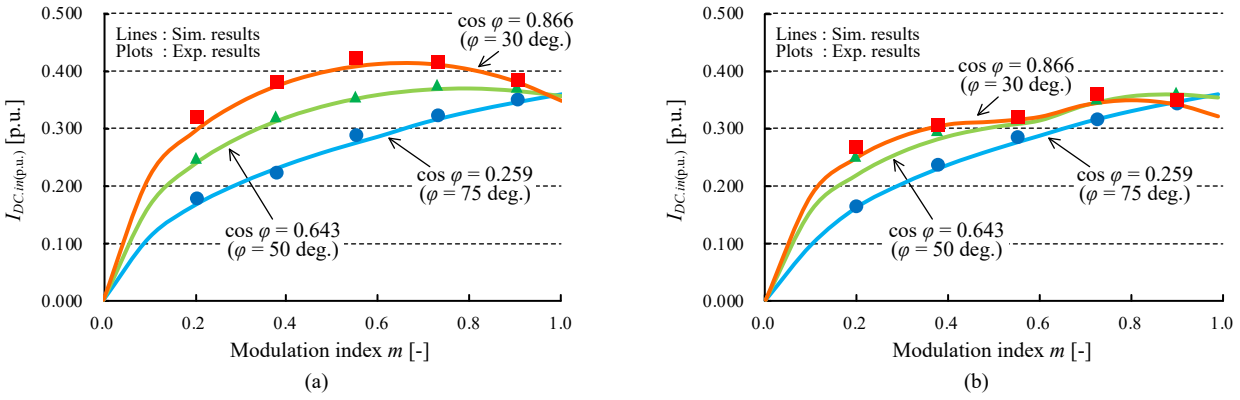

Fig. 13. Simulation and experimental results of DC-link current harmonics (a) conventional CPWM (b) proposed CPWM.

Fig. 13 shows the simulation and experimental results of the DC-link current harmonics at the load power factor from 0.259 to 0.866. The proposed CPWM reduces the DC-link current harmonics under any conditions of the modulation index and the load power factor. A higher load power factor enables a greater reduction effect on the DC-link current harmonics to be obtained.

B. Output Phase Current Harmonics

Fig. 14 shows the total harmonic distortion (THD) of the output u-phase current at the load power factor of 0.866. The harmonic components up to 40th-order of the fundamental frequency are considered in this evaluation. These characteristics are similar to the analytic results of the harmonic flux rms value shown in Fig. 8. The application of

the proposed CPWM leads to higher distortion of the output phase current compared to those with the conventional CPWM. Nevertheless, those THD with the proposed CPWM is superior to those with the DPWM based DC-link current harmonics reduction modulation method proposed in [11], and the almost same level of those with the conventional DPWM method.

V. Electrolytic Capacitor Lifetime Comparison

The expected lifetime of the electrolytic capacitor can be calculated as the multiplication of the specified lifetime (L_o) on the manufacturer catalog by three acceleration rates which are dependent on the ambient temperature (F_T), the ripple current (F_I), and the applied voltage (F_V) [15]. In this evaluation, only the acceleration according to the ripple current F_I is considered, and the other two factors are assumed as 1.

Table I shows the frequency coefficient (K_f) of the rated ripple current flowing through the aluminum electrolytic capacitor (RWF series, Nippon Chemi-Con Corp. [16]), which is used in the laboratory setup. With the consideration of the frequency dependency of the equivalent series resistance (ESR) in the aluminum electrolytic capacitors, the DC-link current harmonics can be recalculated for the lifetime estimation as:

$$I_{DC.in.freq(\text{p.u.})} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(\frac{1}{\sqrt{2}}\cdot\frac{i_{DC.in.n}}{K_f}\right)^2}. \qquad (8)$$

Fig. 15 shows the harmonic components of the DC-link current considering the frequency dependency of the ESR in the aluminum electrolytic capacitor at the modulation index of 0.550, and the load power factor of 0.866 (under the same conditions as in Figs. 9-10). The application of the proposed CPWM reduces the DC-link current harmonics $I_{DC.in.freq(\text{p.u.})}$ by 24.2% even when the frequency dependency of the ESR in the electrolytic capacitor is considered. Assuming that the load motor is mostly operated at the modulation index of 0.550 and the load power factor of 0.866, and the embedded electrolytic capacitors in the VSI modulated by the conventional CPWM is designed at the worst case of the rated ripple current, i.e. F_I as 1, the lifetime expectancy L_n of the electrolytic capacitors can be given by

$$\begin{aligned} L_{n\_conv.CPWM} &= L_o \cdot F_I = L_o \times 1 = 5\,000 \text{ h} \\ L_{n\_prop.CPWM} &= L_o \cdot F_I = L_o \times 1.34 = 6\,700 \text{ h} \end{aligned} \qquad (9)$$

where L_o is 5000 hours in case of the aluminum electrolytic capacitor (RWF series, Nippon Chemi-Con Corp. [16]).

Note that the above lifetime calculation is just an example. However, it can be concluded that the application of the proposed CPWM might extend the lifetime of the electrolytic capacitor about 1.34 times longer at most than that with the conventional CPWM.

VI. Conclusion

This paper proposed the novel CPWM to reduce the DC-link current harmonics of VSI over entire load power factor range. The proposed CPWM contributed to the lifetime extension of the smoothing capacitors in the motor drive systems. Furthermore, high cost hardware such as FPGA was not necessary because this modulation method could be implemented with only one triangular carrier. The DC-link current harmonics were reduced by shifting the voltage references in every half control period to reduce the fluctuation of the DC-link current around its average value.

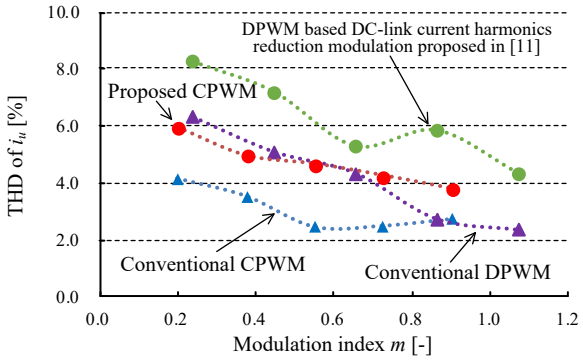

Fig. 14. THD of output u-phase current i_u at cos φ = 0.866.

TABLE I. Frequency Coefficient of Rated Ripple Current Flowing through Aluminum Electrolytic Capacitors (RWF Series, Nippon Chemi-Con Corp. [16])

Frequency [Hz]	50	120	300	1 k	3 k or more
Coefficient K_f	0.80	1.0	1.1	1.3	1.4

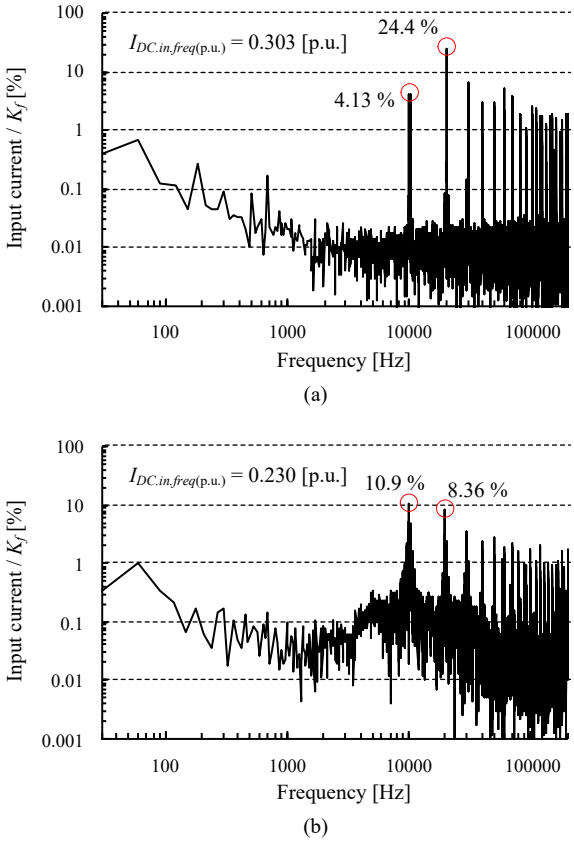

Fig. 15. Harmonic components of DC-link current considering frequency dependency of ESR in aluminum electrolytic capacitor at m = 0.550, and cos φ = 0.866 (under same conditions as in Figs. 9-10)
(a) conventional CPWM (b) proposed CPWM.

The analytical results of the harmonic flux rms values confirmed that the proposed CPWM achieved the same level of the load current quality as the conventional DPWM. In addition, the experimental results confirmed that the application of the proposed CPWM reduced the DC-link current harmonics by 24.2% at most even when the frequency dependency of the ESR in the electrolytic capacitor was considered. As a result of the capacitor lifetime estimation, the 24.2% reduction of the DC-link current harmonics might extend the lifetime of the electrolytic capacitor about 1.34 times longer at most than that with the conventional CPWM.

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