Passive-Damped *LCL* Filter Optimization for Single-Phase Grid-Tied Inverters Operating in both Continuous and Discontinuous Current Mode

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***Abstract*— This paper proposes a filter design method for a passive-damped *LCL* filter in single-phase grid-tied inverters operating in both continuous current mode (CCM) and discontinuous current mode (DCM). Low-inductance filters leads to two main problems: zero-crossing current distortions and filter resonance at weak power grid. An operation in both CCM and DCM is introduced to eliminate the zero-crossing current distortions. Meanwhile, a design flow chart is proposed to show step-by-step how to design the *LCL* filter based on root loci. Current control performances are compared between a well-known proportional-resonant (PR) controller employed with the only-CCM operation, and the PI controller with the proposed CCM/DCM operation. A 4-kW prototype is constructed in order to analyze the control performance. Compared to the conventional CCM control, the proposed CCM/DCM control reduces the current total harmonic distortion (THD) by 75.9%. Even at weak power grid (i.e. a high grid inductance of 2000 μH), the proposed control can obtain a low current THD of 0.8% with the filter inductance reduced to only 160 μH, which is 0.5% of the total inverter impedance.**

Keywords—single-phase grid-tied inverter, continuous current mode, discontinuous current mode, linearization, digital control

I. INTRODUCTION

In grid-tied inverters for photovoltaic systems, a filter is generally required in order to suppress current harmonics and meet grid current harmonic constraints as defined by standards such as IEEE 1547 [1]. *LCL* filters are usually preferred to conventional *L* filters because they can obtain effective switching harmonic attenuation with lower inductance requirement. Nevertheless, the low-inductance *LCL* filter might introduce two main problems to the current control; zero-crossing current distortions and the well-known resonance issue [2]-[4].

The reduction of the inductance leads to a design of a high switching current ripple due to a high dc-link voltage to inductance ratio. This high current ripple results in a current distortion phenomenon called zero-current clamping, which implies the operation of the inverter changes from continuous current mode (CCM) to discontinuous current mode (DCM) around zero-current crossing points [4]. A strong nonlinear behavior of DCM significantly worsens a current control performance, inducing the zero-crossing current distortion [5]. Many DCM nonlinearity compensation methods have been proposed to deal with this problem [6]-[11]. However, the common issue with these conventional methods is that the DCM nonlinearity compensation is dependent on the inductance. When plant mismatch or parameter variation occurs, the current distortion reduction is no longer guaranteed.

On the other hand, the closed-loop current controller design considering the resonance in *LCL* filters becomes more challenging over a wide variation range of grid inductance. The most straightforward way to deal with the *LCL* resonance is to connect a damping resistor in series with the capacitor of the *LCL* filter. Although this method can easily achieve a stable current control over a wide frequency range, decreased high frequency attenuation and high damping loss are undesired drawbacks [2]. Meanwhile, the *LCL* filter with a shunt RC provides a better solution with lower damping loss and good high frequency attenuation [3]. Nevertheless, it has not been reported a filter design considered the DCM operation of the inverter around the current zero-crossing points, which greatly affects the control stability.

This paper proposes a filter design method for a passive-damped *LCL* filter in single-phase grid-tied inverters operating in both CCM and DCM. The zero-crossing current distortion is alleviated by the DCM operation of the inverter around the current zero-crossing points. In particular, an inductance-independent DCM nonlinearity compensation method is introduced in order to control the inverter with the same PI controller designed in CCM [12]. Instead of using the inductance for the calculation of the DCM nonlinearity compensation, a duty ratio at a previous computation period is used to estimate the DCM nonlinearity. On the other hand, a design flow chart is proposed to show step-by-step how to design the passive-damped *LCL* filter based on root loci of closed-loop current control considering the variation of the

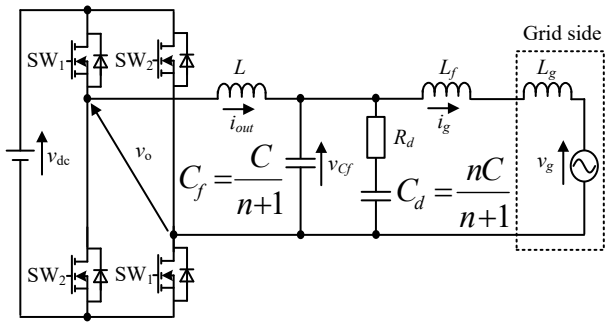


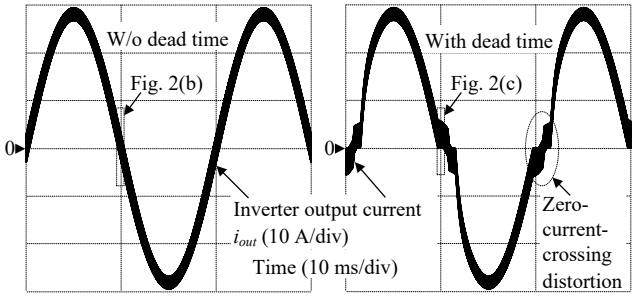
Fig. 1. Single-phase grid-tied inverter. An H-bridge inverter with a passive-damped *LCL* filter is analyzed due to its simple configuration, which provides high fault-tolerant reliability.

grid inductance. In particular, a well-known proportional-resonant (PR) controller employed with the only-CCM operation, and the PI controller with the proposed CCM/DCM operation are analyzed in order to compare the achievable stability in case when the inductance of the *LCL* filter is extremely reduced. The original idea of this paper is that the utilization of the duty ratio at the previous computation period is to make the DCM nonlinearity compensation inductance-independent, whereas the filter design based on the root loci can achieve the most reliable stability with the smallest reducible filter volume. This paper is organized as follows: in section II, the problems with the increasing grid current THD due to the zero-crossing distortion is explained. Next, in section III, the derivation of the CCM/DCM current control based on the PI controller is demonstrated. Then, in section IV, the filter design flowchart for the passive-damped *LCL* filter in single-phase grid-tied inverters operating in both CCM and DCM. Finally, in section V, the operation of the proposed CCM/DCM control is analyzed with several designs of the *LCL* filter.

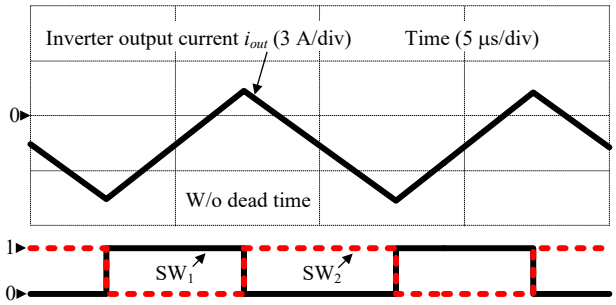
II. Zero-Crossing Distortion

Fig. 1 depicts the circuit configuration of the single-phase grid-tied inverter. Although many DC/AC converter topologies such as, e.g. modular multilevel converters or flying capacitor multilevel converters, have been proposed for the grid-tied inverter, a typical H-bridge inverter is analyzed due to its simple configuration, which provides high fault-tolerant reliability [13]-[16]. The *LCL* filter is used as an interface between the inverter and the grid in order to suppress the current harmonics of the inverter output current i_{out}. Compared to *L* filters or *LC* filters, the *LCL* filter can obtain effective switching harmonics attenuation with lower inductance requirements. However, the low-inductance *LCL* filter design significantly increases the zero-current-crossing distortion; that cannot satisfy the grid current harmonic constraints.

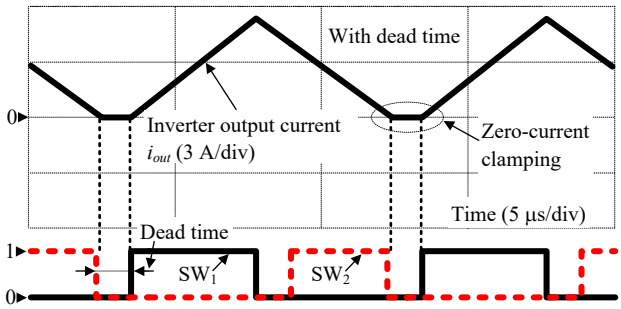
Fig. 2 describes the zero-crossing distortion and comparison of open-loop gains between CCM and DCM. As shown in Fig. 2(a) and 2(b), when a dead time is not in use, the inverter output current flows continuously over entire a switching period; hence, a sinusoidal current waveform is obtained. However, the zero-current clamping phenomenon occurs during the dead-time interval when the dead-time is



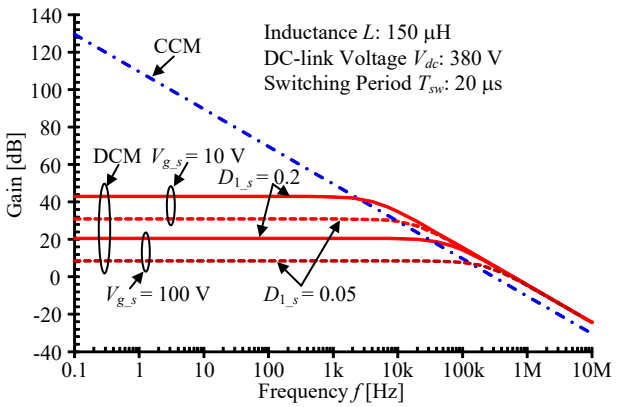
(a) Inverter output current w/o dead time and with dead time



(b) Zoom-in current and switching signals w/o dead time



(c) Zoom-in current and switching signals with dead time



(d) Bode diagram of duty-ratio-to-current transfer function for CCM and DCM.

Fig. 2. Zero-current-crossing distortion and comparison of open-loop gain between CCM and DCM. The dead-time causes the zero-current clamping phenomenon in the vicinities of the zero-current crossing, which changes the inverter operation from CCM to DCM. The low current loop gain in DCM worsens the current response and causes the zero-current-crossing distortion. Note that the long dead-time is employed for better illustration.

applied in order to avoid an instantaneous turn-on of both two switching devices in one leg as shown in Fig. 2(a) and

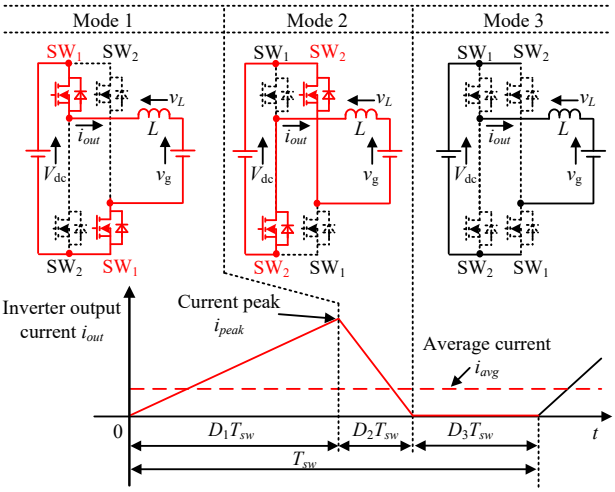


Fig. 3. Current path and inverter output current waveform in DCM when the grid voltage is positive. The zero current interval D_3T_{sw} occurring in DCM introduces the nonlinearities into the transfer function.

2(c). Due to this phenomenon, the inverter operation mode changes from CCM to DCM, which exhibits a nonlinear duty-ratio-to-current transfer function [5]. In particular, as shown in Fig. 2(d), the frequency corresponding to the pole of DCM is certainly much higher than the cutoff frequency of the current control loop [6]. Consequently, the open loop gain in DCM is much lower than in CCM. This worsens the current response in DCM if the same controller as in CCM is employed in DCM. As a result, the current distorts when the circuit mode changes from CCM to DCM due to the employment of the dead time.

III. CONTROLLER DESIGN

In this section, first the DCM nonlinearity compensation and the control system for the operation in only DCM is introduced. Then, the control system for the inverter operating in both continuous current and discontinuous current is explained. Finally, the controller parameter design is demonstrated.

A. Discontinuous-current-mode nonlinearity compensation

Fig. 3 depicts the current path and the inverter output current waveform in DCM when the grid voltage is positive. The filter inductor L_f and the filter capacitor C_f are omitted due to the simplification. In order to derive the nonlinearity compensation for DCM, the circuit model in DCM is required. First, let D_1, D_2 and D_3 denote the duty ratios of the first, the second and the zero-current interval. The inductor voltage during a switching period is expressed as [5], [12],

$$L\frac{di_{avg}}{dt} = v_L = V_{dc}\left(2D_1 - 1\right) - v_g + \left(V_{dc} + v_g\right)\left[1 - \frac{2Li_{avg}}{\left(V_{dc} - v_g\right)D_1T_{sw}}\right] \quad \text{.....(1)}$$

where V_{dc} is the dc-link voltage and v_g is the grid voltage, T_{sw} is the switching period, i_{avg} is the average current. Then, the circuit model in DCM is established based on (1).

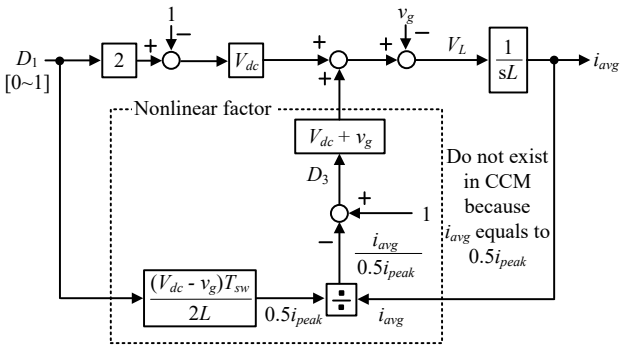


Fig. 4. Circuit model of inverter operating in DCM. The current control loop gain in DCM depends on the average current, i.e. the nonlinearities occurring in the duty-ratio-to-current transfer function and the grid-voltage-to-current transfer function.

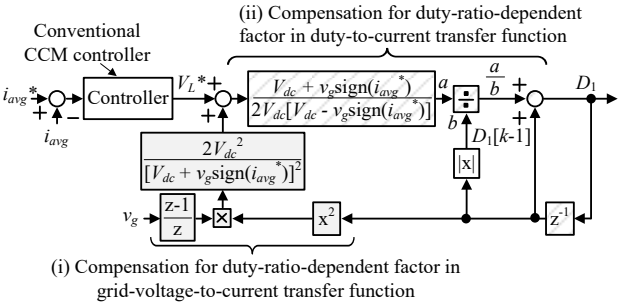


Fig. 5. DCM current control system for single-phase grid-tied inverter. The principle of the DCM nonlinearity compensation is to estimate the duty ratio at the steady-state points by the duty ratio at the previous calculation. Consequently, the circuit parameter such as, e.g. inductance, is not required in the DCM nonlinearity compensation.

Fig. 4 illustrates the circuit model of the inverter operating in DCM. The dash line part does not exist when the inverter operates in CCM because the average current i_{avg} equals to the half current peak $i_{peak}/2$; in other words, the CCM operation makes the zero-current interval D_3T_{sw} shown in Fig. 3 disappear. However, the zero-current interval D_3T_{sw} induces the nonlinearity into the transfer functions when the inverter operates in DCM, which worsens the current response in DCM when the same controller is applied for both CCM and DCM. Therefore, the output of the controller is necessary to be compensated when the inverter operates in DCM.

Fig. 5 illustrates the proposed DCM nonlinearity compensation [12]. As shown in Fig. 4, the value of the duty ratio D_3 is necessary to compensate for the DCM nonlinearity, and D_3 can be estimated from D_1. Therefore, the principle of the DCM nonlinearity compensation in this paper is to use the duty ratio at the previous calculation period $D_1[k\text{-}1]$ in order to estimate the nonlinearity factor. As shown in Fig. 5, the nonlinearity factors in the duty-to-current transfer function and the grid-voltage-to-current transfer function is compensated in the control system. Consequently, the conventional PI controller for CCM can be applied for the DCM operation to achieve the same control performance as in CCM.

B. *Control system of inverter operating in both continuous and discontinuous current*

Fig. 6 indicates the relationship among the CCM duty, the DCM duty and the current mode. The current mode detection between CCM and DCM is necessary when the inverter is designed to operate in both CCM and DCM. One of the conventional current mode detection method is to compare the detection value of the average current i_{avg} (or the average current command i_{avg}^*) with the current value i_{BCM} at the boundary between CCM and DCM; if i_{avg} is larger than i_{BCM}, CCM is determined as the operation mode and vice versa [8]. However, the inductance is used in the calculation of i_{BCM} which implies the current mode determination is inductance-dependent. On the other hand, the current mode determination in this paper focuses on the relationship among the CCM duty $Duty_{CCM}$, the DCM duty $Duty_{DCM}$ and the current mode. In particular, if $Duty_{CCM}$ is larger than $Duty_{DCM}$, DCM becomes the operation mode and vice versa [6], [11]-[12]. Note that $Duty_{CCM}$ is independent from the average current, whereas $Duty_{DCM}$ changes with the variation of the average current. In general, $Duty_{CCM}$ is the output value of the controller, which implies the calculation for $Duty_{CCM}$ is independent from the inductance. If the proposed DCM nonlinearity compensation is employed, the calculation for $Duty_{DCM}$ also becomes inductance-independent. Consequently, if the relationship between $Duty_{CCM}$ and $Duty_{DCM}$ is used to determine the current mode, the inductance-independent current mode determination is achieved.

Fig. 7 describes the CCM/DCM current control system with the waveform of the current mode alternation [12]. In the CCM/DCM current control system, first, both the DCM duty $Duty_{DCM}$ and the CCM duty $Duty_{CCM}$ are generated. Then, the absolute values of these two duty ratios are compared to each other; the smaller duty ratio is used to generate the switching signal for the switches. Note that the absolute operators are used with the consideration of the negative grid voltage. The original idea of the inverter control for the operation in both DCM and CCM is that as first step, the duty ratio at the previous calculation period is used to compensate the DCM nonlinearity regardless of L;

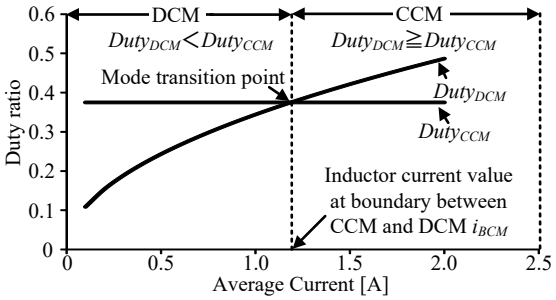


Fig. 6. Relationship among CCM duty, DCM duty and current mode. When the circuit operates in DCM, the DCM duty becomes smaller than the CCM duty and vice versa. The current mode determination is realized independently from the inductor value by using this relationship of the duty ratios.

then, two outputs of the inductance-independently generated duty ratios are compared to each other in order to determine the current mode. Consequently, the CCM/DCM current control system can perform the current control independently from the inductance, which increases the reliability of the inverter control.

C. *Controller parameter design*

In this paper, the PR controller employed with the only-CCM operation, and the PI controller with the proposed DCM nonlinearity is compared. The transfer functions of the PI controller and the PR controller are expressed in (2)-(3), respectively [17]-[19],

$$G_{co\_pi}(s) = K_p + K_i \frac{1}{s} \quad \text{.....(2)}$$

$$G_{co\_pr}(s) = K_p + K_i \frac{s}{s^2 + s + \omega_o^2} \quad \text{.....(3)}$$

where K_p, K_i are gain coefficients, and ω_o ($=2\pi f_g$) is the grid frequency. The current controller design is applied by assuming L_g=0. Note that both PI controller and PR controller are designed with the same crossover frequency ω_c and the same phase margin PM. The gain coefficients of the PI controller and the PR controller are expressed in (4)-(6),

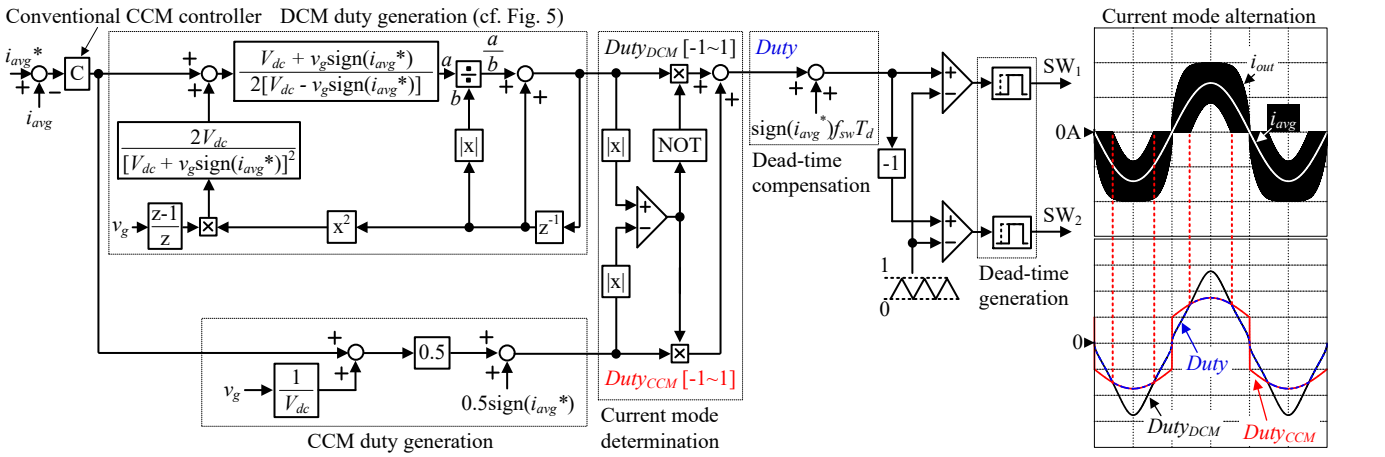


Fig. 7. CCM/DCM current control system with waveform of current mode alternation. The proposed CCM/DCM current control system compensates for the DCM nonlinearity and determines the current mode independently from the circuit parameters such as, e.g. the inductance.

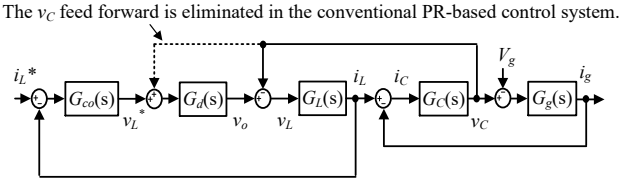


Fig. 8. Block diagram of inverter-current feedback control. The low-inductance filter design increases the disturbance gain of v_c; hence, the inverter becomes more unstable at weak power grid.

respectively,

$$K_{p-pi} = K_{p-pr} = \omega_c (L + L_f) \quad \text{.....(4)}$$

$$K_{i-pi} = \omega_c K_p \tan\left(\frac{\pi}{2} - \frac{\omega_c T_{sw}}{2} - PM\right) \quad \text{.....(5)}$$

$$K_{i-pr} = \left(\omega_c^2 - \omega_o^2\right) K_p \tan\left(\frac{\pi}{2} + \frac{\omega_c T_{sw}}{2} - PM\right) \Big/ 2\omega_c \quad (6)$$

IV. Filter Design

Fig. 8 depicts the block diagram of inverter-current feedback control. Note that the feed forward of v_C is required to make the output of the controller in Fig. 3 become v_L^* in the proposed PI-based control system, whereas this feed forward of v_C is not required in the conventional PR-based control system. The transfer functions in Fig. 8 are expressed in (2)-(3), and (7)-(10),

$$G_d(s) = e^{-1.5T_{sw}s} \quad \text{.....(7)}$$

$$G_L(s) = \frac{1}{Ls} \quad \text{.....(8)}$$

$$G_C(s) = \frac{C_d R_d s + 1}{C_f C_d R_d s^2 + \left(C_f + C_d\right)s} \quad \text{.....(9)}$$

$$G_g(s) = \frac{1}{(L_f + L_g)s} \quad \text{.....(10)}$$

The closed-loop current control transfer function of the proposed control system is derived as follow,

$$G_{cl\_prop}(s) = \frac{G_{co\_pi} G_d G_L G_C G_g}{1 + G_C\left[G_L\left(1 - G_d\right) + G_g\right] + G_{co\_pi} G_d G_L\left(1 + G_C G_g\right)} \quad \text{.....(11)}$$

Fig. 9 describes the filter design algorithm base on the root loci. The filter design starts with the initialization of the following parameters: the rated active power P_n, the dc-link voltage V_{dc}, the single-phase grid voltage v_g, the grid frequency f_g, the switching frequency f_{sw}, and the grid inductance variation L_g. First, L is selected based on the base impedance of the inverter Z_b defined by,

$$Z_b = \frac{v_g^2}{P_n} \quad \text{.....(12)}$$

In general, L is designed such that the impedance of the inverter-side inductor Z_L is several percentages of Z_b in order to avoid the zero-crossing current distortion and the

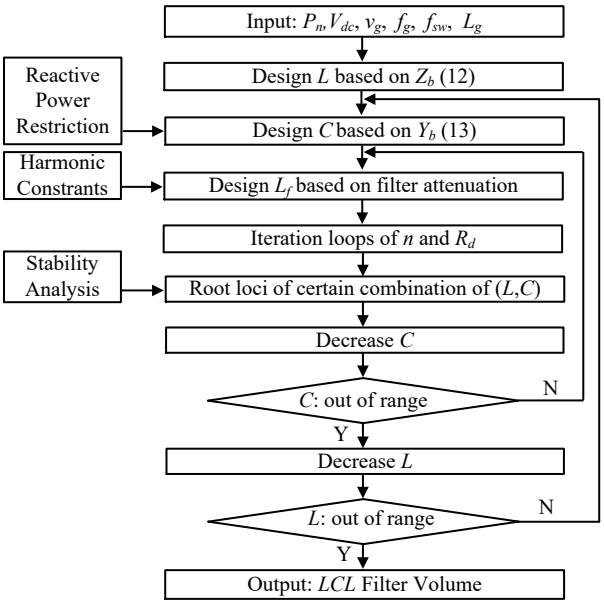


Fig. 9. Passive-damped LCL filter design algorithm. The LCL filter parameters are put in iteration loops in order to achieve the minimum filter volume which is stable even under weak power grid condition.

filter resonance issue. However, this design restricts the minimization of the filter. Therefore, in this paper, the proposed control system with the proposed filter design enables the reduction of the inverter-side inductance.

Next, the capacitor is selected based on the base admittance of the inverter Y_b, which is defined by,

$$Y_b = \frac{1}{2\pi f_g Z_b} = \frac{1}{2\pi f_g} \frac{P_n}{v_g^2} \quad \text{.....(13)}$$

The filter capacitance is limited by the decrease of the power factor at rated power (generally less than 5%), i.e. the reactive power restriction. Then, the grid-side inductance L_f is designed such that the harmonic attenuation of the filter at the switching frequency is high enough to suppress the switching frequency harmonic component of i_g, satisfying the grid standards.

Finally, the capacitor ratio n (i.e. the ratio between C_f and C_d as shown in Fig. 1), and the damping resistor R_d are put in iteration loops in order to analysis the stability considering the grid inductance variation. Each combination of n and R_d is substituting into (11) to obtain the root loci of the closed-loop current control. Consequently, the stability at a certain combination of L and C can be analyzed by the root loci. In order to obtain the minimum filter, L and C can be also put in iteration loops; however, for the sake of simplicity, in this paper, only the stability analysis of one point of (L, C) is demonstrated [20].

V. Laboratory Setup

Table I depicts the system parameters for analysis, simulations and experiment, whereas Fig. 10 shows the prototypes of the inverter and the inverter-side inductor. As shown in Fig. 10(a), the inverter is designed to operate at the high switching frequency of 100 kHz; consequently, the LCL

TABLE I
SYSTEM PARAMETERS FOR ANALYSIS, SIMULATION AND EXPERIMENT

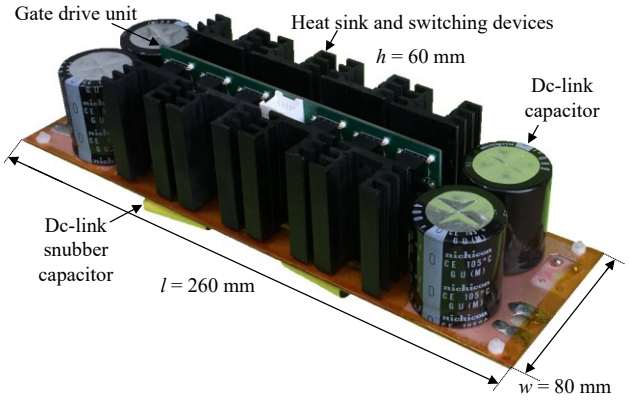
Description	Symbol	Value		
DC link Voltage	v_{DC}	350 V		
Grid Voltage	v_g	200 Vrms		
Nominal Power	P_n	4 kW		
Grid Frequency	f_g	50 Hz		
Switching Frequency	f_{sw}	100 kHz		
Dead Time	$T_{deadtime}$	500 ns		
Sampling Frequency	f_{samp}	25 kHz		
Crossover Frequency	f_c	1 kHz		
Phase Margin	PM	60°		
LCL Filter Design		Case I	Case II	Case III
Grid Inductance	L_g	0	0	2000 μH	2000 μH
Inverter-side Inductance	L	580 μH	160 μH	160 μH	160 μH
Grid-side Inductance	L_f	10 μH	10 μH	10 μH	10 μH
Filter Capacitance	C	4 μF	16 μF	16 μF	16 μF
Capacitance Ratio	n	0.5	1.5	1.5	1.5
Damping Resistance	R_d	16 Ω	16 Ω	16 Ω	8 Ω

filter can be minimized due to a design of a high cutoff frequency. In order to avoid a periodic maintenance of cooling fans, natural cooling method is applied for this prototype. Electrolytic capacitors are used to absorb the single-phase power fluctuation due to their superior ratio between the capacitance and volume compared to film capacitors and ceramic capacitors. As shown in Fig. 10(b), in order to minimize the core loss, and the winding loss at the switching frequency of 100 kHz, ferrite and Litz wire are chosen. It can be observed that the inductor volume (including bobbins) is reduced by 51% when the inverter-side inductor impedance $\%Z_L$ is reduced from 1.8% to 0.5%.

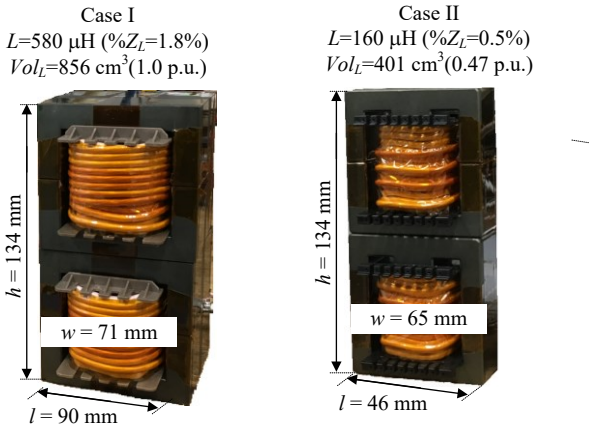
A. Operation verification at normal grid

Fig. 11 depicts the waveforms of grid voltage, grid-side current and inverter-side current under case I and case II, with the PR-based only-CCM control and the proposed PI-based CCM/DCM control. The grid current THD (up to 40th order of the harmonic component) is measured by a YOKOGAWA WT1800 power meter. As shown in Fig. 11(a)-(b), the low-inductance filter design leads to the high switching current ripple. Therefore, when $\%Z_L$, which is the inverter-side inductor impedance normalized by the total inverter impedance Z_b, is reduced from 1.8% to 0.5%, the grid current THD at the rated load of 4 kW with the PR-based only-CCM control increases from 3.7% to 8.7%. According to standards such as IEEE-1547, the grid current THD at the rated load must be lower than 5%; hence, the inductor impedance design of 0.5% with the PR-based only-CCM control, of which the grid current THD at the rated load is 8.7%, does not satisfy the harmonic constraint.

On the other hand, it can be observed clearly from Fig. 11(d) that the inverter is intentionally operated under DCM in the vicinities of the zero-current crossing. Due to the DCM nonlinearity compensation, the same current dynamic as CCM is achieved during the DCM interval; consequently, the zero-current distortion is eliminated. In particular, the proposed PI-based CCM/DCM control reduces the grid current THD at the rated load from 8.7% to 2.1% compared to that of the PR-based only-CCM control with $\%Z_L$ of 0.5%.



(a) 4-kW prototype of single-phase grid-tied inverter



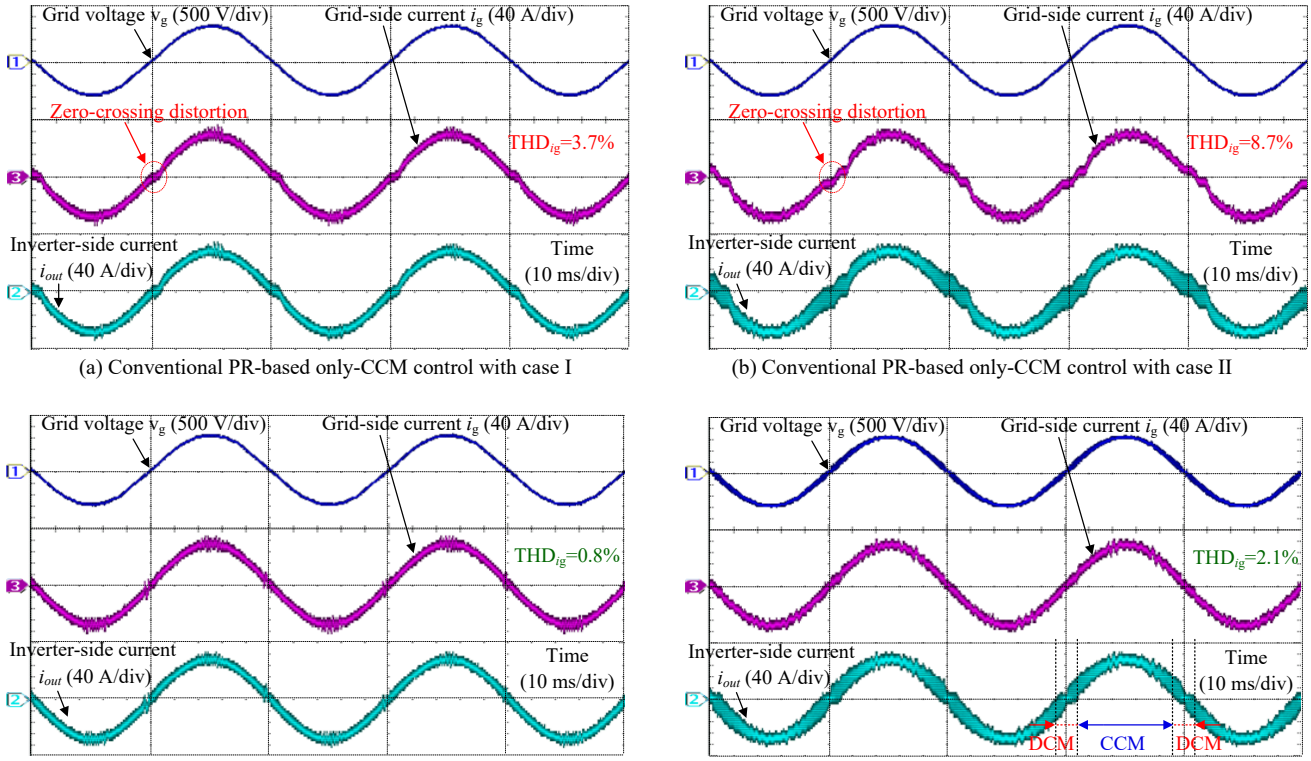
(b) Prototypes of inverter-side inductor

Fig. 10. Prototypes of inverter and inverter-side inductor. SiC switching devices from ROHM semiconductor are chosen to operate the inverter at high switching frequency of 100 kHz. It is clearly observed that the inductor volume is reduced by 51% due to the reduction of the inverter-side inductor impedance $\%Z_L$ from 1.8% to 0.5%.

Therefore, the proposed PI-based CCM/DCM control enables the minimization of the inverter-side inductor impedance without violating the harmonic constraint regulated by standards such as IEEE-1547.

B. Operation verification at weak power grid

Fig. 12 depicts the pole trajectory of the proposed closed-loop control system at weak power grid, i.e. the high grid inductance of 2000 μH. Note that only the poles at low frequencies and the half upper plane is shown. As the damping capacitance C_d increases (or the capacitance ratio increases), the pole moves toward the left plane, i.e. the system becomes more stable. On the other hand, the damping effectiveness does not simply increase with the increase of the damping resistance, because a high damping resistance restricts the current flowing into the damping capacitor, i.e. the reduction of the damping effectiveness. The weak power grid is analyzed under two design cases (case II and case III) as shown in Table I and Fig. 12. In particular, the pole in case II is designed to be at the left plane in respect to the y-axis, whereas the pole in case III is located on the y-axis, i.e. the boundary of stability.



(a) Conventional PR-based only-CCM control with case I

(b) Conventional PR-based only-CCM control with case II

(c) Proposed PI-based CCM/DCM control with case I

(d) Proposed PI-based CCM/DCM control with case II

Fig. 11. Waveforms of grid voltage, grid-side current and inverter-side current under case I and case II, with the PR-based only-CCM control system and the proposed PI-based CCM/DCM control system. The conventional PR-based only-CCM control results in a high current THD of 8.7% when the inverter-side inductance is reduced to 160 μH, which is 0.5% of the total inverter impedance. On the other hand, the proposed PI-based CCM/DCM control enables the design of the low-inductance filter by maintaining the low current THD of 2.1%.

Fig. 13 depicts the simulation waveforms of grid voltage, grid-side current and converter-side current under case II (L_g=2000 μH) and case III with the proposed PI-based CCM/DCM control system. As shown in Fig. 13(a), the filter resonance is effectively damped even with small Z_L and Z_{Lf} of only 0.5% and 0.06% of Z_b, respectively. The low current THD is still achievable even under the weak power grid condition. On the other hand, the filter resonance still occurs in Fig. 13(b) as expected from Fig. 12. Furthermore, the filter resonance also increases the current THD to 6.3%. These results confirm the effectiveness of the proposed control and the validation of the filter design method.

VI. Conclusion

This paper proposed the filter design method for a passive-damped *LCL* filter in single-phase grid-tied inverters operating in both CCM and DCM. The low-inductance filter design can minimize the filter volume. However, this design has to solve two challenges: zero-crossing distortion and the filter resonance. The zero-crossing distortion increases with the decrease in the inductance because the DCM intervals occurring in the in the vicinities of the zero-current crossing becomes longer. Therefore, in order to reduce the current distortion, the inverter operation in both CCM and DCM is used. In particular, the DCM nonlinearity compensation is introduced into the control system in order to obtain the same current control performance as in CCM. The main feature of the CCM/DCM control system is that the DCM nonlinearity compensation is constructed by the duty ratio at the previous calculation period. Compared to the conventional DCM nonlinearity compensation method, the inductance is not required in the proposed DCM nonlinearity compensation method. On the other hand, the filter resonance is damped by inserting a RC leg in parallel to the filter capacitor. The design method for this passive-damped *LCL* filter is accomplished by the filer design flow chart based on the root locus. Current control performances are compared between a well-known proportional-resonant (PR) controller employed with the only-CCM operation, and the PI controller with the proposed CCM/DCM operation. Compared to the conventional CCM control, the proposed CCM/DCM control reduces the current total harmonic distortion (THD) by 75.9%. Even at weak power grid (i.e. a high grid inductance of 2000 mH), the proposed control can obtain a low current THD of 0.8% with the filter inductance reduced to only 160 mH, which is 0.5% of the total inverter impedance.

In the future, the application of the CCM/DCM control method to other topologies such as, e.g. three-phase inverters, or flying-capacitor converters, will be analyzed.

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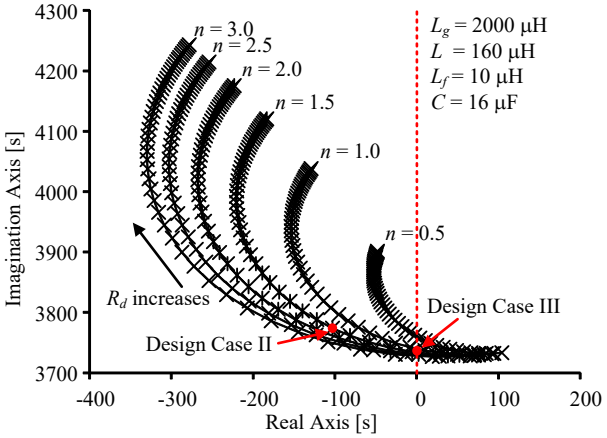
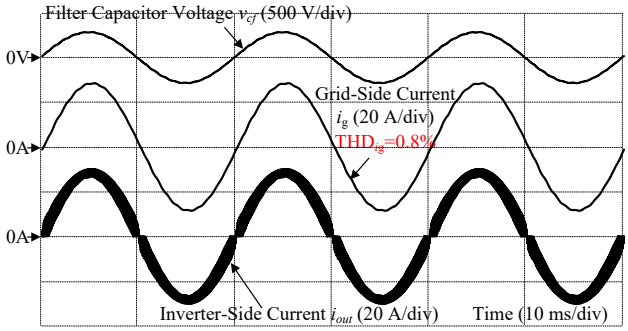
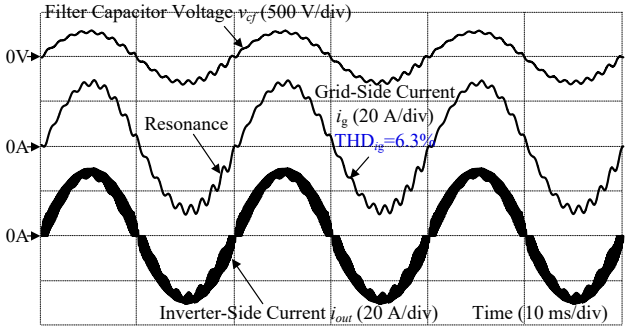


Fig. 12. Pole trajectory of proposed closed-loop control system at weak power grid, i.e. high grid inductance of 2000 μH. The design in case II is selected based on the stability and the damping loss, whereas the design in case III is to confirm the validation of the proposed DCM nonlinearity compensation and the design flowchart.



(a) Proposed control system under case II (L_g=2000 μH)



(b) Proposed control system under case III (L_g=2000 μH)

Fig. 13. Simulation waveforms of grid voltage, grid-side current and converter-side current under case II (L_g=2000 μH) and case III with the proposed PI-based CCM/DCM control system. As expected from Fig. 12, the inverter operates stably in case II (cf. Fig. 13(a)), whereas the filter resonance still remains in case III (cf. Fig. 13(b)).

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