

# Single-phase power decoupling technique utilizing Hybrid method with passive and active power decoupling

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**Abstract**— This paper proposes a power decoupling method utilizing active and passive method to improve the power density. The active power decoupling techniques compensate the double-line frequency power ripple with a small capacitor. However, when whole power ripple is compensated by the active power decoupling circuit, the total volume becomes large due to the additional component in comparison with the passive method with large electrolytic capacitor. The proposed method limits the power ripple compensation value of the power decoupling circuit in order to reduce the buffer capacitance or peak capacitor voltage. Instead, the small electrolytic capacitor is installed on DC-link for the power decoupling capability. In this method, the DC-link capacitor is smaller than that in the passive power decoupling circuit owing to the small buffer power and the low ripple current. From the experimental result, the second order harmonics is reduced by 76.8% by the DC active filter with the small capacitor of 60  $\mu\text{F}$ . Finally, the power density of the DC active filter with the hybrid method is improved by 38% in comparison with the whole active power decoupling operation.

**Keywords**— Grid connected inverter, double-line frequency power ripple, power decoupling

## I. INTRODUCTION

The single phase grid connected inverters are utilizing for DC to single-phase AC power conversion system such as photovoltaic (PV) systems or battery energy storage systems and so on [1]. These converter needs the high efficiency conversion, high reliability, and miniaturization in order to enhance the convenience. Recently, the conversion efficiency has been drastically improved by the wide-band gap devices as SiC-MOSFET [2]. In the DC to single-phase AC system, the double-line frequency power ripple is issue for MPPT performance or battery life-time enhancement. Therefore, the passive power decoupling which use a bulky electrolytic capacitor is necessary. On the other hand, PV system reliability evaluation have been reported by researchers, and it is presented that an electrolytic capacitor limits the life-time of the converter [3].

According to this problem, the active power decoupling techniques which have a film or ceramic capacitor are attracted as the one of this solutions [4]-[6]. The active power decoupling circuit charges and discharges the decoupling capacitor in order to absorb the double-line frequency power ripple, which enables to small capacitor. As a result, large electrolytic capacitor does not necessary. The typical active power decoupling topology is the DC active filter (DCA) which is composed to of the boost converter or buck converter.

The DC active filter is connected in parallel with the main circuit, and it compensates the power ripple by the small capacitor.

The authors have reported the power density evaluation of the passive power decoupling circuit and the active power decoupling circuit with DC active filter [7]. In this report, the component volume miniaturization for active method is required to reach the power density of the passive method. In particular, if the whole power ripple is compensated by the power decoupling circuit, then the ripple voltage of the buffer capacitor becomes large. On the other hand, the buffer capacitor voltage has to keep more than the DC-link voltage for the DC active filter control. As the result, minimum capacitance value is increased.

This paper presents a hybrid power decoupling technique using the active power decoupling capability and the passive power decoupling capability. In this method, the active power decoupling circuit limits the compensation value of the power ripple in order to reduce the buffer capacitance or buffer capacitor peak voltage. In this case, the power ripple still occurs on DC-link. Therefore, the remaining double-line frequency component is compensated by the DC-link capacitor like a passive active power decoupling. Note that the DC link capacitance is reduced in comparison with that of the typical passive power decoupling circuit because the buffer power on DC link capacitor becomes small by the active method. Besides, the low-order ripple current can suppress owing to the active power decoupling circuit.

The remainder of this paper is organized as follows. In section II, the configuration of the proposed converter and fundamental principle of the power decoupling are explained. In section III, the detail of the power decoupling control is explained. In section IV, the circuit design principle of the passive method and the power decoupling circuit is introduced. Finally, the experimental result and the power density comparison among the passive power decoupling, active power decoupling circuit, and the proposed method are demonstrated.

## II. CIRCUIT CONFIGURATION

Fig. 1 shows the single-phase grid-connected inverter with a boost converter. In this converter topology, a bulky electrolytic capacitor  $C_{dc}$  is necessary on the DC-link to absorb the double-line frequency power ripple by the single-phase grid.

Fig. 2 shows a boost type DCA circuit which consists of boost converter and a small buffer capacitor  $C_{buf}$  to absorb the double-line frequency power ripple on DC-link. The capacitor  $C_{buf}$  has the small capacitance, thus the long life-time capacitor such as a film or a ceramic capacitor is usually used instead of electrolytic capacitor.

Fig. 3 shows the principle of the power decoupling compensation. When both the output voltage and current waveforms are sinusoidal, the instantaneous output power  $p_{out}$  is given by

$$p_{out} = \frac{V_{acp} I_{acp}}{2} (1 - \cos 2\omega t) \quad (1)$$

where  $V_{acp}$  is the peak grid voltage,  $I_{acp}$  is the peak inverter output current, and  $\omega$  is the angular frequency of the grid voltage [8]. As shown in (1),  $p_{out}$  includes the frequency component of the double line frequency. This frequency component should be compensated by the energy buffer in order to obtain the constant DC input power.

In order to absorb this power fluctuation, the instantaneous buffer power  $p_{buf}$  should be controlled by

$$p_{buf} = \frac{1}{2} V_{acp} I_{acp} \cos 2\omega t \quad (2)$$

When the  $p_{buf}$  is obtained as (2), the PV input power  $P_{in}$  becomes constant, and it is expressed as

$$p_{in} = \frac{1}{2} V_{acp} I_{acp} = V_{in} I_{in} \quad (3)$$

### III. CONTROL BLOCK DIAGRAM

Fig.4 shows the control block diagram for each converter. In the boost converter control, an input current control with PI control is applied to regulate the PV input current. On the other hand, the DC-link voltage and the inverter output current control are implemented on the Voltage Source Inverter (VSI). The DC link voltage is regulated to be higher than the peak grid voltage  $V_{acp}$ , and the inverter output current is controlled to sinusoidal waveforms.

The DCA control consists of the buffer capacitor average voltage control and the current control. In order to implement the active power decoupling capability, the feed forward control is applied to current control. The feed forward current is expressed as

$$i_{amp} = \frac{P_{comp}^*}{V_{dc}} \cos 2\omega t \quad (4)$$

where  $P_{comp}^*$  is the compensation value of the power ripple.  $V_{dc}$  is the DC-link voltage. In order to reduce the capacitance of the buffer capacitor  $C_{buf}$ , the capacitor voltage is actively fluctuated at double-line frequency of the single-phase grid.

However, the response speed of the voltage control is limited to slow in comparison with the response speed of the

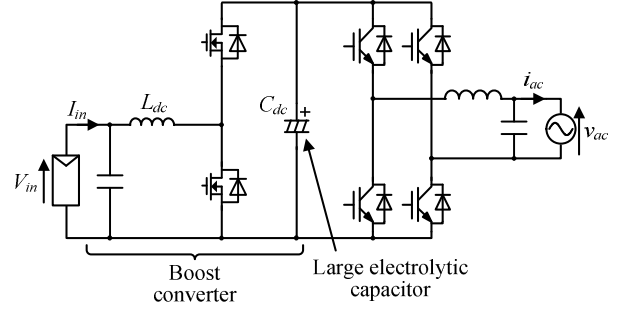


Fig. 1. Typical configuration of DC to single-phase AC grid connected inverter. Large electrolytic capacitor is installed on DC link in order to achieve power decoupling.

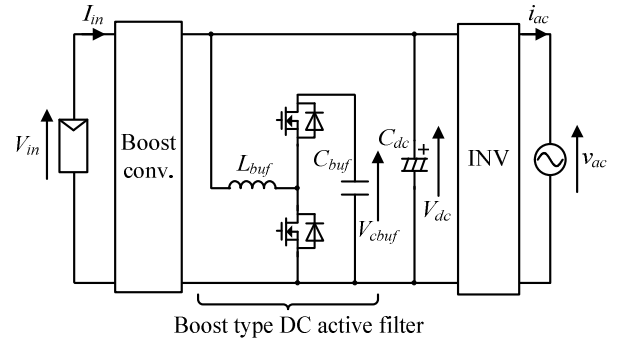


Fig. 2. Circuit configuration of boost type DC active filter. Buffer capacitor voltage  $V_{cbuf}$  is regulated more than the DC link voltage  $V_{dc}$ . proposed hybrid power decoupling is achieved by small buffer capacitor  $C_{buf}$  and DC link capacitor  $C_{dc}$ .

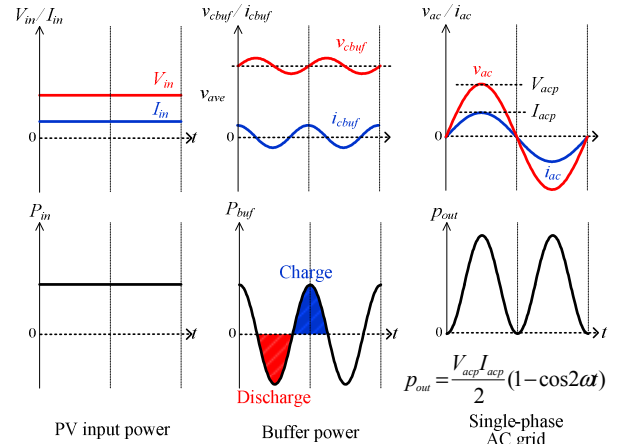


Fig. 3. Principle of the power ripple compensation. Buffer power  $P_{buf}$  is charge and discharge by the buffer capacitor  $C_{buf}$ . The  $P_{buf}$  is given by the mismatch between input power  $P_{in}$  and output power  $P_{out}$ .

current control for control stabilization. Thus, the active power decoupling control is applied to the current control directly. On the other hand, the voltage control regulates only average voltage of  $C_{buf}$ . In addition, the band eliminate filter which has double-line frequency elimination is installed to the detection part of  $V_{cbuf}$ .

Owing to the active power decoupling control, the power ripple is compensated by the small capacitor  $C_{buf}$ . Note that, the capacitance of  $C_{buf}$  is expressed as

$$C_{buf} = \frac{P_{comp}^*}{\omega V_{ave\_cbuf} \Delta V_{cbuf}} \quad (5)$$

where  $V_{ave}$  is the average voltage.  $\Delta V_{cbuf}$  is the ripple voltage. As shown in (5), the buffer power becomes maximum when the  $P_{comp}^*$  is set to 1 p.u. In addition, the  $\Delta V_{cbuf}$  becomes large for reduction of  $C_{buf}$ . However, it means that the high voltage rating is necessary for each components. Focusing on the capacitor volume, it depends on the capacitance and the voltage rating.

In order to solve this problem, the hybrid power decoupling with  $C_{buf}$  and  $C_{dc}$  is proposed. In this method, the  $P_{comp}^*$  is limited to reduce the  $\Delta V_{cbuf}$  or  $C_{buf}$ . The differential value between the buffer power and the actual ripple power is compensated by the DC-link capacitor  $C_{dc}$ . In this case, the capacitance of  $C_{dc}$  is expressed as

$$C_{dc} = \frac{P_{diff}}{\omega V_{ave\_cdc} \Delta V_{dc}} \quad (6)$$

$$P_{diff} = P_{buf\_1p.u.} - P_{comp}^* \quad (7)$$

where  $P_{diff}$  is the differential power between actual ripple power and compensation power of the DCA.  $\Delta V_{dc}$  is the ripple voltage of  $V_{dc}$ . The case of passive power decoupling, the  $\Delta V_{dc}$  is designed to small in order to obtain the constant value. As a result, the  $C_{dc}$  is drastically increase. The proposed power decoupling method obtains the buffer energy from both the  $C_{buf}$  and  $C_{dc}$ . Therefore, the  $P_{diff}$  can be reduced in comparison with the passive power decoupling. Finally, the ripple current of the double-line frequency can be suppressed by the DCA. Thus, the  $C_{dc}$  can choose the small electrolytic capacitor with low capacitance. Besides, the life-time of  $C_{dc}$  can be improved by the small ripple current.

#### IV. CIRCUIT DESIGN

This section introduce the circuit design of the boost converter and the DCA in order to discuss the power density of the power converter. In this paper, the design method of the VSI does not include because it is the same in the active/passive power decoupling capability.

##### A. Boost converter design

The boost inductor  $L_{dc}$  is designed by the ripple current condition. The inductance of  $L_{dc}$  is expresses as

$$L_{dc} = \frac{V_{in} - V_{dc} - V_{in}}{\Delta I_{Ldc} f_{sw} V_{dc}} \quad (8)$$

where  $V_{in}$  is the PV input voltage,  $V_{dc}$  is the DC-link voltage,  $\Delta I_{Ldc}$  is the ripple current,  $f_{sw}$  is the switching frequency.

The inductor volume is decided from many parameters of the components, and there are a lot of ways to choose the core for the inductor. In this paper, the inductor volume is decided from an area product concept using the window area and the cross-sectional area.

The volume of the  $L_{dc}$  is calculated by

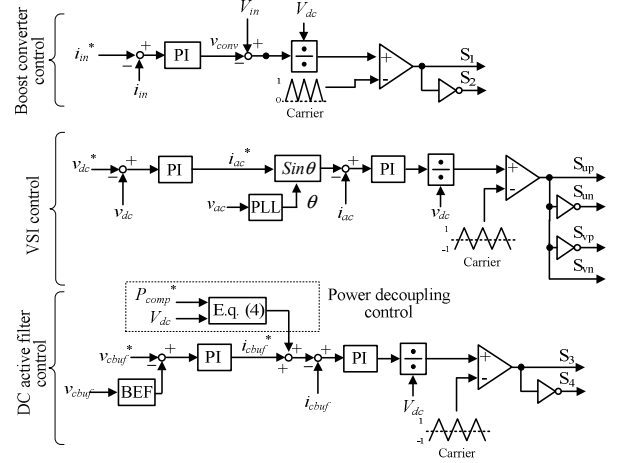


Fig. 4. Control method of the DC active filter. Feed forward control is applied to current control for active power decoupling.

$$Vol_{Ldc} = K_v \left( \frac{L_{dc} I_{max}^2}{K_u B_{max} J} \right)^{\frac{3}{4}} \quad (9)$$

where  $K_v$  is the volume coefficient,  $I_{max}$  is the maximum current of the inductor,  $K_u$  is the fill factor of the window,  $B_{max}$  is the maximum flux density, and  $J$  is the current density of the wire.

Fig. 5 shows the relationship between the compensation value  $P_{comp}^*$  and the capacitance of  $C_{dc}$ . Note that the DC-link capacitance is designed from (6). According to Fig.5, the capacitance is reduced when the  $P_{comp}^*$  is increased. In particular, the capacitance for the power decoupling becomes zero when the  $p_{comp}^*$  is set to 1 p.u.. Actually, the small capacitor is necessary for the VSI control and the switching filter. Therefore, the small ceramic capacitor should be installed on DC-link because the capacity requirement of  $C_{dc}$  is very small.

On the other hand, the electrolytic capacitor should be selected when the  $P_{comp}^*$  is small because the large capacitance is required for the power decoupling capability.

The electrolytic capacitor is selected based on the capacitance from Fig. 5, and the allowable ripple current. With the frequency multipliers, the allowable ripple current is calculated by

$$I_{rms\_cap} = \sqrt{\frac{I_{100Hz\_rms}^2}{K_{100Hz}} + \left( \frac{1}{K_{sw}} \right)^2 \sum_{n=1}^{\infty} I_{nsw}^2} \quad (10)$$

where  $I_{100Hz\_rms}$  is the effective current whose frequencies are double line frequency of the single-phase grid,  $I_{nsw}$  is the effective current at the switching frequency,  $K_{100Hz}$  and  $K_{sw}$  are the frequency multipliers at 100 Hz and the switching frequency, respectively. An electrolytic capacitor, which has the allowable ripple current higher than the result of (10), should be required. In the passive method, the large ripple current rating is necessary because the  $I_{100Hz\_rms}$  is becomes large. However, the hybrid method can reduce the ripple current with low-order harmonics by the DC active filter. Therefore, an electrolytic capacitor with low current rating can select in the proposed method.

Fig. 6 shows the relationship between the low-order harmonics ripple current through the DC-link capacitor with 100 Hz and the compensation value of  $P_{comp}^*$ . The low-order ripple current is suppressed by the active power decoupling circuit. Therefore, the small electrolytic capacitor with low ripple current rating is applied for the hybrid method in order to improve the power density.

### B. DC active filter design

The inductor of DCA  $L_{buf}$  is also designed from the ripple current as the boost converter, and the inductance  $L_{buf}$  is expressed as

$$L_{buf} = \frac{V_{dc}}{\Delta I_{L_{buf}} f_{sw}} \frac{(V_{cbuf\_ave} + \frac{\Delta V_{cbuf}}{2}) - V_{dc}}{(V_{cbuf\_ave} + \frac{\Delta V_{cbuf}}{2})} \quad (11)$$

the ripple current becomes the maximum value when the difference between the dc-link voltage and the buffer capacitor voltage reaches the maximum. Therefore, the  $L_{buf}$  is designed at the buffer capacitor peak voltage condition. The buffer capacitor peak voltage is calculated by (5). The inductor volume is also calculated from (9). Note that the inductor current becomes small in the hybrid method. Therefore, the inductor volume is reduced when the  $P_{comp}^*$  is set to low value.

Fig. 7 shows the relationship between the compensation value  $P_{comp}^*$  and the minimum buffer capacitance for voltage control, and Fig.8 shows the relationship between the buffer capacitor peak voltage and the buffer capacitance condition. The buffer capacitor voltage has to keep more than the DC-link voltage due to the boost-up operation. According to Fig. 7, the minimum value of the  $C_{buf}$  becomes large when the  $P_{comp}^*$  is increased. This is because the ripple voltage  $\Delta V_{buf}$  becomes large. Therefore, the small buffer capacitor is obtained when  $P_{comp}^*$  is set to low value. In addition, the capacitance of  $C_{buf}$  is drastically reduced when the average voltage  $V_{cbuf\_ave}$  is set to high. On the other hand, the buffer capacitor peak voltage becomes large from Fig. 8. As the result, the switching loss of the DCA increases. However, the peak voltage condition is changed due to the buffer capacitance design. For example, the peak voltage is reduced when the  $C_{buf}$  is the same at each compensation value. Therefore, the relationship between the heat sink volume and the buffer capacitor volume has the trade-off because the buffer capacitor is designed to minimum value at each compensation condition, the peak buffer capacitor becomes same.

### C. Heat sink design

Generally, the cooling system volume is decided from the thermal resistance. In this paper, the cooling system volume is designed by the Cooling System Performance Index (CSPI). CSPI means the cooling performance per unit volume of the cooling system. The cooling system is miniaturized when CSPI become higher. The volume of the cooling system  $Vol_{heatsink}$  is given by

$$Vol_{heatsink} = \frac{1}{R_{th(f-a)} CSPI} \quad (12)$$

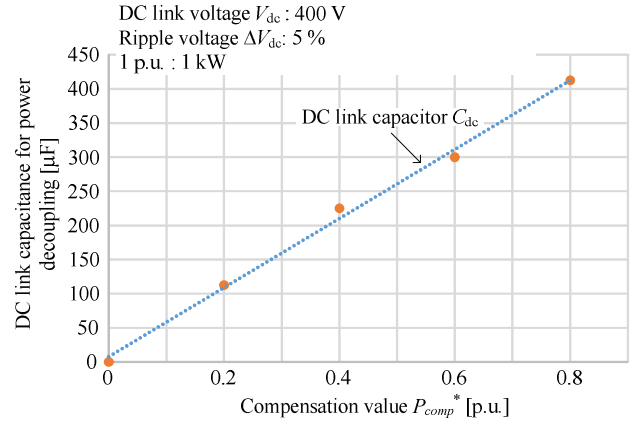


Fig. 5. Relationship between compensation value and capacitance of  $C_{dc}$ . the DC link capacitor volume becomes small when compensation value increases.

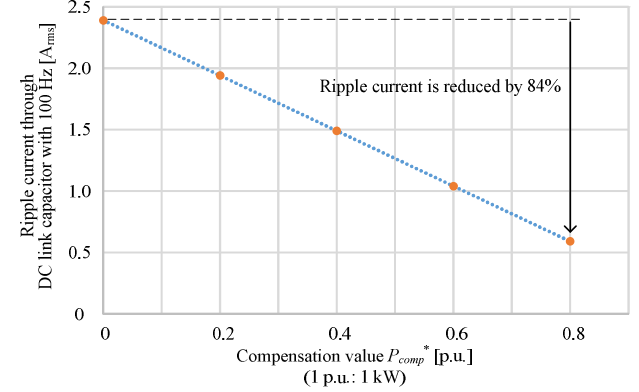


Fig. 6. Relationship between compensation value and capacitance of  $C_{dc}$ . the DC link capacitor volume becomes small when compensation value increases.

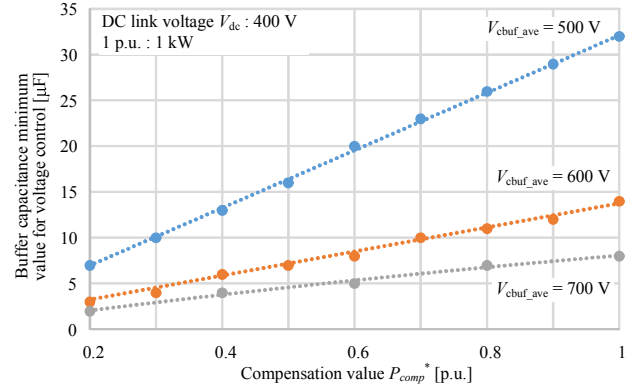


Fig. 7. Buffer capacitor minimum value when average voltage is changed.

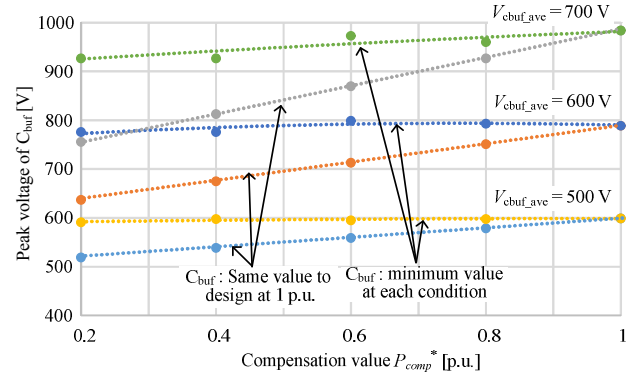


Fig. 8. Peak voltage of buffer capacitor when capacitor condition is changed.

where  $R_{th(f-a)}$  is the thermal resistance of the cooling system which is given by

$$R_{th(f-a)} = \frac{T_j - T_a}{P_{loss}} \quad (13)$$

where  $T_j$  is the junction temperature of the switching device,  $T_a$  is the ambient temperature, and  $P_{loss}$  is the converter losses. The total loss  $P_{loss}$ , which is composed of the conduction loss  $P_{loss\_cond}$  and the switching loss  $P_{loss\_sw}$  from the switching devices, and there are given by following equation.

$$P_{loss\_cond\_buffer} = \frac{1}{T_{out}} \int_0^{T_{out}} i_{Lbuf}^2 r_{on\_buffer} dt \quad (14)$$

$$P_{loss\_sw\_buffer} = \frac{1}{E_{dcd} I_{md}} (e_{on} + e_{off}) f_{sw} \frac{1}{T_{out}} \int_0^{T_{out}} v_{cbuf} i_{Lbuf} dt \quad (15)$$

respectively, where,  $T_{out}$  is the period of the grid,  $r_{on}$  is the on-resistance of the switching devices,  $f_{sw}$  is the switching frequency of the DCA,  $e_{on}$  and  $e_{off}$  are the turn-on and turn-off energy per switching referred from a datasheet, respectively,  $E_{dcd}$  and  $I_{md}$  are the voltage and the current under the measurement condition of the switching loss described in the datasheet.

The boost converter losses are also obtained based on (14) and (15), and it is calculated by

$$P_{loss\_cond\_boost} = \frac{1}{T_{out}} \int_0^{T_{out}} i_{Ldc}^2 r_{on\_buffer} dt \quad (16)$$

$$P_{loss\_sw\_boost} = \frac{1}{E_{dcd} I_{md}} (e_{on} + e_{off}) f_{sw} \frac{1}{T_{out}} \int_0^{T_{out}} v_{dc} i_{Ldc} dt \quad (17)$$

## V. EXPERIMENTAL RESULT AND POWER DENSITY EVALUATION

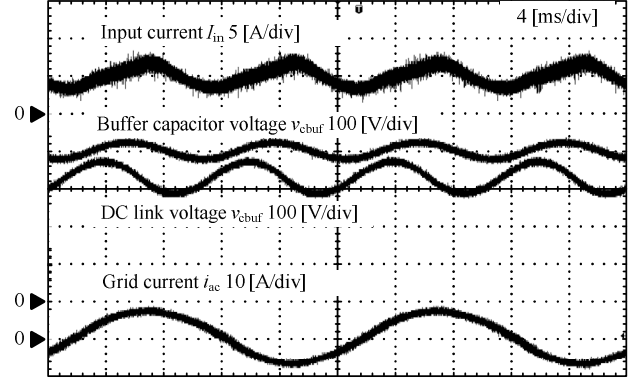
In this section, the fundamental consideration is demonstrated by experiment. Table. I shows the experimental condition.

Fig. 9 shows the experimental result when  $P_{comp}^*$  is set to 1.0 p.u., and Fig. 10 shows the harmonic analysis result of the PV input current. According to Fig. 9 (b), the PV input current becomes constant in comparison with without power decoupling. In addition, it is confirmed that the buffer capacitor voltage is fluctuated at the double-line frequency by the active power decoupling control. Therefore, the active power decoupling operation is achieved. According to Fig. 10, the second order harmonics is reduced by 76.8% in comparison with without active power decoupling control.

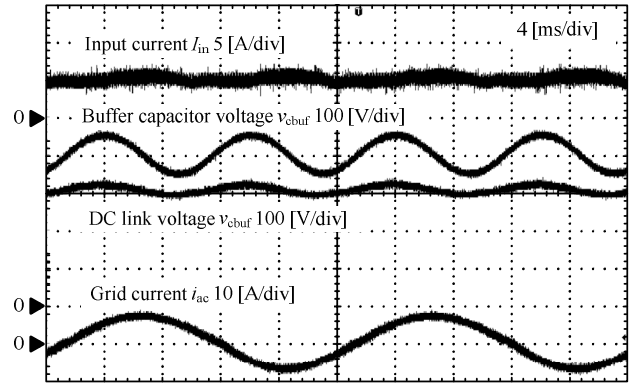
Table II shows the component parameters, and Fig. 11 shows the pareto front between the power density and the conversion efficiency when the buffer capacitance is changed to minimum at each condition. In this figure, the boost converter and the DCA are considered. The conversion losses are calculated from (14) to (17). In addition, the electrolytic capacitor is selected based on the minimum capacitance value for the power decoupling and the low-order harmonics current ripple. Finally, the power density of the active power

Table. I. Experimental condition.

Symbol	Quantity	Value
$V_{in}$	Input voltage	200 V
$P_{rated}$	Rated power	1 kW
$f_{sw}$	Switching frequency	20 kHz
$C_{buf}$	Buffer capacitor	60 $\mu$ F
$C_{dc}$	DC link capacitor	40 $\mu$ F
$f_{ac}$	Grid frequency	50 Hz
$V_{ac}$	Grid voltage	200 V <sub>rms</sub>



(a) Without power decoupling



(b) With power decoupling

Fig. 9. Experimental result with DC active filter. The constant input current is obtained by the power decoupling control.

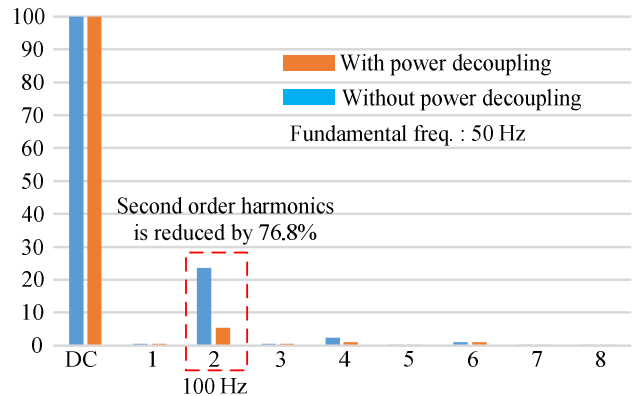


Fig. 10. Harmonic analysis result. The second order harmonics is reduced by 76.8% in comparison with without power decoupling.

decoupling circuit based on the flying capacitor DC/DC converter (FCC) without the additional components is also considered. Note that the detail of the converter operation and the circuit configuration is introduced in [8].

According to Fig. 11, the power density of the DC active filter with whole power decoupling is 4.32 kW/dm<sup>3</sup>. On the other hand, the power density of the DC active filter with hybrid method is improved by 38% when the  $P_{comp}^*$  is set to 0.2 p.u. This is because the buffer inductor volume is drastically reduced. On the other hand, the power density of the FCC becomes high more than the DCA and passive method because this circuit does not need the additional inductor for the power decoupling capability. The power density of the FCC with the hybrid method is also improved by 7%. This is because the flying capacitor volume is reduced.

Fig. 12 shows the pareto front when the buffer capacitance is the same at each condition. In this case, the buffer capacitance is designed by the whole power decoupling condition. According to Fig. 12, the each power density of the DCA with the hybrid method is improved because the buffer inductor and the heat sink volume becomes small. However, the power density of the FCC with the hybrid method is decreased. This is because the boost inductor current is the same at each condition. In other words the power density of the FCC depends on the DC-link capacitor, and the heat sink. In this case, the increasing rate of the DC-link capacitor volume is large in comparison with the reduction of the heat sink volume. As the result, the power density becomes low. According to Fig. 11 and 12, it is confirmed that the buffer capacitor minimization design with the hybrid method achieves the high power density.

## VI. CONCLUSION

This paper proposed the hybrid power decoupling method utilizing the active power decoupling circuit and passive power decoupling to reduce the circuit volume. The proposed method uses the active power decoupling circuit and the small electrolytic capacitor in order to compensate the power ripple. As the experimental result, the second order harmonics of input current is reduced by 76.8%. Finally, the power density of the hybrid method is improved by 38% in comparison with the full power decoupling control. In addition, the FCC with the hybrid method is obtained the high power density in comparison with the passive method and the DCA.

## REFERENCES

- [1] Mitsumasa Ushiroda, Takaaki Wakimoto, Hiroaki Yamada, Toshihiko Tanaka, Masayuki Okamoto, Koji Kawahara "Voltage Rise Suppression and Load Balancing by PV-PCS with Constant DC-Capacitor Voltage-Control-Based Strategy in Single-Phase Three-Wire Distribution Feeders" *IEEJ Journal of Industry Application*, Vol. 6, No. 5, pp. 303-310, (2017)
- [2] Ritwik Chattopadhyay, Subhashish Bhattacharya, Nicole C. Foureux, Igor A. Pires, Helder de Paula, L enin Moraes, Porfirio C. Cortizio, Sidelmo M. Silva, Braz Cardoso Filho, Jos e A. de S. Brito "Low-Voltage PV Power Integration into Medium Voltage Grid Using High-Voltage SiC Devices" *IEEJ Journal of Industry Application*, Vol. 6, No. 6, pp. 767-775, (2015)
- [3] H. Wang; K. Ma; F. blaabjerg; "Design for reliability of power electronics systems" *IECON 2012*, pp. 33-44, (2012)
- [4] Yi Tang; F. Blaabjerg; "A Component-Minimized Single-Phase Active Power Decoupling Circuit With Reduced Current Stress to Semiconductor Switches" *IEEE Trans. Power Electron.* Vol. 30, No. 6, pp. 2905-2910, (2015)
- [5] T. Shimizu, S. Suzuki; "A single-phase grid-connected inverter with power decoupling function" *ECCE Asia*, pp. 2918-2923, (2006)
- [6] S. Yamaguchi, S. Suzuki; "Single-phase Power Conditioner with a Buck-boost-type Power Decoupling Circuit" *IEEJ Journal of Industry Application*, Vol. 5, No. 3, pp. 191-198, (2016)
- [7] J. Itoh, T. Sakuraba, K. Kusaka, H. Watanabe, K. Furukawa; "Comparison of Circuit Topologies for Active Power Decoupling toward High Power Density", the 2016 8th International Power Electronics and Motion Control Conference - ECCE Asia, No. Mb6-30 (2016)
- [8] H. Watanabe, K. Kusaka, K. Furukawa, K. Orikawa, J. Itoh; "DC to Single-phase AC Voltage Source Inverter with Power Decoupling Circuit based on Flying Capacitor Topology for PV System", The Applied Power Electronics Conference and Exposition 2016, pp. 1336-1343 (2016)

Table. II. Device parameters.

Symbol	Quantity	Value
$V_{dc}$	DC link voltage	400 V
$P_{rated}$	Rated power	1 kW
$V_{cbuf,ave}$	Buffer capacitor average vol.	600 V
$C_{buf}$	Ceramic capacitor SP 900 (TDK)	5 $\mu$ F/900 V
$C_{dc}$	Electrolytic capacitor EKHS501VSN820MP30S (United Chemi-Con)	82 $\mu$ F/500 V 0.7A@100 Hz
Switching devices	DCA, Boost conv.	SCT3030KL (ROHM sem.) 1200V/72A 30m $\Omega$
	FCC	SCT3017AL (ROHM sem.) 650V/118A 17m $\Omega$

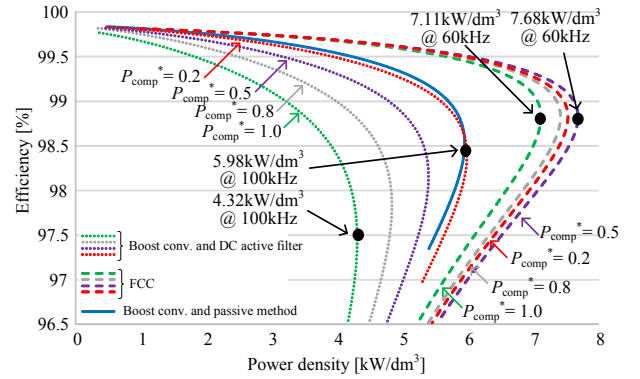


Fig. 11. Pareto front with constant buffer voltage condition.

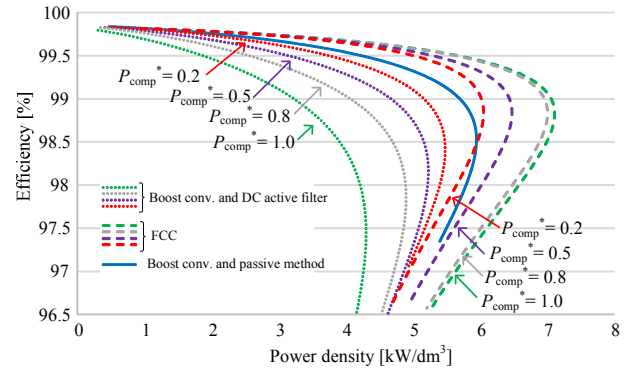


Fig. 12. Pareto front with constant buffer capacitor condition.