

Voltage Balance Control Method for Multi-port Grid-tied Inverter with Square-wave-voltage Multilevel Converter and Active Power Filter Connected in Series

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This paper proposes a multi-port grid-tied inverter in order to reduce the power conversion loss. The proposed circuit consists of a multilevel converter, a series active filter, and a full bridge inverter. In the proposed circuit, the number of inductors are reduced from four to two compared to conventional circuit. In addition, a voltage balance controller is proposed in order to keep the capacitor voltage. The simulation results confirm that the total harmonic distortion (THD) of the output current is less than 0.17%. Furthermore, capacitor voltage is balanced under different the capacitance and initial voltage conditions.

Keywords Multi-port converter, Series active power filter, Constant capacitor voltage control

1. Introduction

With renewable energy, the generated electric power fluctuates due to the weather conditions. In order to level the generated power, energy storage systems such as a battery and a double-layer capacitor are required [1]. In general, a power conversion system is employed in a grid-tied inverter with a boost-up chopper and a DC-AC converter to connect the PV modules and the battery to the single-phase grid system. However, the power conversion system has the problems which are the increase in the power conversion loss and the circuit volume due to the boost and grid tied inductors. A multi-port converter has been actively researched in order to reduce the conversion loss and the circuit volume [2-4]. However, it cannot reduce the number of a inductor because of the grid-tied inverter is required.

This paper proposes a multi-port grid-tied inverter which to reduce both the circuit volume and the power conversion loss. Only an active power filter and an output filter use the inductor. Therefore, the circuit volume of the power converter is reduced. In addition, a capacitor voltage control is proposed in order to keep the voltage in each cell. Moreover, the simulation results confirm that the operation of the proposed circuit and capacitor voltage control method.

2. Proposed circuit and capacitor voltage control

2.1 Proposed circuit

Fig. 1 shows the configuration of the proposed circuit. The proposed circuit consists of a square-wave-voltage multilevel converter, an active power filter, and a full bridge inverter. Furthermore, the square-wave-voltage multilevel converter consists of the two cells (Cell A-B), and the active filter consists of the two cells (Cell C-D).

Fig. 2 shows the operation principle of the proposed circuit. Fig. 2(a) shows the input voltage of the full bridge inverter and the

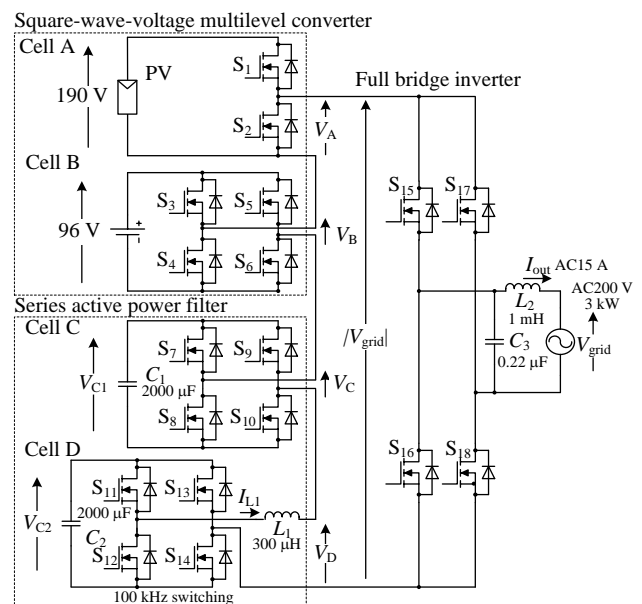
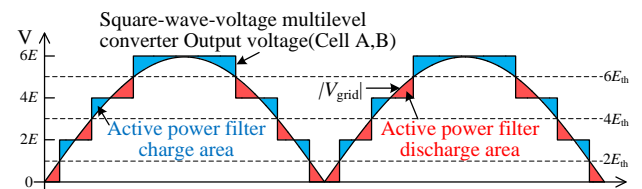
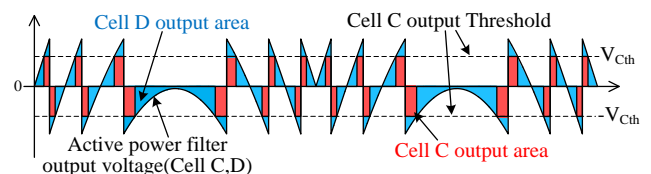


Fig. 1. Circuit configuration of proposed circuit.



(a) $|V_{grid}|$ and Cell A, B output voltage.



(b) Cell C and active filter output voltage.

Fig.2. Conceptual diagram of proposed circuit operation.

output voltage of the Cell A and the Cell B, whereas Fig. 2(b) shows the operation waveforms of the active power filter output voltage. In Fig. 2 (a), the square-wave-voltage multi-level converter outputs four level voltage which is synchronized with full-wave rectification of the grid voltage. In Fig. 2(b), the series active power filter operates to remove the harmonic components of the four level voltage waveform which is output by the Cell A and the Cell B. In consequence, the square-wave-voltage multilevel converter and the active power filter output full-wave rectified waveform. Next, the full bridge inverter converts the full-wave-rectification voltage waveform into the sinusoidal voltage waveform, i.e. the switching frequency of twice grid frequency. Therefore, the converter loss is reduced by the proposed circuit due to low switching loss. In addition, the inductor volume is also reduced because the inductor voltage becomes the difference between the grid voltage and multilevel square wave voltage.

Fig. 3 shows the block diagram of an inductor current control of Cell D. A waveform of the Cell A-D output current is required full-wave rectified waveform. Therefore, in the inductor current control is provided command that the full-wave rectified waveform. Thus, voltage and current that full-wave rectified waveform, output by the all cell.

2.2 Capacitor Voltage Control Method

In the proposed circuit, the capacitor voltage balance control and average control are implemented in order to stabilize the capacitor voltage.

Fig. 4 shows the control block diagrams for the proposed circuit. In Fig. 4(a) shows the capacitor voltage average control of the Cell C and the Cell D, whereas Fig. 4(b) shows the capacitor voltage balance control of the Cell C and the Cell D. In the capacitor voltage average control, the total capacitor voltage of V_{C1} and V_{C2} is stabilized. The threshold value $2E_{th}$, $4E_{th}$, and $6E_{th}$ is controlled in order to match the red area and the blue area in Fig. 2(a). In the capacitor voltage balance control, the Cell C outputs the threshold value V_{Cth} in order to match the red area of the positive and the red area of the negative in Fig. 2(b). On the other hand, the capacitor in Cell D, match the blue area of the positive and the blue area of the negative in Fig. 2(b) is required. The capacitor voltage of Cell D is determined by the total voltage of the two cells and the capacitor voltage of Cell C. The total voltage of the two cell are determined by capacitor voltage average control, whereas the capacitor voltage of Cell C is determined by the capacitor voltage balance control. Therefore, the Cell C and the Cell D of the capacitor voltages are balanced by two voltage controls.

3. Simulation Results

The fundamental operation of the proposed circuit and capacitor voltage control are verified by simulation. In the simulation, the ideal voltage sources are applied as the power supplies in square-wave-voltage multilevel converter. In addition, the capacitor voltage commands v_{c1}^* and v_{c2}^* are set to 32 V.

Fig. 5 shows the operation waveforms of the steady state and the transient state. In Fig 5, the Cell A-D output voltage is confirmed that the full-wave rectified waveform. Moreover, the total harmonic distortion (THD) of the output current is 0.17%. In addition, the capacitor voltage V_{C1} and V_{C2} includes the ripple voltages. The ripple voltage ΔV_{C1} and ΔV_{C2} have 12.6 V and 5.88 V. The ripple voltage which fluctuates at twice grid frequency is caused by the capacitor voltage control. At the transient state, the output current

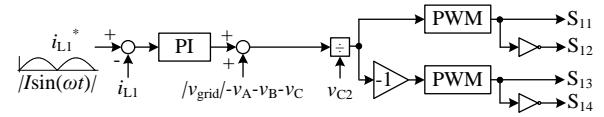
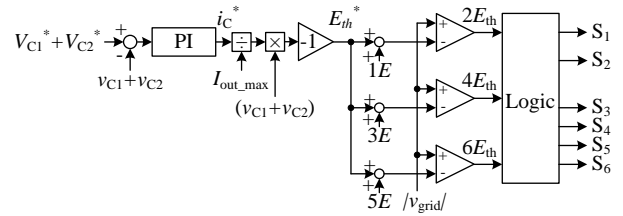
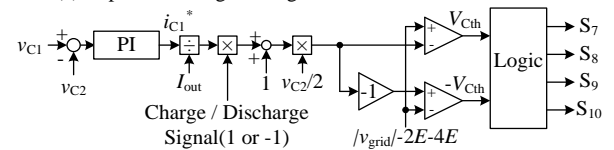


Fig. 3. Block diagram of the Cell D with inductor current control.



(a) Capacitor voltage average control of Cell C and Cell D.



(b) Capacitor voltage balance control of Cell C and Cell D.

Fig. 4. Control block diagrams of the proposed circuit.

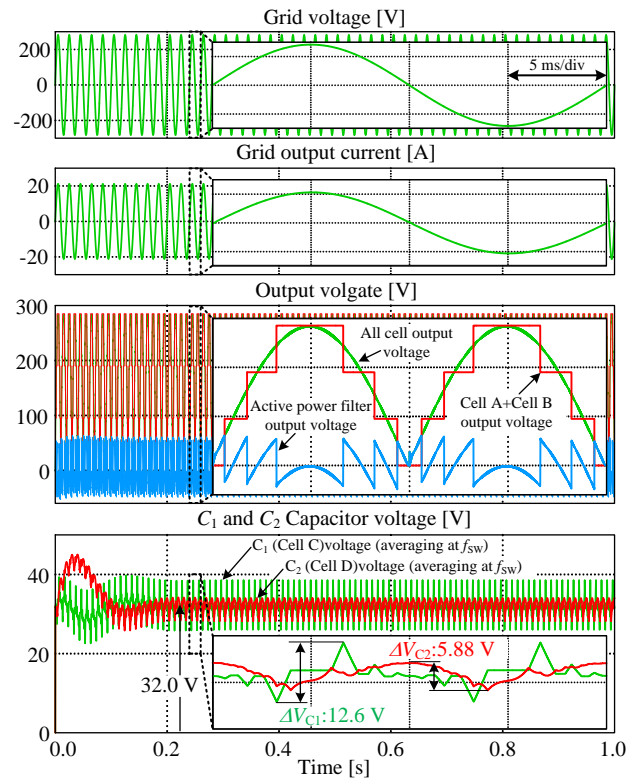


Fig. 5. Waveforms of the simulation results.

is also sinusoidal waveform. Thus, the validity of the capacitor voltage control is confirmed by simulation.

In the future work, the verification of the proposed circuit will be conducted by an actual prototype circuit

References

- [1] N. Kawakami, et al: ICRERA, pp. 1 - 5, (2012)
- [2] A. Bhattacharjee et al: "Review of Multi Port Converters for Solar and Energy Storage Integration", IEEE Trans. PELS, Early Access, (2018)
- [3] B. G. Dobbs, et al: IEEE Trans. PELS, Vol.1, No.1, pp. 6-9, (2003)
- [4] H. Zhu, et al: IEEE Trans. IE, vol.62, no. 8, pp. 4937-4947, (2015)