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Paper

Open-loop-based Island-mode Voltage Control Method for Single-phase Grid-tied Inverter with Minimized LC Filter

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This paper proposes an island-mode voltage control method using an open-loop control that applies a high-gain disturbance observer (DOB) for a single-phase inverter with a low-capacitance output filter. The output voltage is distorted with low capacitance obtained from the conventional method that consists of a PID regulator for an automatic voltage regulator and a PI regulator for an automatic current regulator. To compensate for the output voltage distortion, the high-gain DOB for the output voltage is applied for open-loop-based voltage control. DOB is implemented into a field-programmable gate array with high-speed sampling. In the LC filter of a 1-kW prototype, the impedance of the inductor is minimized to 1.0% of the normalized inverter impedance, whereas the admittance of the capacitor is reduced to 0.25% of the normalized inverter admittance. Using the proposed method, the inverter output voltage total harmonic distortion is reduced by 82.4% even with the diode rectifier load compared to conventional voltage control, whereas the constant output voltage is achieved regardless of load conditions.

Keywords : Grid-tied inverter, Island-mode, Minimized LC filter, Open-loop-based voltage control

1. Introduction

In recent years, grid-tied inverters such as photovoltaic systems, fuel cell systems, and wind turbine systems have been actively studied for energy conservation [1-3]. An inverter must have a small volume to increase the power density of the system [4, 5]. Because interconnected inductors account for most of the inverter size, it is desirable to reduce the size of the interconnected inductors. By reducing the inductance, it is possible to reduce the volume of the inductor. This can be achieved using high switching frequency silicon carbide (SiC) or gallium nitride (GaN)-based devices, applied using the same current ripple. Moreover, the capacitance of the filter capacitor can be reduced by designing a filter with a high cutoff frequency. Therefore, it is possible to apply a high resonance frequency output filter for the inverter by increasing the switching frequency. On the other hand, the inverter output current overshoot rate becomes high during the voltage sag when the inductance of the interconnected inductor is reduced. Thus, the authors propose a high-speed gate-block method and the design of an LC or LCL filter to meet the fault ride-through (FRT) requirements [6, 7]. In particular, to meet the FRT requirements, a filter capacitor with low capacitance is designed to reduce the resonance.

The grid-tied inverter is required to perform the island-mode operation to supply power to the load, when a blackout in a long period that exceeds the FRT requirements occurs [8-10]. In order to output the voltage, it is necessary to implement a voltage controller for the inverter. However, the disturbance suppression performance of the voltage controller worsens due to the low capacitance of the filter capacitor in the minimized LC filter. The inverter output voltage is distorted when the island-mode operation with low disturbance suppression performance is connected to a nonlinear load, such as a rectifier load. As a solution to this problem, the control response of the voltage controller and the current controller are increased to enhance the disturbance suppression performance. However, the increase in the control response is based on the limited detection delay time and the sampling frequency. Moreover, to improve the output voltage distortion, voltage control methods, such as an uninterruptible power supply (UPS) system, are proposed in (11), (12). It is not necessary to consider the FRT operation for the operation of a UPS. Thus, it is possible to increase the capacitance of the filter capacitor of the output filter. The voltage control methods of (11) and (12) do not consider the output of the low capacitance filter. Therefore, in the grid-tied inverter, the voltage control with low capacitance must be considered. Moreover, it is necessary to implement a complex control or sampling method for the control methods of (11) and (12).

This paper proposes a new open-loop-based island-mode voltage control method equipped with high-gain disturbance suppression in order to achieve low total harmonic distortion (THD) of the output voltage. The originality of this paper is that an island-mode voltage control with a minimized LC filter can compensate for an output error voltage for the load current without a current feedback loop. Moreover, it is not necessary to consider the interference between the voltage controller and the current controller. This control is defined as the voltage disturbance compensation open-loop control (VDCOLC) in this paper. The proposed VDCOLC compensates for the load current disturbance by using the output voltage detection value to calculate the disturbance through a high-gain disturbance observer (DOB) [13-15]. In order to compensate for the disturbance with high-speed sampling, the high-gain DOB is implemented using a field-programmable gate array (FPGA). By using this proposed VDCOLC, a reduction of THD for the inverter output voltage is confirmed with a 1-kW prototype.

2. Problem of Island-mode Voltage Control with Minimized LC Filter

Figure 1 shows a circuit configuration of a single-phase grid-tied

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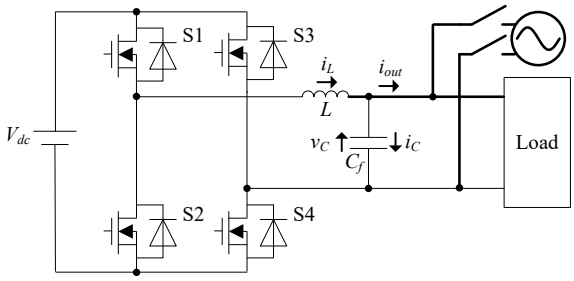


Fig. 1. Circuit diagram for island mode. In this paper, the output LC filter is minimized.

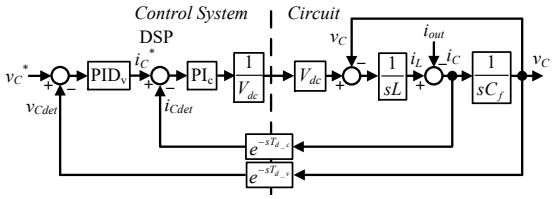


Fig. 2. Control block diagram of conventional closed-loop-based voltage control for island-mode operation. To improve the disturbance suppression performance, the control response must be increased.

inverter with an LC filter. Owing to its simplicity, an H-bridge single-phase two-level inverter is employed in this paper. In order to reduce the inverter volume, the size of the LC filter is minimized. In the island-mode operation, the output voltage is controlled by configuring the voltage controller with the filter capacitor of the output LC filter as the control object. The disturbance gain of the output current i_{out} $G_D(s)$ when the voltage controller is constructed using a PI controller is expressed as

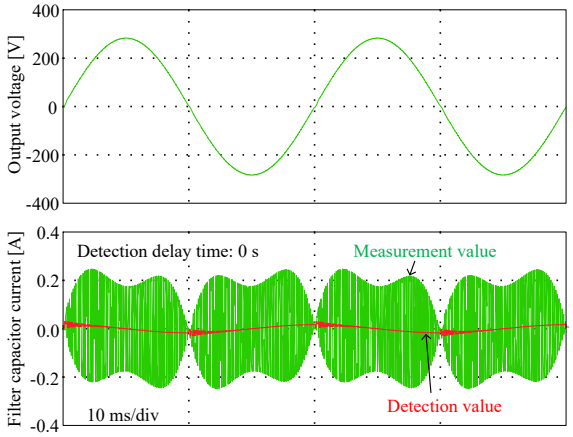
$$G_D(s) = \frac{s}{s^2 C_f + sK_p + \frac{K_p}{T_i}} \quad \text{..... (1),}$$

where C_f is the capacitance of the filter capacitor; K_p is the proportional gain; T_i is the integral time; s is the Laplace operator; and the current control gain is unity. The disturbance suppression performance worsens due to the increase in the disturbance gain when the capacitance of the filter capacitor C_f is decreased in (1). Thus, it is necessary to improve the disturbance suppression performance to achieve the island-mode operation with the minimized LC filter.

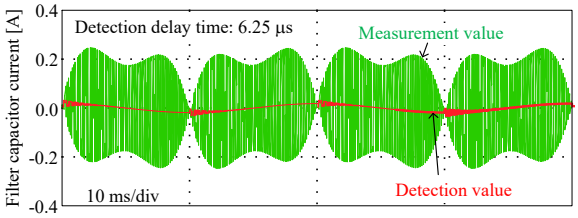
3. Open-loop-based Voltage Control for Island-Mode Operation

3.1 Current Detection Problem of Filter Capacitor

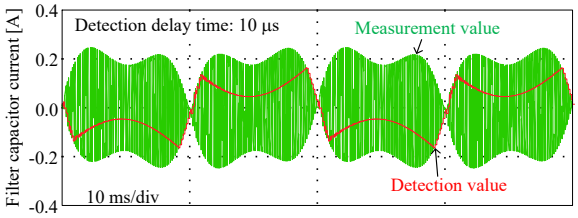
Figure 2 shows a conventional closed-loop-based island-mode voltage control with a current controller consisting of a PI regulator. In general, island-mode voltage control is carried out by a voltage controller that has an inner loop of the current controller. Note that the disturbance suppression performance is improved by using the filter capacitor current control [16]. The disturbance for the voltage controller, such as the load current, is included in the filter capacitor current. Thus, the disturbance compensation for the output voltage controller is not necessary by the filter capacitor current feedback control. Moreover, it is necessary to increase the control response, which is limited due to the controller hardware, to achieve the island



(a) Without current detection delay time.



(b) Current detection delay time is half the carrier period.



(c) Current detection delay time is not half the carrier period.

Fig. 3. Comparison of filter capacitor current detection with different current detection delay time.

mode with the minimized LC filter.

Figure 3 shows the filter capacitor current detection value under the same output voltage with different detection delay time of the filter capacitor current, where the impedance of the interconnected inductor is 1.0% of the normalized inverter impedance, and the admittance of the filter capacitor is 0.25% of the normalized inverter admittance in the 1-kW system. The detection of the filter capacitor average current for one switching period is required, as shown in Fig. 2. However, the filter capacitor current has a large current ripple when the low capacitance of the filter capacitor is applied, because the switching frequency becomes higher than the fundamental frequency component of the output current. Thus, it is impossible to detect the filter capacitor average current per the switching period due to the current detection delay time. In Fig. 3 (a) and (b), it is possible to detect the average filter capacitor current as a sinusoidal wave when the detection delay time is 0 s or half the carrier period (6.25 μs). However, the detection point of the output current is different from the average value, i.e., the filter capacitor current detection value becomes a non-sinusoidal wave when the detection delay time of the filter capacitor current becomes longer, as shown in Fig. 3(c) as 10 μs. Thus, it is impossible to detect the filter capacitor average current due to the above problem. As a result, the inverter output voltage THD becomes worse. It is necessary to apply multirate sampling for the average capacitor

current detection [11, 12] to solve above problem.

3.2 Proposed Open-loop-based Island-mode Voltage Control

The resonant frequency of the filter is shifted to the high frequency range when the LC filter is minimized. The transfer function for the output voltage command with the open-loop operation $G_{com\_OL}(s)$ is expressed as

$$G_{com\_OL}(s) = \frac{1}{s^2 LC_f + 1} \quad \text{..... (2).}$$

The transfer function becomes wide bandwidth for the output voltage command v_c^* with the minimized LC filter by (2). Therefore, an open-loop-based voltage control can be employed without the occurrence of the output voltage resonance. Nevertheless, the output voltage with the open-loop-based voltage control varies highly, dependent on the load, because the output voltage is not fed back and is not regulated by the voltage controller. Furthermore, an odd number of harmonic components occur in the output voltage due to the nonlinear output current when a diode rectifier load is connected to the inverter. Therefore, it is necessary to compensate for the disturbance of the output current to obtain a stable and constant output voltage regardless of the load.

Figure 4 shows the conventional open-loop-based island-mode voltage control with typical dead-time compensation. The output voltage error due to the dead-time error voltage is compensated by using this method. However, the harmonic components due to a nonlinear load, such as the diode rectifier, cannot be compensated.

Figure 5 shows the proposed VDCOLC. In order to achieve high-gain compensation, the compensator is implemented by an FPGA. Moreover, the compensator is operated as a DOB that compensates for the disturbance due to the output current i_{out}. The disturbance estimation value $\hat{v}_{dis}$ is expressed by

$$\hat{v}_{dis} = \frac{\omega_c}{s+\omega_c} v_{conv}^* - \frac{\omega_c}{s+\omega_c} v_{cdet} \quad \text{..... (3),}$$

where ω_c is the cutoff angular frequency of the DOB; v_{conv}^* is the voltage command after the disturbance compensation; and v_{cdet} is the detection value of the filter capacitor voltage.

Moreover, a grid-tied inverter is disconnected from the grid when a blackout or a long period voltage sag occurs in the grid and the inverter is only connected to the load. Switching behavior from grid-tied to island operation is determined by detection of the blackout or the long period voltage drop. The transition of the grid-tied operation to island-mode operation is carried out when the following conditions are detected: (i) drop of the grid voltage below the threshold of the voltage drop defined by the FRT requirements, such as the E.ON grid code [17]; (ii) occurrence of a long period voltage drop exceeding the FRT operation duration defined in the FRT requirements [17]. Thus, the voltage source inverter (VSI) control is switched from the grid-tied operation with the current control to the proposed voltage control for the island operation mode when the above conditions are detected. Moreover, the proposed island mode operates with the DOB to obtain the sinusoidal waveforms based on the voltage command. Therefore, it is possible to supply the power to the load during the transition operation because the output voltage and frequency commands are the same as the grid voltage and grid frequency. However, when a nonlinear load, such as a diode rectifier load, is connected, an inrush current prevention method, such as an initial charge circuit or an output current limiter, is necessary to stabilize the inverter operation.

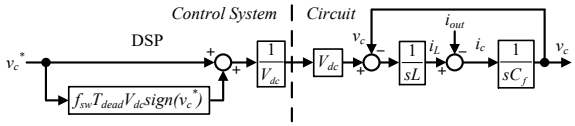


Fig. 4. Control block diagram of conventional open-loop-based island-mode voltage control for island-mode operation.

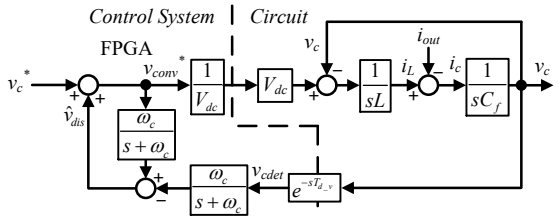


Fig. 5. Control block diagram of proposed VDCOLC for island-mode operation. To compensate for the output voltage in the high-gain, the DOB is implemented using an FPGA.

3.3 Application Area of Proposed Open-loop-based Voltage Control for Island Mode

In the disturbance compensator of (3), the low-pass filter (LPF) is implemented into the DOB in order to suppress the resonance components of the LC filter for the voltage command in the voltage controller. The resonant frequency of the LC filter f_{res_LC} is expressed as

$$f_{res\_LC} = \frac{1}{2\pi\sqrt{LC_f}} \quad \text{..... (4).}$$

In order to reduce the resonance component of the LC filter by using an LPF, the cutoff frequency of the LPF is designed to be less than 1/10 to 1/2 for the resonant frequency of the LC filter f_{res_LC}. Thus, it is possible to reduce the effect of the LC filter resonance. However, in order to increase the performance of the disturbance compensator, it is necessary to increase the cutoff frequency of the LPF. Due to the output current disturbance caused by the diode rectifier load, the odd-order harmonic components are included in the inverter output voltage. For instance, when considering the reduction of the harmonics to 11th order for the fundamental wave of the output voltage, the 11th order harmonic wave is 550 Hz when the fundamental wave is 50 Hz. Thus, it is necessary to increase the LPF cutoff frequency of the DOB to greater than 550 Hz. Therefore, in order to consider the suppression of the harmonics to k order, the proposed method is applied subject to the following condition:

$$kf_{out} < f_c < \frac{f_{res\_LC}}{n}, \quad \left(n: 2 \sim 10, f_c = \frac{\omega_c}{2\pi} \right) \quad \text{..... (5),}$$

where f_{out} is the frequency of the output voltage; and n is the ratio for the resonant frequency of the LC filter f_{res_LC}, which implies a DOB cutoff frequency from 1/10 to 1/2 for the resonant frequency of the LC filter. In this paper, the resonant frequency of the LC filter is approximately 10 kHz, where L is 1.29 mH (%Z = 1.0%), and C_f is 0.2 μF (%Y = 0.25%); therefore, if k is eleven, it is possible to meet (5). Furthermore, to compensate for the 11th order harmonic without interfering with the resonant frequency of the LC filter, the DOB cutoff frequency is set to 2 kHz.

Figure 6 shows the comparison of the disturbance gain characteristics of a conventional closed-loop-based voltage control and the proposed VDCOLC. The controller of the conventional method is similarly constructed as in Fig. 2, where the angular

frequency of the voltage controller is 3000 rad/s, and the angular frequency of the current controller is 30000 rad/s. Moreover, the disturbance suppression gain is calculated from the transfer function, where the output current i_{out} is the input, and the output voltage v_c is the output. Furthermore, the disturbance suppression performance is analyzed by sweeping the frequency of the disturbance suppression gain from 1 Hz to 100 kHz, as shown in Fig. 6; the disturbance gain is reduced with the proposed control from 30 Hz to 1 kHz of the disturbance frequency, which includes the harmonic components from 1st to 20th for the fundamental frequency of the output voltage. Thus, it is possible to reduce the output voltage distortion by using the proposed method.

4. Simulation Results for Proposed VDCOLC

Table 1 shows the simulation conditions for the proposed method. The LC filter parameter and the DOB cutoff frequency are changed in the simulation results.

Figure 7 shows the simulation results of the proposed method with the diode rectifier load. In Fig. 7(a), it is possible to suppress the inverter output voltage THD to less than 5.0%, when the resonant frequency of the LC filter is 10 kHz (L = 1.29 mH; %Z = 1.0%, C_f = 0.2 μF; %Y = 0.25%), and the DOB cutoff frequency is 2 kHz. The LC filter parameter is designed to suppress the output current overshoot with low inductance during the voltage sag [7]. In order to reduce the resonance of the output current at the voltage fluctuation, the capacitance of the filter capacitor is designed to be small. The inverter output voltage THD is 1.56%. Moreover, with the DOB cutoff frequency lower than the resonant frequency of the LC filter, it is possible to reduce the resonance component in the inverter output voltage. Thus, the resonance component of the inverter output voltage in Fig. 7(a) does not occur, i.e., the condition of Fig. 7(a) meets (5). In Fig. 7(b), the resonant frequency of the LC filter and the DOB cutoff frequency are 2 kHz. The inverter output voltage THD is higher than 5%; in addition, the resonance occurs in the inverter output voltage. This is because the condition of Fig. 7(b) does not meet (5), i.e., the LC filter resonance component is included in the voltage command. In Fig. 7(c), the resonant frequency of the LC filter is 10 kHz and the DOB cutoff frequency is 200 Hz. The inverter output voltage THD is higher than 5.0% in this condition. This is because the disturbance suppression performance of the DOB decreases due to the low DOB cutoff frequency. Thus, the inverter output voltage THD is worse for the diode rectifier load due to the disturbance. In addition, the dead-time error voltage compensation by the DOB is not effective enough due to the low DOB cutoff frequency. In Fig. 7(d), the resonant frequency of the LC filter is 2 kHz and the DOB cutoff frequency is 200 Hz. The inverter output voltage THD is also higher than 5.0% in this condition. The inverter output voltage includes the distortion due to the low resonant frequency of the LC filter. Furthermore, the disturbance compensation value is not effective enough for the diode rectifier load due to the low DOB cutoff frequency. Thus, the inverter output voltage THD in Fig. 7(d) is higher than the condition of Fig. 7(c). In conclusion, the proposed method can only be applied in the area of (5).

5. Experimental Results

In the experimental verification of the island-mode operation, three cases of load test are considered. The load conditions are as follows:

(a) No-load.

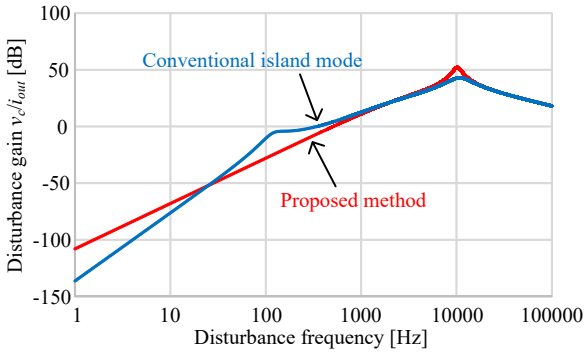


Fig. 6. Characteristics of disturbance gain from output current i_{out} to output voltage v_c. The resonance due to the controller is effected to the output voltage distortion with the conventional method.

Table 1. Simulation conditions.

Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	80 kHz
DC link vol.	V_{dc}	380 V	Samp. fre. of DOB	f_{so}	80 kHz
Output volt. command	v_c^*	200 V_{rms}	Crest factor of load		3.0

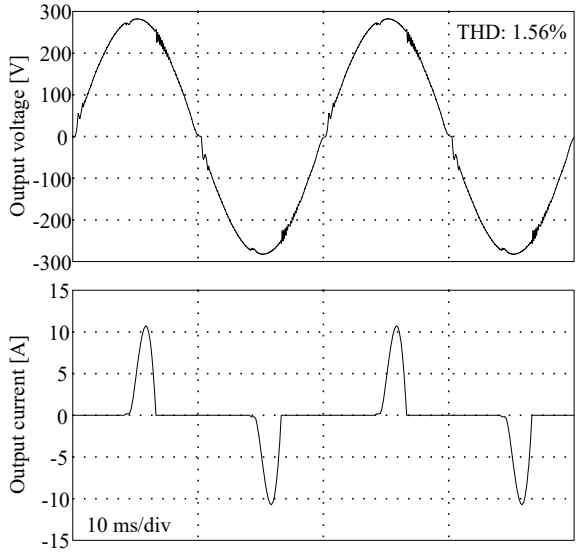
(b) Linear load, such as resistance load.

(c) Nonlinear load, such as diode rectifier load.

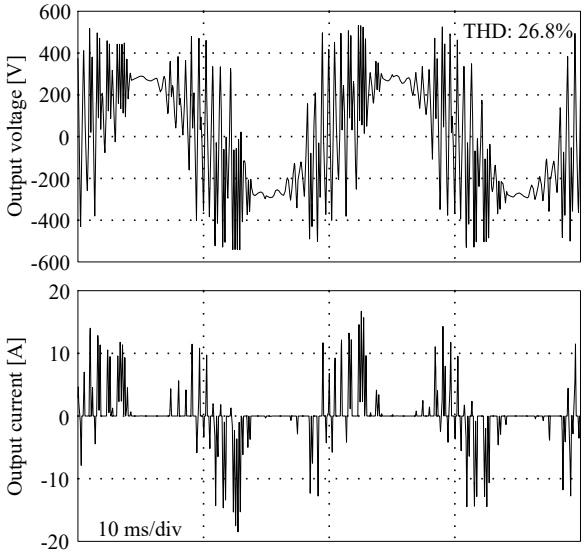
Table 2 shows the experimental conditions. By considering the frequency of the voltage command as 50 Hz, the angular frequency of the voltage controller for the conventional closed-loop-based island-mode voltage control is designed to ten times the voltage command frequency. Thus, the angular frequency is set to 3000 rad/s. Moreover, in order to prevent interference, the angular frequency of the current controller is designed to ten times the angular frequency of the voltage controller. Thus, the angular frequency of the current controller is set to 30000 rad/s. Note that the minimized LC filter parameter is designed such that the FRT requirements are met during the voltage sag [7]. The island-mode operations are compared with the conventional closed-loop-based voltage control, the conventional open-loop-based island mode with dead-time error compensation, and the proposed VDCOLC.

5.1 No-load Operation

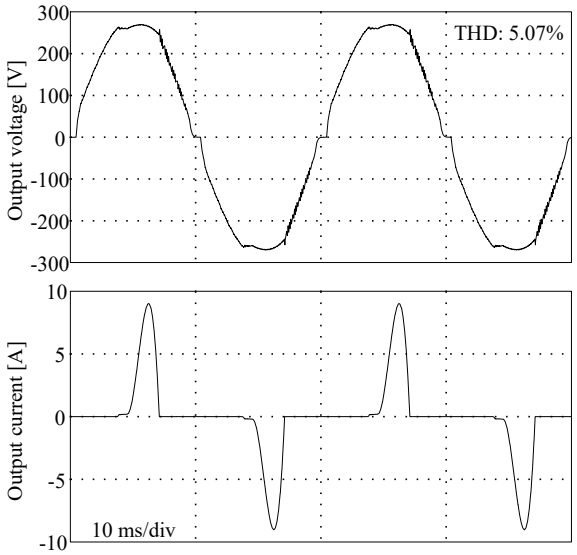
Figure 8 shows the experimental results for the no-load operation. In Fig. 8(a), (b), and (c), the output voltage THD of the three methods are suppressed to less than 5.0%. However, the inverter output voltage THD in Fig. 8(a) is high in the conventional closed-loop-based voltage control. This is because the filter capacitor current detection has a delay time that is different from the half period of the carrier, as shown in Fig. 3(c). Thus, it is impossible to detect the average value for the filter capacitor current. Therefore, the inverter output voltage is distorted in Fig. 8(a). In particular, the distortion of the inverter output voltage with the proposed method is reduced by 70.2% compared with the conventional closed-loop-based voltage control. In addition, the output voltage in Fig. 8(a) is higher than the voltage command due to the high gain of the current controller. In order to regulate the output voltage in Fig. 8(a), it is necessary to reduce the gain of the current controller. Moreover, the output voltage in Fig. 8(b) is also higher than the voltage command due to typical dead-time compensation. The dead-time error voltage does not occur in the no-load operation. Thus, the output voltage increases by the dead-time compensation value. On the other hand,



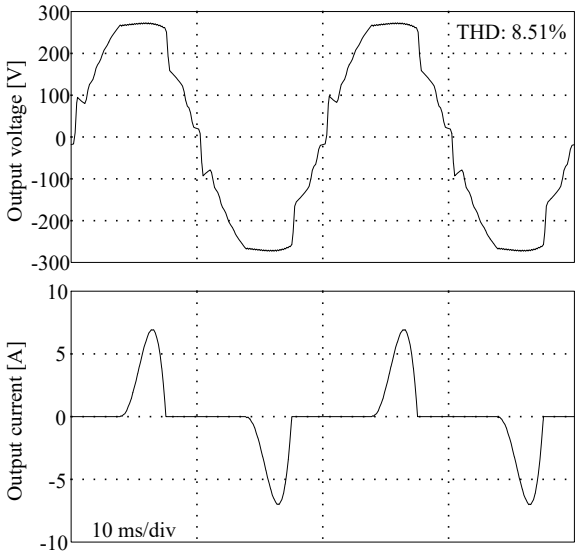
(a) With high-resonant frequency LC filter.



(b) DOB cutoff frequency and LC filter resonant frequency are the same.



(c) With high-resonant frequency LC filter and low-DOB cutoff frequency.



(d) DOB cutoff frequency and LC filter resonant frequency are low.

Fig. 7. Simulation results for any condition of resonant frequency of LC filter and DOB cutoff frequency with the proposed VDCOLC. The inverter output voltage THD is suppressed to less than 5% when (5) is met.

the output voltage in Fig. 8(c) is almost same compared with the voltage command.

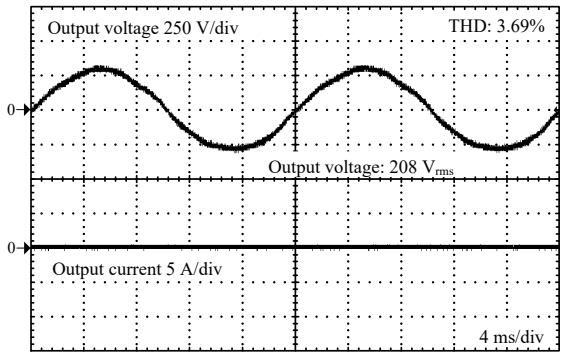
5.2 Linear-load Operation

Figure 9 shows the experimental results for the linear load operation. In Fig. 9(a), (b), and (c), the output voltage THD at the rated power with three methods are also suppressed to less than 5.0%. The inverter output voltage THD in Fig. 9(a) is high compared with both methods of Fig. 9(b) and (c), for the same reason as in Fig. 8(a). In particular, the inverter output voltage THD with the proposed method is improved by 61.4% compared with the conventional closed-loop-based voltage control at the rated load. In addition, the output voltage in Fig. 9(a) is higher than the voltage command for the same reason as in Fig. 8(a). Moreover, the output voltage in Fig. 9(b) decreases due to the load current compared with Fig. 8(b). On the other hand, the output voltage in Fig. 9(c) is almost the same as the voltage command.

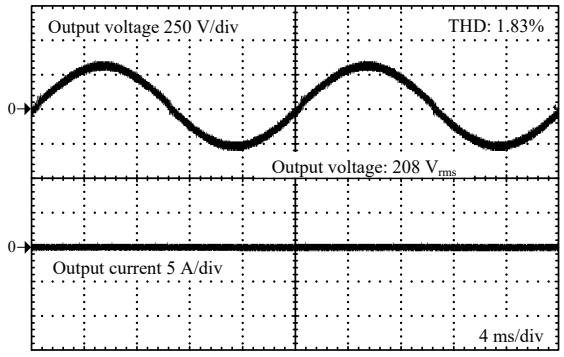
Table 2. Experimental conditions.

Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	80 kHz
DC link vol.	V_{dc}	380 V	Samp. fre. of DSP	f_s	20 kHz
Output volt. command	v_c^*	200 V_{rms}	Angl. fre. of AVR	ω_{avr}	3000 rad/s
Inter. Induc. (%Z)	L	1.29 mH (1.0%)	Angl. fre. of ACR	ω_{acr}	30000 rad/s
Filter cap. (%Y)	C_f	0.2 μF (0.25%)	Samp. fre. of DOB	f_{so}	80 kHz
			Cutoff fre. of DOB	f_c	2 kHz

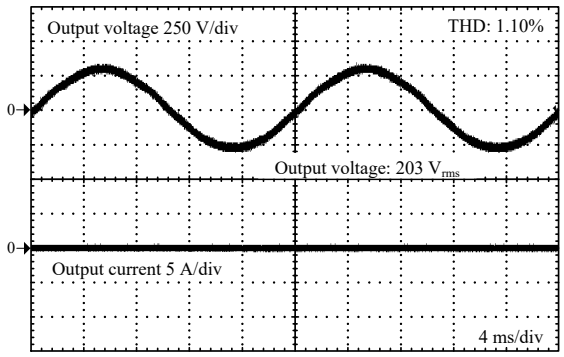
Figure 10 shows the output voltage THD characteristic and the output voltage variation against the linear load. In Fig. 10(a), the output voltage THD with the proposed method is reduced more effectively than with the conventional closed-loop-based voltage control. The maximum improvement of the output voltage THD is



(a) Conventional closed-loop-based voltage control.

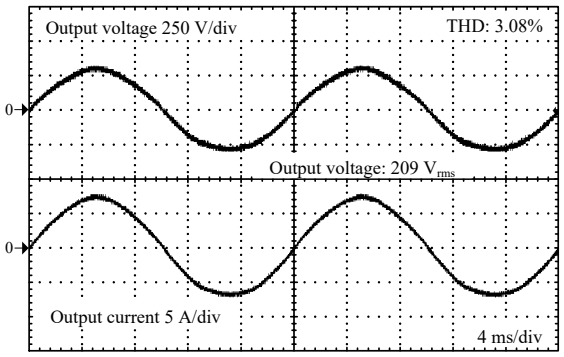


(b) Conventional open-loop-based voltage control.

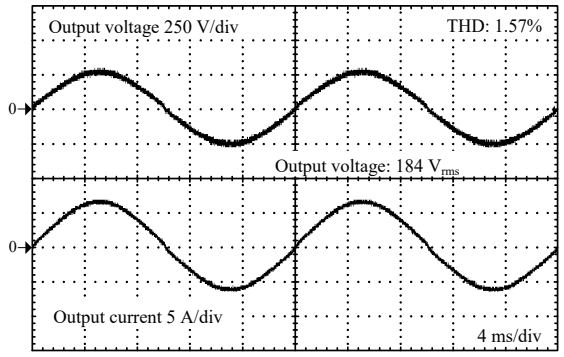


(c) Proposed VDCOLC.

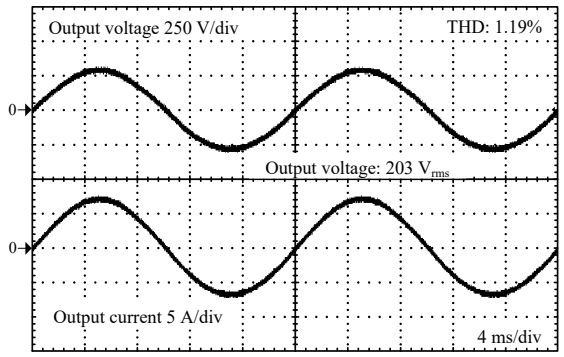
Fig. 8. Experimental results for no-load operation. The output voltage THD is suppressed to less than 5.0% in both the conventional method and the proposed method.



(a) Conventional closed-loop-based voltage control.



(b) Conventional open-loop-based voltage control.



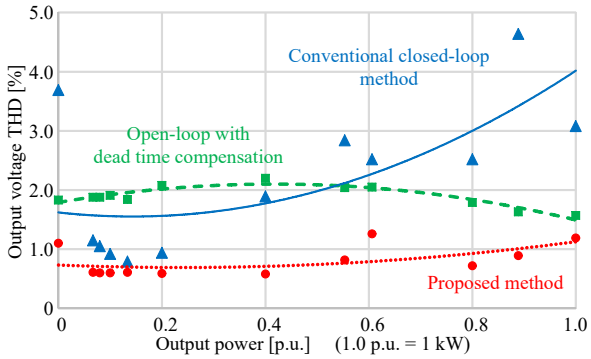
(c) Proposed VDCOLC.

Fig. 9. Experimental results for linear load operation at rated load. The output voltage THD is suppressed to less than 5.0% in both the conventional method and the proposed method.

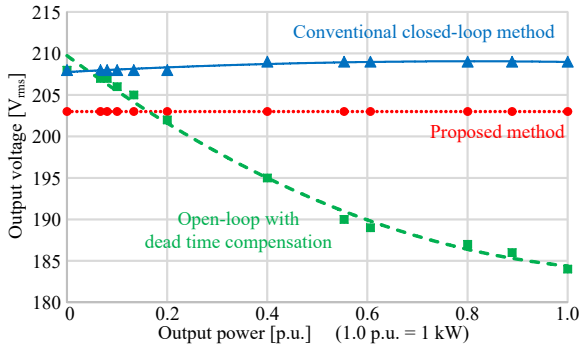
80.8% at a load of 0.9 p.u. Moreover, the inverter output voltage THD characteristic with the conventional open-loop-based island mode or the proposed method are approximately constant compared with the conventional closed-loop-based voltage control in the load range from 0 p.u. to 1.0 p.u. The cause of the difference for the inverter output voltage THD with the conventional closed-loop-based voltage control is that the variation in the load current causes the error of the filter capacitor average current detection value. Due to the detection error of the filter capacitor average current, the inverter output voltage becomes a non-sinusoidal wave. Thus, the operation of the conventional closed-loop-based voltage control becomes unstable. On the other hand, in Fig. 10(b), the inverter output voltage with the conventional closed-loop-based voltage control is almost constant in the load range from 0 p.u. to 1.0 p.u. This is because the voltage controller regulates the inverter output voltage. However, the output voltage with the conventional open-loop-based voltage control varies significantly depending on the load. This is because the inverter output voltage decreases due to the decrease in the filter capacitor current by the load current. On the other hand, the output voltage with the proposed method is constant. In the proposed control, the DOB uses the detection value of the output voltage to estimate the output current and then compensates for the disturbance of the output current. On other perspective, the output voltage is indirectly regulated by a feedback loop in the DOB. Therefore, in the proposed method, it is possible to have the inverter output a constant voltage during the island mode with a linear load.

5.3 Nonlinear-load Operation

Figure 11 shows the experimental results for the nonlinear load operation. The diode rectifier is applied as a nonlinear load. The



(a) Output voltage THD characteristic with linear load.

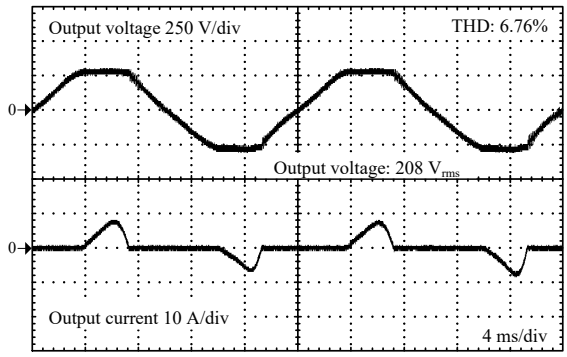


(b) Output voltage variation with linear load.

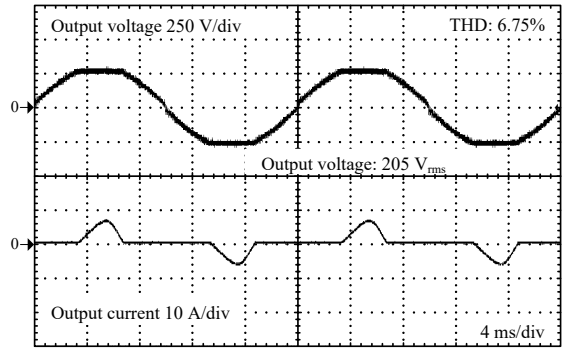
Fig. 10. Relationship between output voltage and resistive load in 1-kW system. By the proposed method, the output voltage THD is better than for the other two methods. In addition, the output voltage is constant.

crest factor of the diode rectifier load is approximately 3.0. The output voltage THD is higher than 5.0% when using the conventional closed-loop-based voltage control and the conventional open-loop-based island mode, as shown in Fig. 11(a) and (b). The inverter output voltage with the conventional closed-loop-based voltage control distorts due to the reduction of the disturbance suppression performance by the low capacitance of the filter capacitor and the error of the filter capacitor average current detection. In particular, the disturbance compensation is not effective enough for the output current control with the nonlinear load. Moreover, the inverter output voltage with the conventional open-loop-based island mode also distorts due to the non-sinusoidal output current that flows during the output voltage peak. On the other hand, by using the proposed method, as shown in Fig. 11(c), the output voltage THD is less than 5.0%. It is possible to compensate for the voltage drop due to the open-loop-based operation with the high-gain DOB in the proposed method. Thus, the inverter output voltage becomes a sinusoidal wave even with the diode rectifier load. Therefore, it is possible to suppress the output voltage THD by using the proposed method.

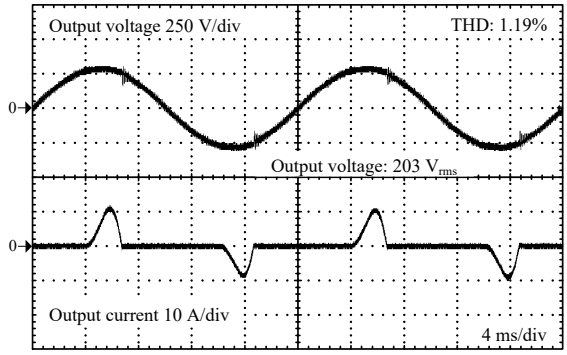
Figure 12 shows the THD characteristic and the output voltage variation against the nonlinear load. In Fig. 12(a), the output voltage THD with the proposed method is reduced more effectively than with the conventional closed-loop-based voltage control or the conventional open-loop-based voltage control. The maximum improvement of the output voltage THD with the proposed method compared with the conventional closed-loop-based voltage control at the heavy nonlinear load is 82.4%. Moreover, in Fig. 12(b), the



(a) Conventional closed-loop-based voltage control.



(b) Conventional open-loop-based voltage control.



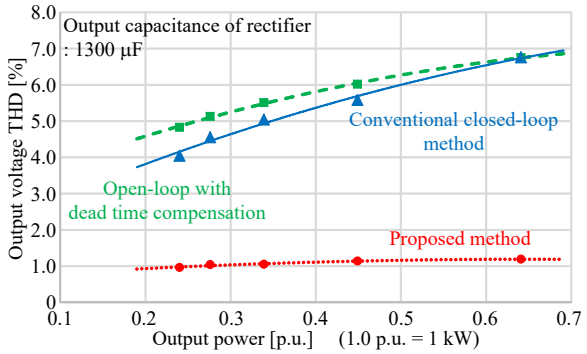
(c) Proposed VDCOLC.

Fig. 11. Experimental results for diode rectifier load operation. By using the proposed method, the output voltage THD is reduced to 1.19% with the nonlinear load.

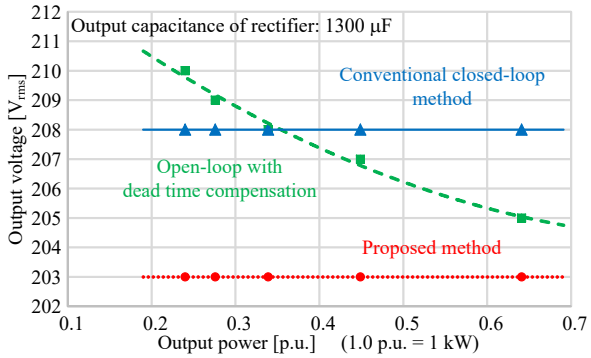
output voltage with the conventional open-loop-based island mode decreases greatly at the heavy nonlinear load. On the other hand, the output voltage with the conventional closed-loop-based voltage control and the proposed method has a constant value. Thus, in the proposed method, it is possible to have the inverter output a constant voltage during the island mode with a nonlinear load. Therefore, it is confirmed that by using the proposed method, the output voltage is constant regardless of any conditions of load, i.e., linear/nonlinear load, or light/heavy load.

6. Conclusion

This paper proposed an open-loop-based island-mode voltage control with high-gain disturbance compensation when the LC filter is minimized. Moreover, the application area of the proposed method is clarified by the DOB cutoff frequency and the resonant



(a) Output voltage THD characteristic with nonlinear load.



(b) Output voltage variation with nonlinear load.

Fig. 12. Relationship between output voltage and rectifier load in 1-kW system. By using the proposed method, the output voltage THD is suppressed to less than 5%. Moreover, the output voltage is constant.

frequency of the LC filter. By using the proposed method, the output voltage is constant in the island mode regardless of any conditions of load. Furthermore, the output voltage THD with the proposed method is suppressed to less than 5.0%. In particular, the output voltage THD was improved by 82.4% compared with the conventional closed-loop-based voltage control when the nonlinear load was connected. Therefore, the proposed method was confirmed as to the utility of the island mode with the minimized LC filter.

References

(1) Hung-I Hsieh, and Jiaxin Hou : "Realization of Interleaved PV Microinverter by Quadrature-Phase-Shift SPWM Control", *IEEJ J. Ind. Appl.*, Vol.4, No.5, pp.643-649, 2015.

(2) Luis Valverde, Carlos Bordons, and Felipe Rosa : "Integration of Fuel Cell Technologies in Renewable-Energy-Based Microgrids Optimizing Operational Costs and Durability", *IEEE Trans. Ind. Electron.*, Vol. 63, No. 1, pp. 167-177, 2016.

(3) Zhenbin Zhang, Hui Fang, Feng Gao, José Rodríguez, and Ralph Kennel : "Multiple-Vector Model Predictive Power Control for Grid-Tied Wind Turbine System With Enhanced Steady-State Control Performance", *IEEE Trans. Ind. Electron.*, Vol. 64, No. 8, pp. 6287-6298, 2017.

(4) Min Huang, Xiongfei Wang, Poh Chiang Loh, Frede Blaabjerg, and Weimin Wu : "Stability Analysis and Active Damping for LLCL-Filter-Based Grid-Connected Inverters", *IEEJ J. Ind. Appl.*, Vol.4, No.3, pp.187-195, 2015.

(5) R. Peña-Alzola and M. Liserre : "LCL-Filter Design for Robust Active Damping in Grid-Connected Converters", *IEEE Trans. Ind. Info.*, Vol. 10, No. 4, pp. 2192-2203, 2014.

(6) S. Nagai, K. Kusaka, J. Itoh : "FRT Capability of Single-phase Grid-connected Inverter with Minimized Interconnected Inductor", *in Proc. IEEE Appl. Power Electron. Conf. and Expo.* (*APEC*) 2017, No. 1800, pp. 2802-2809, 2017.

(7) S. Nagai, K. Kusaka, J. Itoh : "ZVRT Capability of Minimized-LCL-filter-based Single-phase Grid-tied Inverter with High-speed Gate-block", *in Proc. IEEE Energy Conversion Congress Expo.* (*ECCE*) 2017, No. 847, pp. 1757-1764, 2017.

(8) Rong-Jong Wai, Wen-Hung Wang, and Chung-You Lin : "High-Performance Stand-Alone Photovoltaic Generation System", *IEEE Trans. Ind. Electron.*, Vol. 55, No. 1, pp. 240-250, 2008.

(9) Kenta Sayama, Shohei Anze, Kiyoshi Ohishi, Hitoshi Haga, and Takayuki Shimizu : "Robust and fine sinusoidal voltage control of self-sustained operation mode for photovoltaic generation system", *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, pp. 1760-1765, 2014.

(10) César Trujillo Rodríguez, David Velasco de la Fuente, Gabriel Garcerá, Emilio Figueres, and Javier A. Guacaneme Moreno : "Reconfigurable Control Scheme for a PV Microinverter Working in Both Grid-Connected and Island Modes", *IEEE Trans. Ind. Electron.*, Vol. 60, No. 4, pp. 1582-1595, 2013.

(11) Mitsutoshi Ito, Reo Fujiwara, Ryunosuke Araumi, Takuma Yoshino, and Tomoki Yokoyama : "Robust digital control of single phase PWM inverter using 3MHz multi sampling method with FPGA based hardware controller", *in Proc. IEEE International Power Electron. and Motion Control Conf. - ECCE Asia*, No. P103 (2016).

(12) Atsuo Kawamura, Hiroshi Fujimoto, and Tomoki Yokoyama : "Survey on the real time digital feedback control of PWM inverter and the extension to multi-rate sampling and FPGA based inverter control", *IECON 2007 - 33rd Annual Conference of the IEEE Industrial Electronics Society*, Vol. TPC3-24, pp. 2044-2051.

(13) S. Nagai, H. N. Le, T. Nagano, K. Orikawa, J. Itoh : "Minimization of Interconnected Inductor for Single-Phase Inverter with High-Performance Disturbance Observer", *in Proc. IEEE International Power Electron. and Motion Control Conf. - ECCE Asia*, No. Wb8-06 (2016).

(14) T. Yamaguchi, Y. Tadano, and N. Hoshi : "Using a Periodic Disturbance Observer for a Motor Drive to Compensate Current Measurement Errors", *IEEJ J. Ind. Appl.*, Vol.4, No.4, pp.323-330, 2015.

(15) N. Hoffmann, M. Hempel, M. C. Harke and F. W. Fuchs : "Observer-based Grid Voltage Disturbance Rejection for Grid Connected Voltage Source PWM Converters with Line Side LCL filters", *in Proc.* IEEE Energy Conversion Congress and Expo. (ECCE), 2012, pp. 69-76, 2012.

(16) Walid R. Issa, Mohammad A. Abusara, and Suleiman M. Sharkh : "Control of Transient Power During Unintentional Islanding of Microgrids", IEEE Trans. Power Electron., Vol. 30, No. 8, 2015, pp. 4573-4584.

(17) M. Tsili, S. Papathanassiou, "A review of grid code technical requirements for wind farms", *IET Renew. Power Gener.*, Vol. 3, No. 3, pp. 308-332, 2009.

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