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**Paper**

# Discontinuous Current Mode Control for Minimization of Three-phase Grid-Tied Inverters in Photovoltaic System

Hoai Nam Le* Student member, Jun-ichi Itoh*a) Senior Member

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In this paper, a current control method for discontinuous current mode (DCM) is proposed for a three-phase grid-tied inverter to minimize inductors without worsening current total harmonic distortion (THD). In conventional continuous current mode (CCM) control, current THD increases as an inductor value is reduced because a zero-clamping phenomenon occurs due to dead-time. In the proposed DCM current control, a zero-current interval is intentionally controlled and a dead-time-induced error voltage is simply compensated with conventional dead-time feedforward compensation. The validation of the control method is confirmed by simulations and a 700-W prototype. Compared to conventional CCM current control, the current THD is reduced by 97.6% with the proposed DCM current control, whereas the inductor volume is reduced by 70%. In the experiments, the current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u. even when the inductance impedance is reduced to 0.5% of the inverter total impedance.

**Keywords** : three-phase grid-tied inverter, continuous current mode, discontinuous current mode

## 1. Introduction

In the last decade, researches on photovoltaic system (PV) have accelerated due to an increasing demand of renewable and sustainable energy sources [(1)-(4)]. In the PV system, H-bridge three-phase grid-tied inverters are generally employed as an interface between solar panels and three-phase grid. In such grid-tied inverters, a grid filter is required to connect between an output of the inverter and the grid in order to filter out the current harmonics and to meet grid current harmonic constraints as defined by standards such as IEEE-1547 [(5)-(6)]. Due to the observation that inductors in the grid filter occupy a major volume of the inverter, an inductor value of the grid filter is necessarily reduced in order to minimize the grid filter as well as the inverter. However, this reduction of the inductor value implies a design of a high switching current ripple due to a high dc-link voltage to inductance ratio. This high current ripple results in a current distortion phenomenon called zero-current clamping, where a current distortion increases notably as the switching current ripple increases [(7)].

Due to the zero-current clamping effect, the dead-time-induced error voltage exhibits a strong nonlinear behavior around zero-current crossing points. Hence, a conventional dead-time feedforward compensation method such as, e.g. two-level approximation compensation method (ACM) [(8)], cannot compensate for this nonlinear behavior of the dead-time-induced error voltage. Several compensation methods for the nonlinearity of the dead-time-induced error voltage such as an adaptive dead-time compensation method and a turn-off transition compensation method have been proposed to deal with this nonlinearity behavior and to reduce the zero-crossing current distortion [(9)-(10)]. Nevertheless, both methods exhibit the requirements which restrict the employment over a wide range of application. Adjustment mechanism parameters for the adaptive dead-time compensation must be properly tuned for each individual system [(9)]. Meanwhile, accurate device parameters, e.g. parasitic capacitances, are required for the turn-off transition compensation method [(10)].

On the other hand, a single-stage multiphase inverter is proposed with the discontinuous current mode (DCM) control in order to generate multiphase currents with only one inductor [(11)], leading to a significant inductance reduction without worsening the current total harmonic distortion (THD). However, this method requires at least one bidirectional switching device for each phase; consequently, high conduction loss of the switching devices results in low efficiency. Meanwhile, the DCM control has been also proposed for two-stage three-phase grid-tied inverters [(12)-(13)]. The notable drawback with these DCM control methods is that the DCM control in one phase is interfered with other phases; leading to the complexity of the controller due to the requirement of the interference decoupling. Different from continuous current mode (CCM) control, the interference decoupling in the DCM operation is complicate due to the DCM nonlinearity [(14)] and requires many calculation efforts of the hardware [(12)-(13)]. Hence, the application of the conventional DCM control methods is limited.

In this paper, a current control for the three-phase grid-tied inverter operated in discontinuous current mode is proposed in order to minimize the grid filter without worsening the current distortion. In order to deal with the zero-current clamping effect, the inverter is intentionally operated in DCM instead of CCM. In other words, the zero-current interval with the DCM operation is controlled, enabling a proper compensation for the nonlinear behavior. Consequently, the conventional dead-time feedforward compensation, i.e. two-level ACM, can be employed simply in order to compensate the dead-time-induced error voltage and reduce the current distortion. The novelty of the proposed DCM control method is that the control of each phase current is separated into individual intervals in order to avoid the interference between the phase currents. Therefore, the proposed

a) Correspondence to: Jun-ichi Itoh. E-mail: itoh@vos.nagaokaut.ac.jp
* Nagaoka University of Technology.
1603-1, Kamitomioka-machi, Nagaoka, Niigata, Japan 940-2188

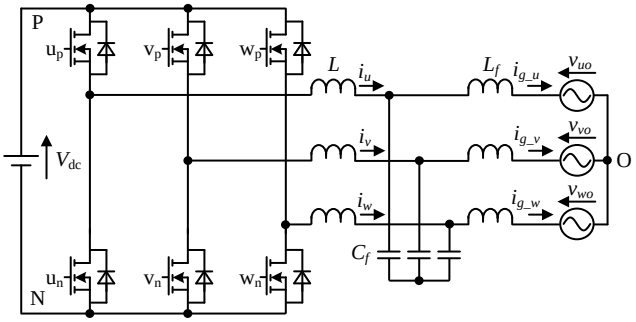
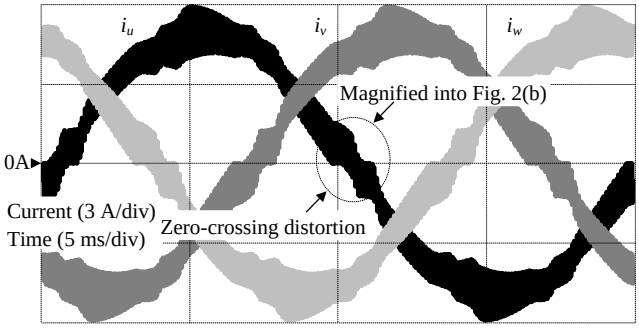
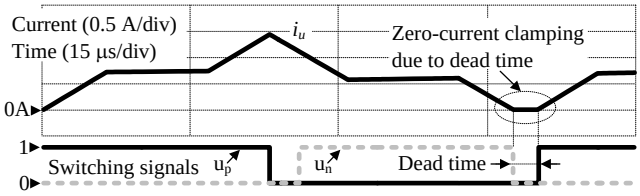



Fig. 1. H-bridge grid-tied three-phase inverter. This topology is employed due to its simple control and construction.




(a) Zero-crossing distortions in inverter output currents




(b) Zero-current clamping effect due to dead-time

Fig. 2. Zero-current distortion phenomenon. The current distortion increases with the high current ripple due to the dead-time.

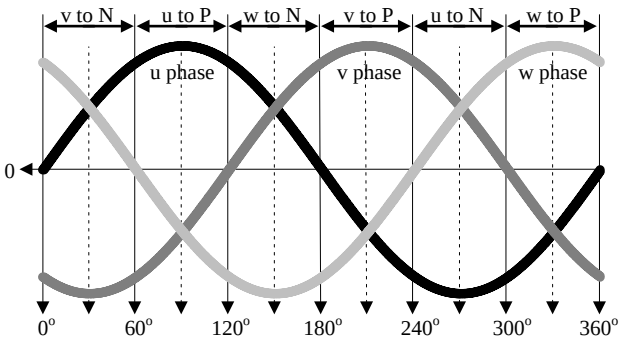
DCM control method without the interference decoupling simply achieves the sinusoidal current regulation in numerous applications. The effectiveness of the proposed current control is confirmed by simulations and experiments.

## 2. Discontinuous-current-mode current control

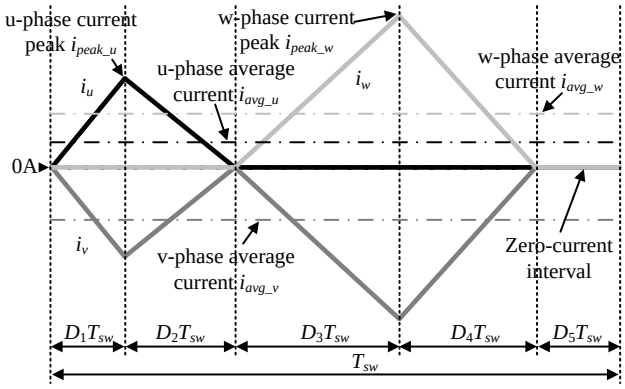
**2.1 Zero-crossing distortion** Figure 1 depicts the H-bridge three-phase grid-tied inverter with a *LCL*-based grid filter. The minimization of the *LCL* filter generates a current with a high ripple in the inductors *L*. The filter stage with $L_f$ and $C_f$ can suppress the high-order current harmonics in order to meet grid current harmonic constraints as defined by standards such as IEEE-1547 [5]-[6].

Figure 2 describes the zero-crossing current distortion phenomenon. As the current ripple increases with the minimized *LCL* filter, the current distortion increases notably around the zero-crossing points due to the zero-current clamping effect, making the dead-time-induced error voltage become nonlinear. Therefore, the employment of the conventional two-level ACM just further increases the current distortion.

**2.2 Discontinuous-current-mode operation** Figure 3 indicates the phase clamping selection in six cycles of traditional




(a) Phase clamping selection in six cycles of DPWM




(b) Inverter output current waveform in one switching period during 0°-60° region

Fig. 3. Six 60-degree time regions of DPWM and inverter output current in DCM. In order to simplifying the DCM control, DPWM is employed, controlling only two phase currents at the same time.

discontinuous pulse width modulation (DPWM), and the inverter output current waveform in one switching period during 0°-60° region. In order to simplify the control of DCM, only two phase currents should be controlled, whereas the current of the third phase is the summation of the currents of the first two phases. Hence, DPWM is employed in order to satisfy this control condition. During each 60-degree time region in DPWM, one phase is clamped to P or N polarity of dc-link voltage as shown in Fig. 3(a), whereas the other two phases are modulated to control separately two inverter output currents as shown in Fig. 3(b). The separation of the controlled currents into each individual intervals result in the elimination of the interference decoupling, which is required many calculation efforts due to the nonlinearity in DCM [14]. Hence, the proposed DCM control method leads to a simple current control and can be applied into numerous application.

**2.3 Circuit modelling** The circuit model in DCM is derived in order to generate the duty ratios. Average small signal modeling technique is used to model the inverter for the current control loop design [14].

First, considering the u-phase current in Fig. 3(b), $D_1$ and $D_2$ indicate the duty ratios of the first and the second intervals of the u-phase current, whereas $D_3$ and $D_4$ indicate the duty ratios of the first and the second intervals of the w-phase current, and $D_5$ depicts the duty ratio of the zero-current intervals. The u-phase inductor voltage in $D_1T_{sw}$, $D_2T_{sw}$ and $(D_3+D_4+D_5)T_{sw}$ is given by (1)-(3), respectively,

$$v_{Lu\_1} = V_{dc} - v_{uo} + v_{vo} \quad \text{.....(1)}$$

$$v_{Lu\_2} = \left(-v_{uo} + v_{vo}\right) \quad \text{.....(2)}$$

$$v_{Lu\_3} = 0 \quad \text{.....(3)}$$

where $V_{dc}$ is the dc-link voltage and $v_{uo}$ and $v_{vo}$ are the phase voltages. Then, the inductor voltage during a switching period is expressed by (4),

$$\begin{aligned} v_{Lu} &= D_1 v_{Lu\_1} + D_2 v_{Lu\_2} + D_0 v_{Lu\_3} \quad \text{.....(4)} \\ &= D_1\left(V_{dc} - v_{vuo} + v_{vo}\right) + D_2\left(-v_{uo} + v_{vo}\right) \end{aligned}$$

where $D_0$ is the sum of $D_3$, $D_4$ and $D_5$. The average current $i_{avg\_u}$ and the current peak $i_{peak\_u}$ shown in Figure 3 is expressed as,

$$i_{avg\_u} = \frac{i_{peak\_u}}{2}(D_1 + D_2) \quad \text{.....(5)}$$

$$i_{peak\_u} = \frac{V_{dc} - (v_{uo} - v_{vo})}{2L} D_1 T_{sw} \quad \text{.....(6)}$$

Substituting (6) into (5), and solving the equation for the duty ratios $D_2$, then the duty ratio $D_2$ is expressed by (7),

$$D_2 = \frac{4Li_{avg\_u}}{D_1 T_{sw}(V_{dc} - v_{uo} + v_{vo})} - D_1 \quad \text{.....(7)}$$

Substituting (7) into (4) in order to remove the duty ratio $D_2$ and representing (4) as a function of only the duty ratio $D_1$, (8) is obtained.

$$L\frac{di_{avg\_u}}{dt} = v_{Lu} = D_1 V_{dc} - v_{uv} + v_{uv}\left[1 - \frac{4Li_{avg\_u}}{D_1 T_{sw}(V_{dc} - v_{uv})}\right] \quad \text{.....(8)}$$

Then, the circuit model in DCM is established based on (8) [14]-[15].

Fig. 4 illustrates the circuit model of the inverter operating in DCM. The dash line part does not exist when the inverter operates in CCM because the average current $i_{avg}$ equals to the half current peak $i_{peak}/2$; in other words, the CCM operation makes the zero-current interval $D_3T_{sw}$ shown in Fig. 3 disappear. Consequently, the zero-current interval $D_3T_{sw}$ induces the nonlinearity into the transfer functions when the inverter operates in DCM, which implies that the duty ratio in DCM is a function of the current at steady-state points. Substituting the u-phase inductor voltage $v_{Lu}$ in (8) as zero and the duty ratio $D_1$ is expressed as,

$$D_1 = 2\sqrt{\frac{i_{avg\_u} L f_{sw}(v_{uo} - v_{vo})}{V_{dc}(V_{dc} - v_{uo} + v_{vo})}} \quad \text{.....(9)}$$

where $f_{sw}$ is the switching frequency. Then, substituting the u-phase inductor voltage $v_{Lu}$ in (4) as zero and the duty ratio $D_2$ is expressed as in (10),

$$D_2 = \frac{D_1(V_{dc} - v_{uo} + v_{vo})}{v_{uo} - v_{vo}} \quad \text{.....(10)}$$

Similarly, the duty ratios $D_3$ and $D_4$ of the w-phase current shown in Fig. 3(b) can be expressed as in (11)-(12),

$$D_3 = 2\sqrt{\frac{i_{avg\_w} L f_{sw}(v_{wo} - v_{vo})}{V_{dc}(V_{dc} - v_{wo} + v_{vo})}} \quad \text{.....(11)}$$

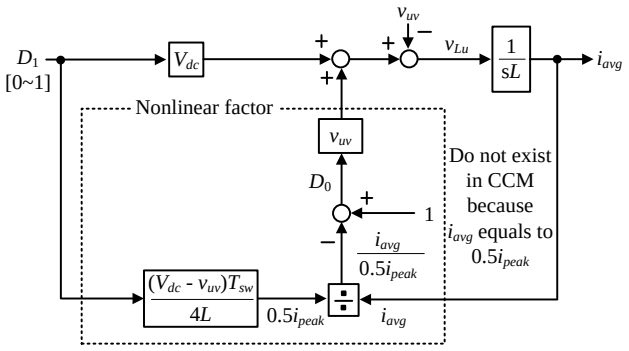



Fig. 4. Circuit model of inverter operating in DCM. The current control loop gain in DCM depends on the average current, i.e. the nonlinearities occurring in the duty-ratio-to-current transfer function.

$$D_4 = \frac{D_3(V_{dc} - v_{wo} + v_{vo})}{v_{wo} - v_{vo}} \quad \text{.....(12)}$$

**2.4 DCM control system** Figure 5 shows the control system and the control operation flowchart of the three-phase grid-tied inverter operating completely in DCM, whereas Table 1 depicts the look-up table for the duty calculation and the switching signal output in each 60-degree time region. When the grid operates normally, the inverter only has to regulate the grid current following the sinusoidal waveform.

First, the new switching period is detected by using the carrier. In the start of new switching period, the 60-degree time section is detected by detected values of the grid phase voltage $v_{uo}$, $v_{vo}$, and $v_{wo}$. Then, the phase current references and the phase voltages are distributed to input values of a duty calculation based on the detected 60-degree time section as shown in Table 1. In the DCM operation, the duty ratio can be directly calculated from the current reference. Therefore, feed-forward control method is employed for the DCM operation in this paper. In the duty calculation step, the duty ratios $D_1$-$D_5$ are expressed as follows. Note that the calculation of the duty ratios $D_1$-$D_5$ is similar to that of the duty ratios $D_1$-$D_4$ shown in Figure 3.

$$D_1 = 2\sqrt{\frac{i_{1\_ref} L f_{sw}(v_1 - v_2)}{V_{dc}(V_{dc} - v_1 + v_2)}} \quad \text{.....(13)}$$

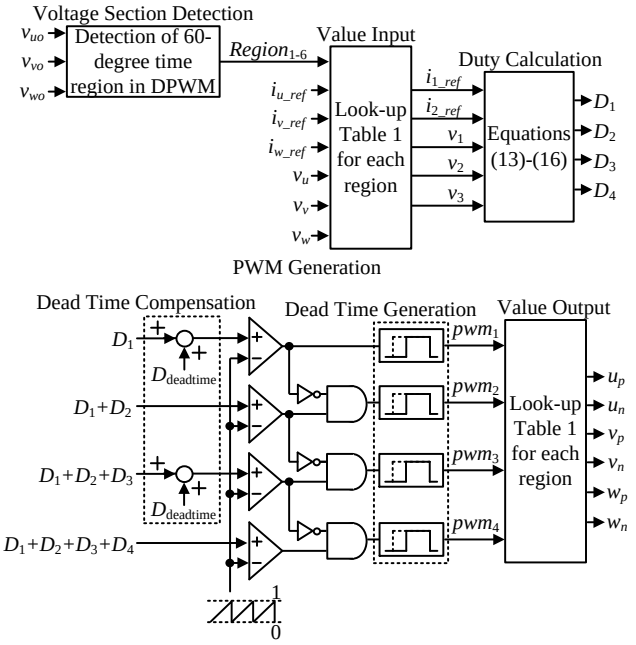
$$D_2 = \frac{D_1(V_{dc} - v_1 + v_2)}{v_1 - v_2} \quad \text{.....(14)}$$

$$D_3 = 2\sqrt{\frac{i_{2\_ref} L f_{sw}(v_3 - v_2)}{V_{dc}(V_{dc} - v_3 + v_2)}} \quad \text{.....(15)}$$

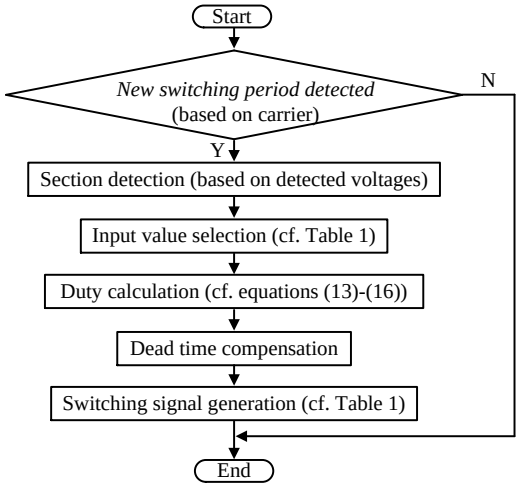
$$D_4 = \frac{D_4(V_{dc} - v_3 + v_2)}{v_3 - v_2} \quad \text{.....(16)}$$

$$D_5 = 1 - D_1 - D_2 - D_3 - D_4 \quad \text{.....(17)}$$

where $i_{1\_ref}$ and $i_{2\_ref}$ are the first and second controlled currents in each 60-degree time region, and $v_1$, $v_2$ and $v_3$ are the voltages corresponding to the controlled currents. For instance, during the 0°-60° time region, the controlled currents are $i_u$ and $i_w$ as shown in Fig. 3. Therefore, the input values to $i_1$, $i_2$, $v_1$, $v_2$, and $v_3$ are $i_{u\_ref}$,




(a) Control system




(b) Control operation flowchart

Fig. 5. Control system of the three-phase grid-tied inverter operating completely in DCM. The dead-time-induced error voltage is compensated simply when the inverter is intentionally operated in DCM because the zero-current interval is controlled.

$i_{w\_ref}$, $v_{uo}$, $v_{vo}$ and $v_{wo}$, respectively, as shown in Table 1.

Next, the dead-time compensation is introduced at the first step of PWM generation. The duty ratio which compensates for the dead-time-induced error voltage, is expressed as follow,

$$D_{deadtime} = f_{sw} T_{deadtime} \quad \text{..... (19)}$$

where $T_{deadtime}$ is the dead-time. The dead-time-induced error voltage is simply compensated as shown in Fig. 4 because when the inverter is intentionally operated in DCM, the zero-current interval is under control. The compensated duty ratios are then compared with the sawtooth waveform to generate the PWM signals. In order to avoid the simultaneous turn-on of both switching devices in one leg, the typical dead-time generation is used to delay the turn on. Finally, the PWM signals are distributed

Table 1. Look-up table for duty calculation and PWM output.

| Region / Variable | 0°-60° | 60°-120° | 120°-180° | 180°-240° | 240°-300° | 300°-360° |
|---|---|---|---|---|---|---|
| $i_{1\_ref}$ | $i_{u\_ref}$ | $i_{w\_ref}$ | $i_{v\_ref}$ | $i_{u\_ref}$ | $i_{w\_ref}$ | $i_{v\_ref}$ |
| $i_{2\_ref}$ | $i_{w\_ref}$ | $i_{v\_ref}$ | $i_{u\_ref}$ | $i_{w\_ref}$ | $i_{v\_ref}$ | $i_{u\_ref}$ |
| $v_1$ | $v_u$ | $-v_w$ | $v_v$ | $-v_u$ | $v_w$ | $-v_v$ |
| $v_2$ | $v_v$ | $-v_u$ | $v_w$ | $-v_v$ | $v_u$ | $-v_w$ |
| $v_3$ | $v_w$ | $-v_v$ | $v_u$ | $-v_w$ | $v_v$ | $-v_u$ |
| $u_p$ | $pwm_1$ | 1 | $pwm_3$ | $pwm_2$ | 0 | $pwm_4$ |
| $u_n$ | $pwm_2$ | 0 | $pwm_4$ | $pwm_1$ | 1 | $pwm_3$ |
| $v_p$ | 0 | $pwm_4$ | $pwm_1$ | 1 | $pwm_3$ | $pwm_2$ |
| $v_n$ | 1 | $pwm_3$ | $pwm_2$ | 0 | $pwm_4$ | $pwm_1$ |
| $w_p$ | $pwm_3$ | $pwm_2$ | 0 | $pwm_4$ | $pwm_1$ | 1 |
| $w_n$ | $pwm_4$ | $pwm_1$ | 1 | $pwm_3$ | $pwm_2$ | 0 |

Table 2. Simulation parameters.

| **Circuit Parameter** | | |
|---|---|---|
| $V_{DC}$ | DC link Voltage | 500 V |
| $v_g$ | Line-to-line Voltage | 200 Vrms |
| $P_n$ | Nominal Power | 3 kW |
| $f_g$ | Grid Frequency | 50 Hz |
| $Z_b$ | Total Impedance | 13.3 Ω |
| $f_{sw}$ | Switching Frequency | 40 kHz |
| $T_{deadtime}$ | Dead-time | 500 ns |
| $L_1$ | 1st Inductor Value | 1061 μH (2.5%) |
| $L_2$ | 2nd Inductor Value | 254.6 μH (0.6%) |
| $L_3$ | 3rd Inductor Value | 31.8 μH (0.075%) |
| **Current Controller Parameter** | | |
| $\zeta$ | Damping Factor | 0.7 |
| $f_c$ | Cutoff Frequency | 1 kHz |

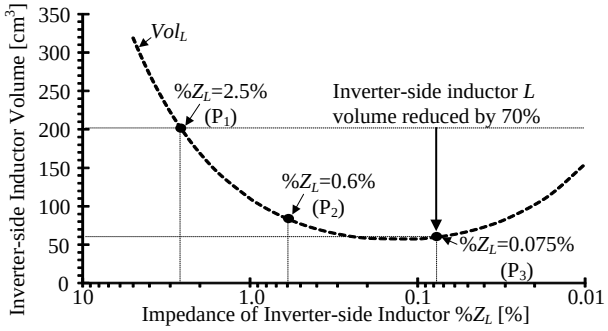
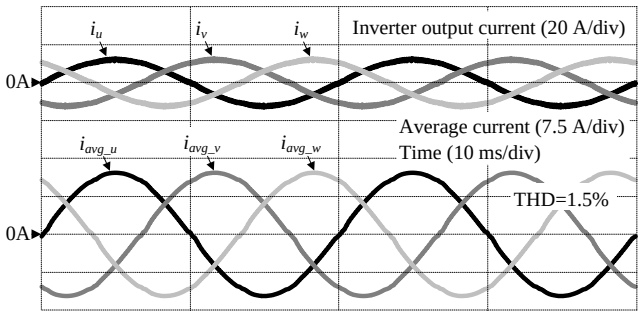



Fig. 6. Relationship between filter volume and inductor impedance at switching frequency of 40 kHz. The inductor volume can be minimized greatly when reducing the inductor impedance.

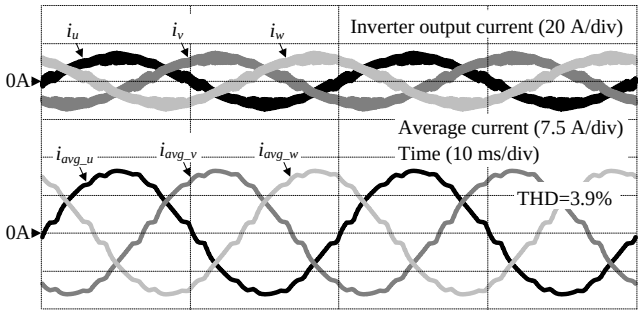
to the switching devices corresponding to each 60-degree time region of DPWM based on Table 1. Note that if the outputs $pwm_2$ and $pwm_4$ are utilized as shown in Table 1, the inverter is operated under synchronous switching; otherwise, if the outputs $pwm_2$ and $pwm_4$ are set to zero, the inverter is operated under asynchronous switching.

## 3. Simulation results

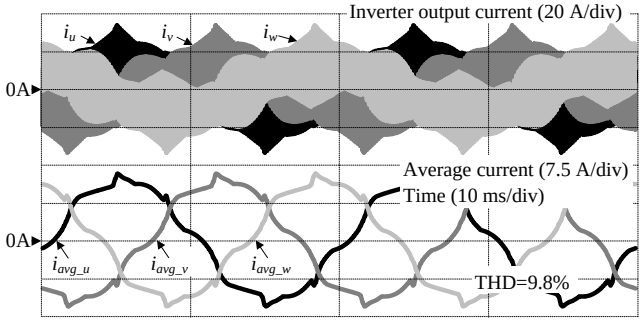
Table 2 shows the circuit parameters to evaluate the operation of the inverters, whereas Figure 6 depicts the inductor volume against the inductor impedance. The inverter-side inductors $L$ in Fig. 1 occupy a majority of the inverter volume. Therefore, the minimization of $L$ is mainly focused in this paper. Generally, the inductor value is expressed as a grid filter impedance scaled to the inverter total impedance $\%Z_L$ [16]. In particular, three designs of the grid filter impedance are evaluated. As shown in Fig. 6, the inverter-side inductor $L$ volume is minimized by 70% when the



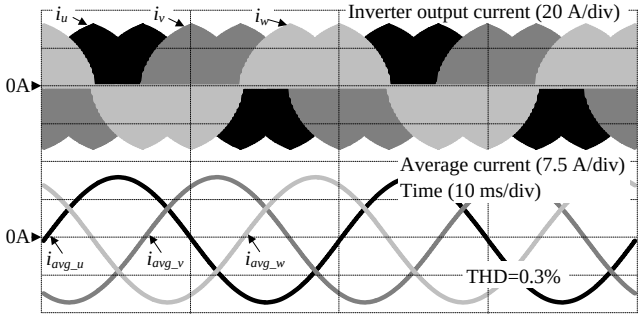

(a) Conventional CCM control with $\%Z_L$ = 2.5% at rated load




(b) Conventional CCM control with $\%Z_L$ = 0.6% at rated load




(c) Conventional CCM control with $\%Z_L$ = 0.075% at rated load




(d) Proposed DCM control with $\%Z_L$ = 0.075% at rated load

Fig. 7. Inverter output currents and average currents of conventional CCM current control and proposed DCM current control at rated load. The current THD of the conventional CCM current control increases with the reduction of the grid filter inductor impedance $\%Z_L$ is reduced from 2.5% to 0.075%.

Figure 7 shows the inverter output currents and the average currents of the conventional CCM current control and the proposed DCM current control at rated load with three inductor designs from Fig. 6. As the current ripple increases, i.e. the decrease in the inductor impedance, the current with the conventional CCM current control distorts notably around the zero-crossing points. Consequently, the current THD increases from 1.5% to 9.8% when the inductor impedance $\%Z_L$ is reduced from 2.5% to 0.075%. On the other hand, when the inverter is operated in DCM, the zero-current interval can be controlled and the dead-time-induced error voltage can be compensated simply as shown in Fig. 5. Therefore, even with the minimized inductor impedance of 0.075%, the low current THD of 0.3% is achieved with the proposed DCM current control.

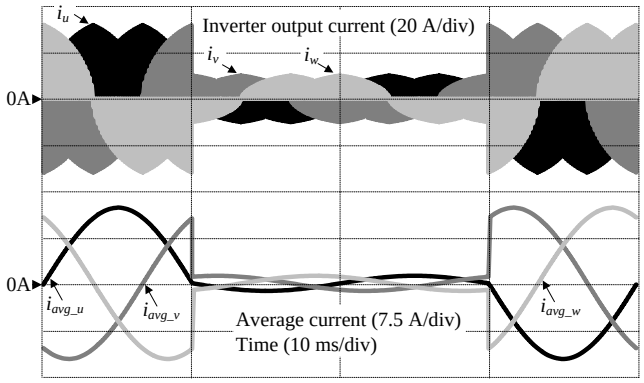



Fig. 8. Load step response between load of 0.1 p.u. and load of 1.0 p.u.. The stable inverter operation is confirmed even at load step change. Moreover, the balanced phase currents are also confirmed.

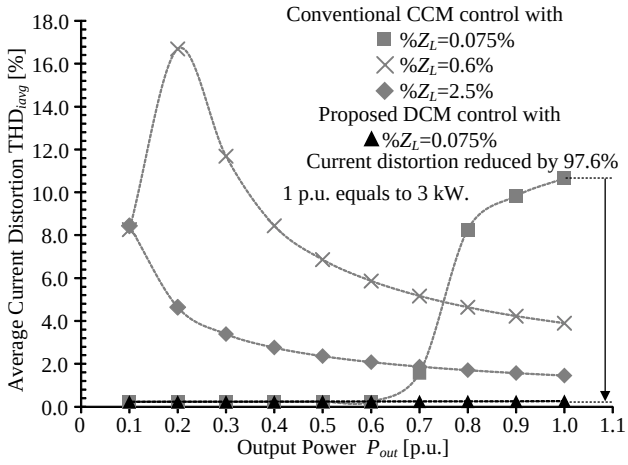



Fig. 9. Current THD characteristics of conventional CCM current control and proposed DCM current control with three different inductor designs. With the proposed DCM current control, the current THD is maintained below 5% over entire load range from 0.1 p.u. to 1.0 p.u..

Figure 8 depicts the load step response of the proposed DCM current control. Even under the sudden load step between the load of 0.1 p.u. and the load of 1.0 p.u., the stable inverter operation and the balanced three-phase currents are still achieved with the proposed control.

Figure 9 shows the current THD characteristics of the conventional CCM current control and the proposed DCM current control with three inductor designs from Fig. 6. At rated load

Table 3. Experimental parameters.

| **Circuit Parameter** | | |
|---|---|---|
| $V_{DC}$ | DC link Voltage | 300 V |
| $v_g$ | Line-to-line Voltage | 100 Vrms |
| $P_n$ | Nominal Power | 700 W |
| $f_g$ | Grid Frequency | 50 Hz |
| $Z_b$ | Total Impedance | 4.8 Ω |
| $f_{sw}$ | Switching Frequency | 20 kHz |
| $T_{deadtime}$ | Dead-time | 500 ns |
| $L$ | Inductor Value | 80 μH (0.5%) |

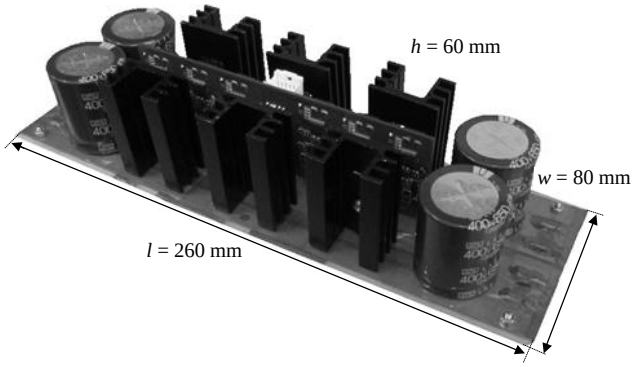


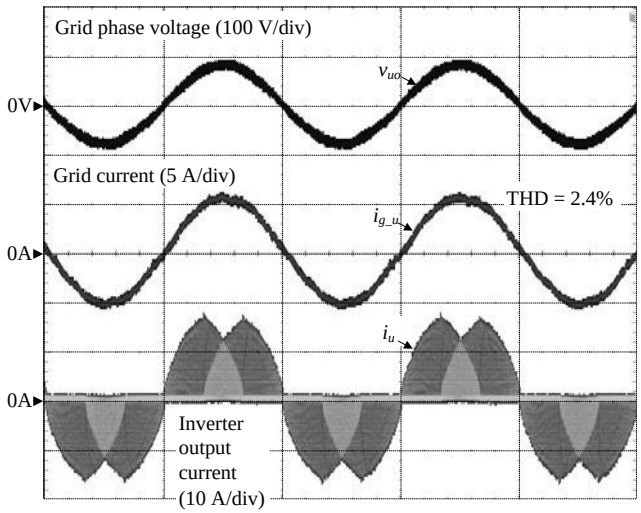

Fig. 10. Prototype of miniature three-phase grid-tied inverter.

with the inductor impedance of 0.075%, the current distortion of the proposed DCM current control is reduced by 97.6% compared to the conventional CCM current control. Note that the current THD of the conventional CCM current control with the inductor impedance of 0.075% or 0.6% has a tendency to decrease at light load. The reason is when the average current is significantly smaller than the current ripple, the current mode is no longer CCM but triangular current mode (TCM) [17]. In TCM, all the turn on of the switching devices is zero voltage switching. On other words, the dead-time-induced error voltage does not occur in TCM. Hence, the current distortion due to the zero-clamping phenomenon disappears at light load.

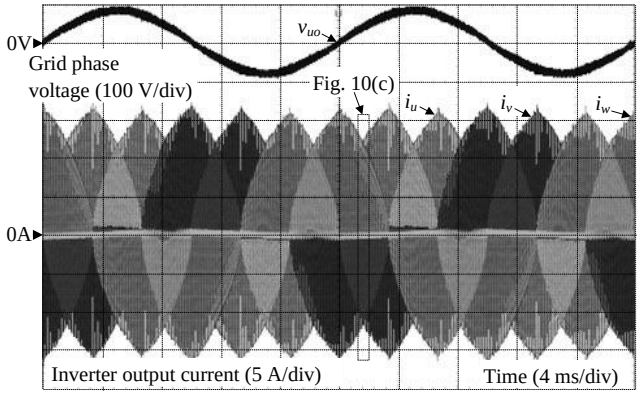
## 4. Laboratory setup

Table 3 shows the experimental parameters, whereas figure 10 depicts the prototype of the miniature three-phase grid-tied inverter. In order to operate the inverter under DCM over entire load range with the switching frequency of 20 kHz, the inverter-side inductor value is designed at 80 μH, whose impedance is 0.5% of the total inverter impedance.

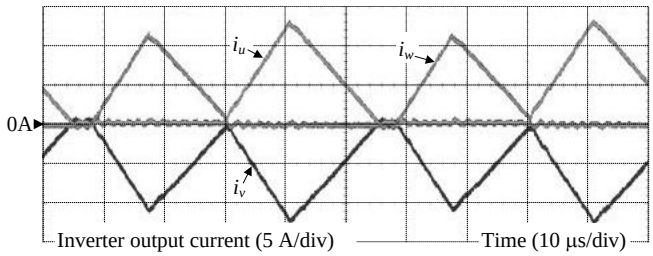
**4.1 Discontinuous-current-mode operation** Figure 11 depicts the three-phase grid-tied inverter DCM operation waveform at rated load. In Figure 11(a), the phase difference between the grid current of u phase and the grid u-phase voltage is almost zero, i.e. the unity-power-factor operation. Furthermore, even with the small inverter-side inductor impedance of 0.5%, the low current THD of 2.4% is still achieved. As shown in Figure 11(b)-(c), the three-phase inverter output currents are similar to those shown in Figure 7(c), i.e. the operation of the proposed DCM control is confirmed.




(a) Grid phase voltage, grid current, and inverter output current of u phase




(b) Grid phase voltage of u phase, and three-phase inverter output currents

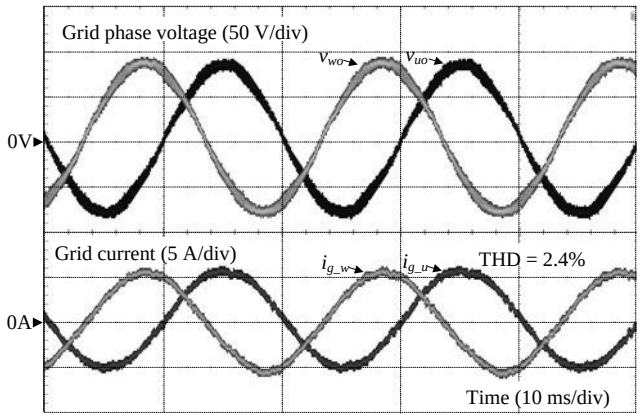



(c) Zoom-in three-phase grid current from Fig. 10(b)

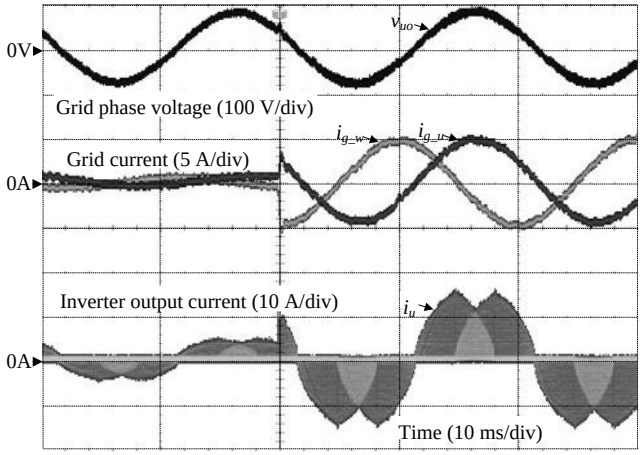
Fig. 11. Three-phase grid-tied inverter DCM operation waveform at rated load. The three-phase inverter output currents shown in Fig. 10(b) are similar to those shown in Fig. 6(c). This confirms the operation of the proposed DCM control.

Figure 12 shows the grid phase voltages and the grid currents of u phase and w phase at the normal operation and at step-up load change. At the normal operation, the three-phase grid current is well balance and the low current THD of 2.4% is achieved for all three-phase grid current. At the step-up load change from 0.1 p.u. to 1.0 p.u., the stable current response is confirmed. Note that the three-phase grid currents are still balance both before and after the step-up load change.

Figure 13 depicts the current THD characteristics of the




(a) Grid phase voltages and grid currents of u phase and w phase at normal operation




(b) Current response of step-up load change

Fig. 12. Grid phase voltages and grid currents of u phase and w phase at normal operation and at step-up load change.

proposed DCM current control. The current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u., which satisfies the current THD constraint in IEEE-1547, even when the inductance impedance is reduced to 0.5% of the inverter impedance. The increase of the current THD at light load can be explained due to the high occupation of the reactive current flowing through the filter capacitor. Therefore, in order to reduce the current THD at light load, the DCM control should also consider the effect of the reactive current in the filter capacitor.

**4.2 Efficiency comparison between asynchronous switching and synchronous switching in DCM** Figure 14 shows the asynchronous switching and synchronous switching in DCM. In the asynchronous switching, the corresponding switches are turned after the period $D_1T_{sw}$ and $D_3T_{sw}$ finish. Therefore, the current has to flow through the diode. In the next generation switching devices such as SiC or GaN, the forward voltage of the inverse diode in such devices is generally higher than that of the conventional MOS-FET devices. Consequently, the conduction loss with the asynchronous switching is higher that of the synchronous switching, where the current flows through the FET part. As shown in Figure 14, the synchronous switching can also be applied into DCM in the same manner as the conventional CCM. Consequently, the conduction loss of the switching device is reduced.

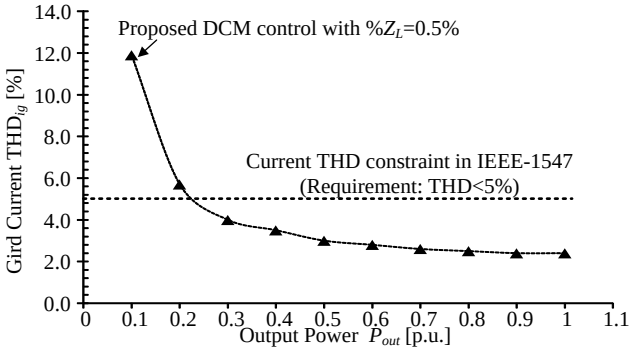



Fig. 13. Current THD characteristics of proposed DCM current control. The current THD is maintained below 5% over load range from 0.3 p.u. to 1.0 p.u., which satisfies the current THD constraint in IEEE-1547, even when the inductance impedance is reduced to 0.5% of the inverter impedance.

Figure 15 depicts the efficiency comparison between asynchronous switching and synchronous switching in DCM. The application of the DCM synchronous switching reduces the conversion loss by 33% compared to the DCM asynchronous switching at rated load. Furthermore, the maximum efficiency of 97.8% is achieved at rated load.

## 5. Conclusion

In this paper, the DCM current control was proposed to the grid-tied three-phase inverter in order to minimize the grid filter volume without worsening the current THD. The DCM control separated the control of each current in individual intervals in order to avoid the control interference of current into each other. Therefore, the interference decoupling control for DCM operation was not required for the proposed control, leading to the simple control system. The effectiveness of the proposed DCM control method was confirmed by both simulations and experiments. In particular, the low current THD of 2.4% was achieved even when the inductance impedance was reduced to 0.5% of the inverter total impedance.

In future works, DCM current feedback controls will be considered in order to eliminate the circuit-parameter dependency.

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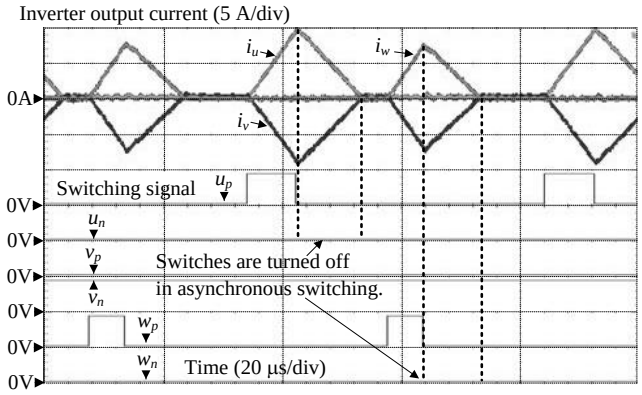
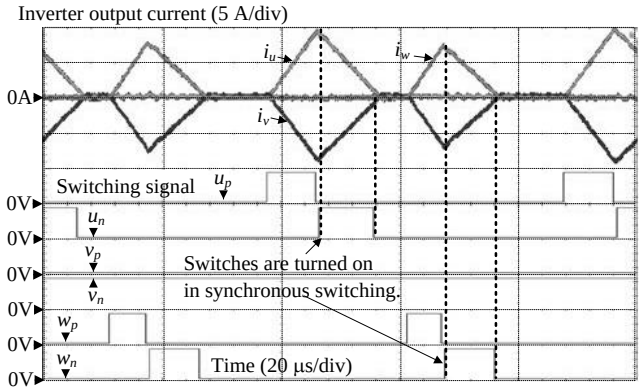



(a) Asynchronous switching in DCM




(b) Synchronous switching in DCM

Fig. 14. Asynchronous switching and synchronous switching in DCM.

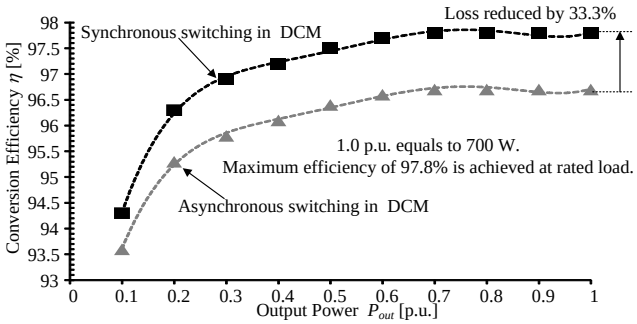



Fig. 15. Efficiency comparison between asynchronous switching and synchronous switching in DCM.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**Hoai Nam Le**

(Student member) received his B.S. and M.S. degrees in electrical, electronics and information engineering from Nagaoka University of Technology, Niigata, Japan in 2014 and 2016, respectively. Presently, he is a Ph.D. candidate at Nagaoka University of Technology, Niigata, Japan. He is the student member of IEEJ and IEEE. His main research interests include multilevel converters. His current research interests include control techniques, design and optimization of power electronic systems employing latest power semiconductor technology (SiC and GaN).

**Jun-ichi Itoh**

(Senior Member) received his M.S. and Ph.D. degrees in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan in 1996 and 2000, respectively. From 1996 to 2004, he was with Fuji Electric corporate Research and Development Ltd., Tokyo, Japan. Since 2004, He has been with Nagaoka University of Technology as an associate professor. He received the IEEJ academic promotion award (IEEJ Technical Development Award) in 2007 and the Isao Takahashi power electronics award in 2010. His research interests include matrix converters, DC/DC converters, power factor correction techniques and motor drives. He is a member of the Institute of Electrical Engineers of Japan and the Society of Automotive Engineers of Japan.