Current Harmonic Reduction based on Space Vector PWM for DC-link Capacitors in Three-Phase VSIs Operating over a Wide Range of Power Factor

Koroku Nishizawa, *Student Member, IEEE*, Jun-ichi Itoh, *Senior Member, IEEE*,
Akihiro Odaka, *Member, IEEE*, Akio Toba, *Member, IEEE*, and Hidetoshi Umida, *Member, IEEE*

***Abstract*-- This paper proposes a novel space vector pulse width modulation (SVPWM) strategy to reduce the switching-frequency-order inverter input current harmonics for a two-level three-phase voltage source inverter operating over a wide range of the load power factor. The fluctuation of the inverter input current around its average value is minimized by optimization of the utilized voltage space vectors to reduce the inverter input current harmonics, which extends the lifetime of the DC-link electrolytic capacitors. Furthermore, the proposed strategy can be adapted to a motor drive system, where a wide variation of the load power factor is desired, by changing the optimized combinations of the voltage space vectors according to the polarities of the output phase currents. Experiments with application of the novel SVPWM confirm that the inverter input current harmonics is reduced by up to 29.5% compared to that with the conventional SVPWM strategy. Moreover, the analytical and experimental results confirm that the proposed SVPWM reduces the inverter input current harmonics in both driving mode and regenerative braking mode, as well as with any load power factor.**

***Index Terms*—DC-link capacitor, Inverter input current harmonics, Space vector pulse width modulation, Three-phase VSI.**

I. Introduction

Three-phase AC motors are widely used in industrial and household applications [1]–[3]. The lifetime extension of the AC motor drive system has been an intense research topic for several decades [4]–[6]. The AC motor is supplied with power from a pulse width modulation (PWM) inverter. Capacitors in the DC-link part of the PWM inverter, which act as an energy buffer stage to stabilize the DC-link voltage and guarantee an acceptable DC-link voltage ripple, are required to have large capacitance. Electrolytic capacitors are generally employed due to their superior capacitance per volume ratio compared to film capacitors or ceramic capacitors. However, the system becomes less reliable due to the short lifetime expectancy of electrolytic capacitors. In particular, the lifetime of a DC-link capacitor is related to its current, which is dependent on the switching-frequency-order inverter input current harmonics [7]. The inverter input current is known to be a superposition summation of the switched current pulses from each phase leg of the three-phase PWM voltage source inverter (VSI), and thus contains many high-order switching harmonics [8], [9]. In particular, internal heating of an electrolytic capacitor, which is caused by this inverter input current harmonics flowing through an equivalent series resistance (ESR) of the capacitors, constitutes a considerable restriction of the long lifetime. Specifically, vaporization of the electrolyte is closely related to the capacitor temperature, and the lifetime of the electrolytic capacitor is approximately reduced by half if the capacitor core temperature increases by 10℃, according to the *Arrhenius equation* [10]. Therefore, the DC-link capacitor is a key component that determines the lifetime of the entire motor drive system, and the DC-link capacitor lifetime is dependent on the inverter input current harmonics. It is noted that using film capacitors as DC-link capacitors could possibly resolve the lifetime problem; however, film capacitors would make the motor drive system bulky due to its low energy density.

In order to extend the lifetime of the DC-link capacitor, modulation methods of the VSI which reduce the inverter input current harmonics have been proposed [11]–[13]. In [11], the near state PWM (NSPWM) has been proposed to reduce the common mode voltage for three-phase VSI. The NSPWM uses a group of three neighbor voltage vectors to match the output and reference volt-seconds. As a result, not only the common mode voltage, but also the inverter input current harmonics can be reduced when the load power factor is higher than 0.8. However, the NSPWM can be applied only at high-modulation indices due to the restrictions on the voltage vector use; therefore, the inverter input current harmonics cannot be reduced at low-modulation indices with the NSPWM. The proposed PWM method in [12] is basically the same as this NSPWM and the effectiveness of this PWM method on the inverter input current harmonics is analytically and experimentally confirmed in detail. The extended double carrier PWM (Ext-DCPWM), which can reduce the inverter input current harmonics for all values of the modulation index,

Manuscript received December 7, 2017; revised February 20, 2018 and May 22 2018; accepted July 9, 2018.

Koroku Nishizawa and Jun-ichi Itoh are with the Nagaoka University of Technology, Niigata 940-2188, Japan (e-mail: koroku_nishizawa@stn.nagaokaut.ac.jp; itoh@vos.nagaokaut.ac.jp).

Akihiro Odaka, Akio Toba and Hidetoshi Umida are with the Fuji Electric Co. Ltd., Tokyo 191-8502, Japan (e-mail: odaka-akihiro@fujielectric.com; toba-akio@fujielectric.com; umida-hidetoshi@fujielectric.com).

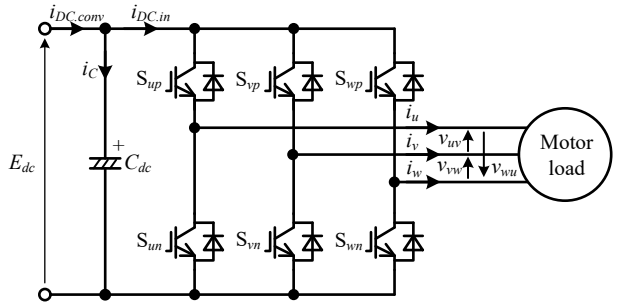


Fig. 1. Three-phase VSI with motor load.

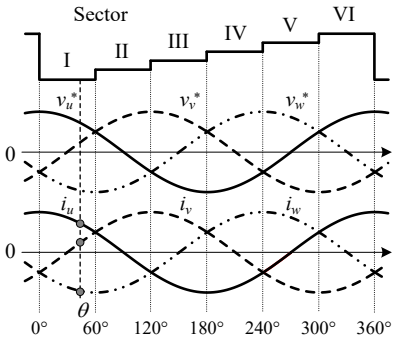


Fig. 2. Waveforms of voltage references and output phase current at unity load power factor ($\varphi = 0°$).

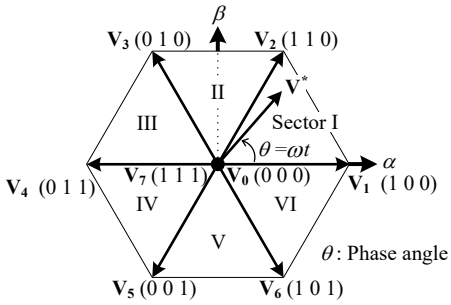


Fig. 3. Output voltage space vectors of VSI in $\alpha\beta$ reference frame.

has been presented in [13]. The Ext-DCPWM uses the same three consecutive voltage vectors as in [11] and [12] at high-modulation indices. In addition, the Ext-DCPWM uses two nonadjacent voltage vectors and one zero vector to reduce the inverter input current harmonics at low-modulation indices. However, in the case of a low load power factor, these modulation methods increase the inverter input current harmonics. Therefore, a modulation method that reduces the inverter input current harmonics over a wide load power factor range is necessary to extend the lifetime of the DC-link capacitor in a motor drive system, of which the variation of the load power factor is considerably wide.

This paper proposes a novel space vector PWM (SVPWM) that reduces the switching-frequency-order inverter input current harmonics under any load power factor condition, i.e. both driving and regenerative breaking modes. As a result of analytical calculations, the employment of voltage vectors in this proposed strategy to reduce the inverter input current harmonics at both high-modulation and low-modulation indices, and provide the same result as the Ext-DCPWM in [13] under a unity load power factor. The analytical calculations also provide a way to indicate the effectiveness of the load power factor on the inverter input current harmonics. The optimized voltage vectors are selected on the basis of the detected output phase current polarities to adapt to variations of the load power factor without detecting it. Therefore, the original contribution of this strategy is the reduction of the inverter input current harmonics over entire region of the load power factor, which is the crucial problem of past works.

This paper is organized as follows; firstly, analytical results on the inverter input current of the three-phase VSI are presented. In particular, the relationship between the inverter input current and the modulation strategy of the VSI is presented. Secondly, the methods for reduction of the inverter input current harmonics by optimization of the voltage space vectors introduced in [13] are explained. The method used to adapt to the variations of the load power factor is then presented. Analytical and experimental results are presented to confirm the effectiveness in terms of the reduction of the inverter input current harmonics, the impact on the output phase current quality, inverter efficiency, and the lifetime of the electrolytic capacitors.

II. Inverter Input Current Harmonics Analysis

A. Conventional Space Vector PWM

Fig. 1 shows a three-phase VSI employed in the motor drive system. The three-phase VSI consists of three half-bridge converters. If the semiconductor switching devices are treated as ideal switches, then the conduction status of any one half-bridge converter can be represented by the following binary switching functions:

$$s_x(t) = \begin{cases} 1, & (\mathrm{S}_{xp}:\mathrm{ON},\ \mathrm{S}_{xn}:\mathrm{OFF}) \\ 0, & (\mathrm{S}_{xp}:\mathrm{OFF},\ \mathrm{S}_{xn}:\mathrm{ON}) \end{cases}, \quad (x = u, v, w). \tag{1}$$

Fig. 2 shows waveforms of the voltage references and the output phase currents at unity load power factor. The output phase currents of the VSI at steady state operating condition can be expressed as:

$$\begin{cases} i_u(t) = I_m \cos(\omega t - \varphi) \\ i_v(t) = I_m \cos\left(\omega t - \dfrac{2\pi}{3} - \varphi\right) \\ i_w(t) = I_m \cos\left(\omega t + \dfrac{2\pi}{3} - \varphi\right) \end{cases}, \tag{2}$$

where I_m is the maximum value of the output phase current, ω is the fundamental angular frequency, and φ is the load power factor angle, i.e. the phase shift between the phase current and phase voltage, respectively.

Fig. 3 shows the output voltage space vectors of the VSI in the $\alpha\beta$ reference frame. These voltage space vectors can be illustrated on the basis of the *Clarke transform*. The switching functions of each phase can become only two different values; therefore, there are $2^3 = 8$ output voltage space vectors of the VSI expressed using the switching functions as $\mathbf{V}$ ($s_u(t)$, $s_v(t)$, $s_w(t)$). Six of these ($\mathbf{V_1}$–$\mathbf{V_6}$) are the active vectors and the others ($\mathbf{V_0}$ and $\mathbf{V_7}$) are the zero vectors. The voltage reference vector can also be derived from the voltage reference values on the basis of the *Clarke transform*, and can be expressed with the modulation index m and the phase angle θ:

$$\mathbf{V}^* = m\angle\theta. \tag{3}$$

In the SVPWM, the voltage reference vector sampled in each control period T_s is generated by synthesizing the three voltage space vectors $\mathbf{V_a}$, $\mathbf{V_b}$, $\mathbf{V_c}$ upon the volt-second balance principle as:

$$\begin{aligned} \mathbf{V}^* &= \frac{t_a}{T_s}\mathbf{V_a} + \frac{t_b}{T_s}\mathbf{V_b} + \frac{t_c}{T_s}\mathbf{V_c}, \\ T_s &= t_a + t_b + t_c \end{aligned} \tag{4}$$

where t_a–t_c are the on-duty of each selected voltage space vector, and a–c represent the number of selected voltage space vectors, as defined in Fig. 3.

Fig. 4 shows the conventional SVPWM strategy. The output phase current harmonics are caused by the difference between the voltage space vector and the voltage reference vector $\mathbf{V}_x$–$\mathbf{V}^*$. Therefore, in the conventional one-carrier PWM strategies [14]–[20], three voltage space vectors which are the closest to the voltage reference vector are used to minimize the output phase current harmonics. In the example shown in Fig. 4, the voltage reference vector is generated using two adjacent active vectors, $\mathbf{V_1}$ and $\mathbf{V_2}$, and the zero vector, $\mathbf{V_0}$ and $\mathbf{V_7}$, at each control period when the voltage reference vector is located in sector I.

B. RMS value of Inverter Input Current

Fig. 5 shows the instantaneous waveform of the inverter input current at sector I when the conventional SVPWM is applied. Note that the phase currents are assumed to be almost constant during a control period. The instantaneous value of the inverter input current is the superposition summation of the switched current pulses from each phase leg and can be calculated as:

$$i_{DC.in}(t) = \sum_{x=u,v,w} \left(s_x(t) \times i_x(t) \right). \tag{5}$$

The DC-side of the three-phase VSI operates at six-fold fundamental frequency, so that the root-mean-square (RMS) value of the inverter input current can be calculated by considering only a sixth of the fundamental period as:

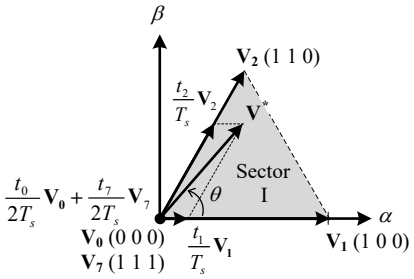


Fig. 4. Conventional SVPWM strategy.

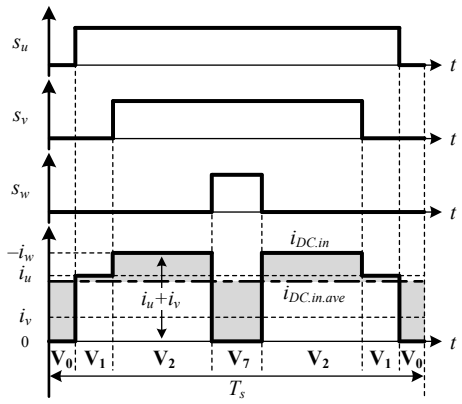


Fig. 5. Instantaneous waveform of inverter input current at sector I with conventional SVPWM.

$$i_{DC.in.RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left(\sum_{k=a,b,c} \frac{t_k}{T_s} i_{DC.in,k}^2(t) \right) d\theta}, \tag{6}$$

where t_k is the on-duty of the selected voltage space vector, and $i_{DC.in,k}(t)$ is the instantaneous value of the inverter input current when the selected voltage space vector is applied. As shown in (6), the RMS value of the inverter input current changes according to the choice of the voltage space vectors.

C. Average value of Inverter Input Current

The inverter input current $i_{DC.in}$ can be split into:

1) a current $i_{DC.conv}$, coming from the converter-side, of which the average value is constant, and
2) a variable current i_C, flowing through the DC-link capacitors.

The average value of $i_{DC.conv}$ is the same as the DC-link average current value because the DC current does not flow through the DC-link capacitors. These average currents can be calculated as follows:

$$\begin{aligned} i_{DC.conv.ave} = i_{DC.in.ave} &= \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left(\sum_{k=a,b,c} \frac{t_k}{T_s} i_{DC.in,k}(t) \right) d\theta \\ &= \frac{3}{4} m \cdot I_m \cos\varphi. \end{aligned} \tag{7}$$

It can be concluded from (7) that the average value of the current coming from the converter-side is not dependent on

the choice of the voltage space vectors, but the modulation index and the load power factor. Thus, the average value of the current coming from the converter-side is always constant, regardless of the choice of the voltage space vectors in the steady state.

D. RMS value of DC-link Capacitor Current

The RMS value of the DC-link capacitor current can be derived by the geometrical difference between the RMS value of the inverter input current (6) and the average value of the current coming from the converter-side (7) as follows:

$$i_{C.RMS} = \sqrt{i_{DC.in.RMS}^2 - i_{DC.conv.ave}^2}. \tag{8}$$

As shown in (8), the RMS value of the DC-link capacitor current, which affects the lifetime of the DC-link capacitors, is also dependent on the choice of the voltage space vectors. Therefore, the lifetime of the DC-link capacitors can be extended by the selection of voltage space vectors that can minimize the RMS value of the inverter input current.

E. Instantaneous RMS value of Inverter Input Current

To minimize the RMS value of the inverter input current, the optimized combination of the voltage space vectors is selected based on the instantaneous RMS value of the inverter input current over one control period, which is derived from (9) [21]:

$$\begin{aligned} i_{DC.in.RMS(T_s)} &= \sqrt{\frac{1}{T_s}\int_0^{T_s}\left(i_{DC.in}^2(t)\right)dt} \\ &= \sqrt{\sum_{k=a,b,c}\frac{t_k}{T_s}\left(i_{DC.in,k}^2(t)\right)}. \end{aligned} \tag{9}$$

Note that a smaller difference between the instantaneous value $i_{DC.in}$, and the average value of the inverter input current $i_{DC.in.ave}$ results in a smaller RMS value of the inverter input current. The RMS value of the inverter input current can thus be reduced by minimizing the fluctuation of $i_{DC.in}$ around the average value, $i_{DC.in.ave}$. The fluctuation of $i_{DC.in}$ is expressed as the shaded areas in the instantaneous waveform of the inverter input current in Fig. 5. In cases where the conventional SVPWM is applied, two zero vectors, $\mathbf{V_0}$ and $\mathbf{V_7}$, are used at each control period. When the zero vector is applied, the instantaneous value of the inverter input current becomes zero, which leads to the large inverter input current fluctuation around the average value.

III. Reduction of Inverter Input Current Harmonics

A. At High Modulation Indices

Fig. 6 shows the optimized combination of the voltage space vectors to minimize the RMS value of the inverter input current at high-modulation indices, and when the phase currents i_u and i_v are positive, and i_w is negative. As shown in Fig. 6(a), three consecutive active vectors ($\mathbf{V_1}$, $\mathbf{V_2}$, and $\mathbf{V_3}$) are used to generate the voltage reference vector, which results in

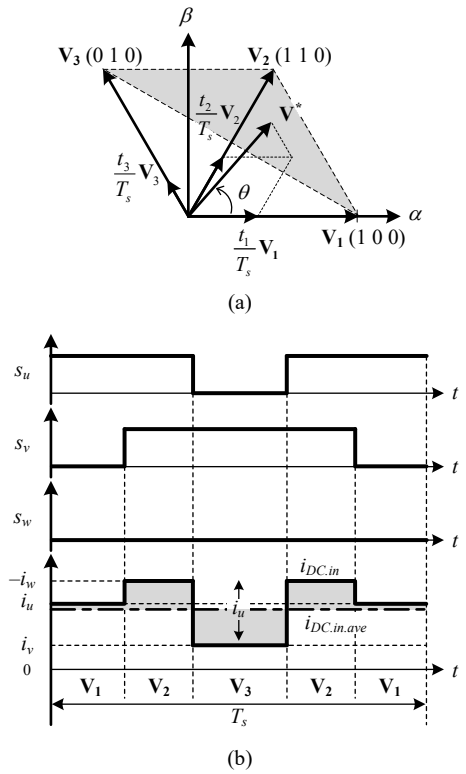
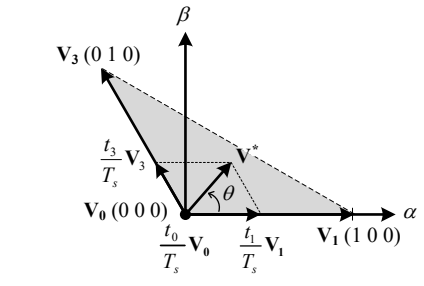
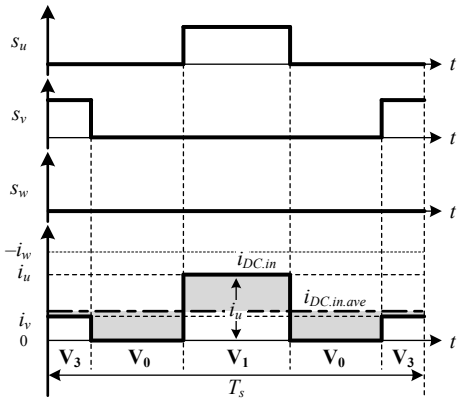


Fig. 6. Optimized combination of voltage space vectors for minimum RMS value of inverter input current when i_u and i_v are positive and i_w is negative at high-modulation indices (a) combination of voltage space vectors and (b) instantaneous waveform of inverter input current.

omission of the zero vector [11]–[13], [22]. Note that, the omission of the zero vector can be achieved only when the tip of the voltage reference vector belongs to the triangle formed by the tips of the three consecutive voltage space vectors shown by the shaded area in Fig. 6(a), i.e. at high-modulation indices. The area that can be output using three consecutive voltage space vectors is the same as that with conventional SVPWM. Thus, the optimized combinations of the voltage space vectors for the minimum RMS value of the inverter input current allows the same output voltage limitations as conventional SVPWM to be obtained. The instantaneous inverter input current does not become zero during a control period, as shown in Fig. 6(b), because the zero vectors are not applied. Furthermore, when the phase current i_u and i_v are positive, and i_w is negative, the fluctuation of the inverter input current around the average value can be minimized with this optimized combination of the voltage space vectors ($\mathbf{V_1}$, $\mathbf{V_2}$, and $\mathbf{V_3}$) at high-modulation indices, which results in the minimum RMS value of the inverter input current. Note that there is only one optimized combination of the voltage space vectors and this optimized combination is dependent on the modulation index, phase angle, and load currents. In order to optimize the combination of the voltage space vectors to obtain the minimum RMS value of the inverter input current, at first, the instantaneous values of the inverter input current of each combination of three voltage space vectors are calculated as (5). Then, the combination, which makes the instantaneous values of the inverter input current become the closest to the average value of the inverter input current, is selected.



(a)

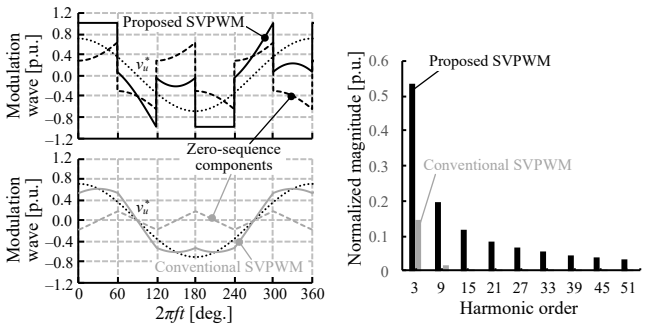


(b)

Fig. 7. Optimized combination of voltage space vectors for minimum RMS value of inverter input current when i_u and i_v are positive and i_w is negative at low-modulation indices (a) combination of voltage space vectors and (b) instantaneous waveform of inverter input current.

B. At Low Modulation Indices

Fig. 7 shows an optimized combination of the voltage space vectors to minimize the RMS value of the inverter input current at low-modulation indices, and the region when the phase currents i_u and i_v are positive and i_w is negative. As shown in Fig. 7(a), one active vector ($\mathbf{V_1}$), one non-adjacent active vector ($\mathbf{V_3}$), and one zero vector ($\mathbf{V_0}$) are used to generate the voltage reference vector [13], [22]. When the tip of the voltage reference vector belongs to the triangle formed by the tips of these three voltage space vectors ($\mathbf{V_1}$, $\mathbf{V_3}$, and $\mathbf{V_0}$), i.e. at low-modulation indices, the use of the zero vector at each control period is unavoidable. However, the effect of the zero current on the fluctuation of the inverter input current around the average value is low at low-modulation indices because the difference between the zero current and the DC-link average current is small. On the other hand, the maximum possible value of the inverter input current, $-i_w$ in Fig. 7(b), causes the largest difference between the instantaneous value of the inverter input current and the average value, and should thus be avoided. Therefore, the voltage space vector $\mathbf{V_2}$ that results in the maximum instantaneous value of the inverter input current when i_u and i_v are positive and i_w is negative, is avoided, and $\mathbf{V_3}$ is alternatively selected for the minimum RMS value of the inverter input current at low-modulation indices.



(a) (b)

Fig. 8. u-phase modulation waveforms and its harmonic contents at cos φ = 0.866, and m = 0.705 (a) modulation waveforms and (b) triplen harmonic spectrum.

The selection of switching states in the proposed SVPWM switches from that shown in Fig. 6 to Fig. 7 by using the modulation index and the phase angle of the voltage references. First, due to that the loading condition is unknown, the loading condition is assumed to be high-modulation indices, i.e. the switching states shown in Fig. 6. Then, the on-duties (t_1, t_2, and t_3) of three consecutive active vectors, which are selected at high-modulation indices, are calculated. Next, following conditional expressions are calculated based on these on-duties:

$$0 \le t_1, t_2, t_3 \le T_s. \tag{10}$$

If these conditional expressions are satisfied, three selected consecutive active vectors are directly used as shown in Fig. 6, i.e. the high-modulation indices. In contrast, if these conditional expressions are not satisfied, it means that the voltage reference vector cannot be generated by synthesizing three selected consecutive active vectors. Therefore, the on-duties of two non-adjacent active vectors and one zero vector, which are selected at low-modulation indices, are calculated and these voltage space vectors are used as shown in Fig. 7.

In terms of the number of switching transitions, it can be observed from Fig. 5 that the number of switching transitions in the conventional SVPWM is 6 per control period. On the other hand, Figs. 6 and 7 confirm that the number of switching transitions in the proposed SVPWM is 4 per control period. Therefore, the application of the proposed SVPWM leads to a higher inverter efficiency than that of the conventional SVPWM because one leg is clamped during each control period.

C. Modulation Waveform of Proposed SVPWM

Fig. 8 shows the u-phase modulation waveforms and its harmonic contents. It is obvious that the modulation waveform of the proposed SVPWM has a larger triplen harmonics than those of the conventional SVPWM, because of the choice of switching states shown in Figs. 6 and 7. These increased triplen harmonics of the modulation waveform generate the larger baseband harmonics, the first carrier sidebands, in the line-to-line voltage of the PWM inverter [23].

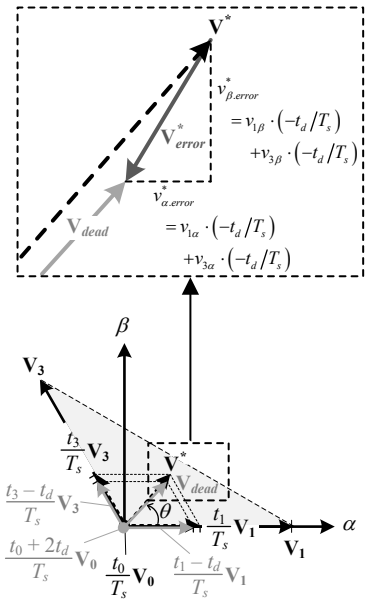


Fig. 9. Dead-time error voltage vector in proposed SVPWM when i_u and i_v are positive and i_w is negative, at low-modulation indices.

D. Dead-time Error Compensation

Fig. 9 shows the dead-time error voltage vector in the proposed SVPWM at low-modulation indices, and the region when the phase currents i_u and i_v are positive and i_w is negative. In fact, the on-duties of each selected voltage space vectors contain duty cycle errors due to the dead-time t_d. With this duty cycle errors, the α-component ($v^*_{\alpha.error}$) and β-component ($v^*_{\beta.error}$) of the dead-time error voltage vector $\mathbf{V}^*_{error}$ can be calculated as shown in Fig. 9 [24]. In the proposed SVPWM, the dead-time error voltage is compensated with feedforward compensation by subtracting $v^*_{\alpha.error}$ and $v^*_{\beta.error}$ from the α-component (v^*_α) and β-component (v^*_β) of the voltage reference vector, respectively. Note that the $v^*_{\alpha.error}$ and $v^*_{\beta.error}$ are dependent only on the dead-time and the sector (A–F) due to the fact that the current polarities are unchanged during each sectors. Only twelve patterns of the calculation for the dead-time error voltage are necessary in advance.

IV. Adaptation to Wide Load Power Factor Range

It should be noted that the reduction effect on the RMS value of the inverter input current through the use of these combinations of the voltage space vectors is dependent on the load power factor because the instantaneous value of the inverter input current is dependent on the output phase currents. Therefore, it is necessary to deal with the variation of the load power factor to reduce the inverter input current harmonics over a wide power factor range, which is a typical requirement of the motor drive system.

Table I lists the sector definitions of the proposed SVPWM. These sectors (A–F) are determined by the combination of the output phase current polarities. With these sectors, the conditions of the output phase currents can be recognized [22].

Fig. 10 shows the layout of the proposed sectors in the $\alpha\beta$ reference frame at a unity load power factor. When i_u and i_v are positive and i_w is negative, i.e. at sector B, the inverter input current harmonics can be minimized with optimized combinations of the voltage space vectors $\mathbf{V_1}$-$\mathbf{V_2}$-$\mathbf{V_3}$ or $\mathbf{V_1}$-$\mathbf{V_3}$-$\mathbf{V_0}$, as shown in Figs. 6 and 7, respectively. Fig. 10 shows that the entire region of sector B is available with these optimized combinations of the voltage space vectors with a unity load power factor. Thus, optimized combinations of the voltage space vectors for reduction of the inverter input current harmonics are applied over the entire phase angle region for the case $|\varphi| < 30°$, i.e. with a high-load power factor.

TABLE I
Sector Definitions of Proposed SVPWM

Sector	Current polarity (P: Positive, N: Negative) i_u	i_v	i_w
A	**P**	**N**	**N**
B	P	P	N
C	N	P	N
D	N	P	N
E	N	N	P
F	P	N	P

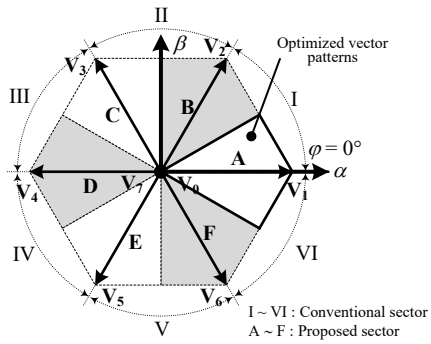


Fig. 10. Layout of proposed sectors in $\alpha\beta$ reference frame at unity load power factor ($\varphi = 0°$).

Fig. 11 shows waveforms of the output phase currents at a load power factor of 0.643 ($\varphi = 50°$), i.e. driving mode. When the load power factor is varied, the proposed sectors shift according to the phase shift of the output phase currents. As a result, the polarity of i_v at the timing of the phase angle θ differs compared with that when the load power factor is unity, as shown in Fig. 2. This leads to an increase of the inverter input current harmonics, even with the same optimized combinations of the voltage space vectors for a unity load power factor.

Fig. 12 shows the layout of the proposed sectors in the $\alpha\beta$ reference frame at a load power factor of 0.643 ($\varphi = 50°$), i.e. driving mode. According to the variation of the load power factor, the proposed sectors are rotated by the phase shift angle, φ. As shown by the mesh area in Fig. 12, a part of sector B is not available with the optimized combinations of the voltage space vectors ($\mathbf{V_1}$-$\mathbf{V_2}$-$\mathbf{V_3}$ or $\mathbf{V_1}$-$\mathbf{V_3}$-$\mathbf{V_0}$) for sector B in the case of $30° < |\varphi| < 90°$, i.e. at a low-load power factor in driving mode. In these areas, new combinations of the voltage space vectors such as three consecutive voltage space vectors or two non-adjacent voltage space vectors with one zero vector, do not reduce the inverter input current harmonics but rather

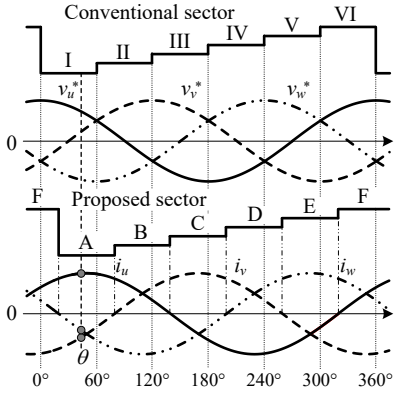


Fig. 11. Waveforms of output phase currents at load power factor of 0.643 (φ = 50°), i.e. driving mode.

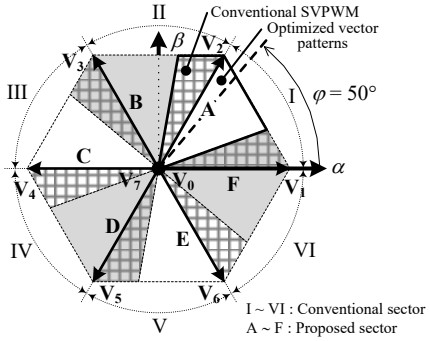


Fig. 12. Layout of proposed sectors in $\alpha\beta$ reference frame at load power factor of 0.643 (φ = 50°).

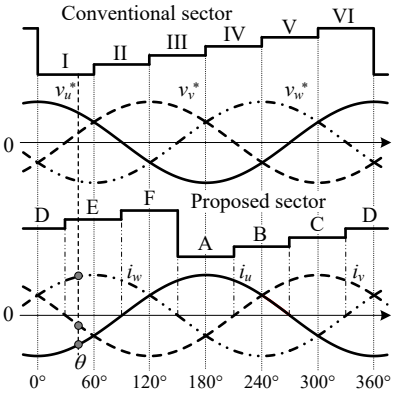


Fig. 13. Waveforms of output phase currents at load power factor of –1.0 (φ = 180°), i.e. regenerative braking mode.

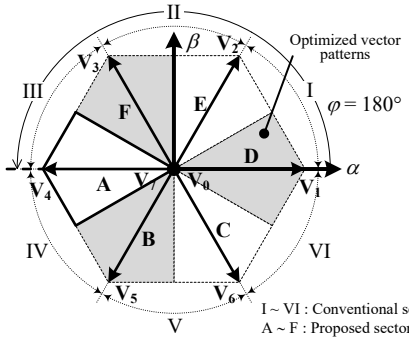


Fig. 14. Layout of proposed sectors in $\alpha\beta$ reference frame at load power factor of –1.0 (φ = 180°).

increase it. Hence, the conventional SVPWM is applied in these areas and the optimized combinations of the voltage space vectors are applied in other areas, which results in a minimum inverter input current harmonics, even when the load power factor is varied.

Fig. 13 shows the waveforms of the output phase currents at a load power factor of –1.0 (φ = 180°), i.e. regenerative braking mode. When the load power factor is –1.0, the polarities of all phase currents at the phase angle of θ reverse; however, the absolute values are the same as those when the load power factor is unity, as shown in Fig. 2. This leads to the same reduction effect on the inverter input current harmonics, even with the same optimized combinations of the voltage space vectors for a unity load power factor. Thus, the inverter input current harmonics can be minimized in regenerative braking mode as well as in driving mode.

Fig. 14 shows the layout of the proposed sectors in the $\alpha\beta$ reference frame at a load power factor of –1.0 (φ = 180°), i.e. regenerative braking mode. Even though the proposed sectors are rotated by 180° according to φ, reduction of the inverter input current harmonics is possible. Note that the area of sector B is no longer available with the optimized combinations of the voltage space vectors (**V_1-V_2-V_3** or **V_1-V_3-V_0**) for sector B. Alternatively, the optimized combinations of the voltage space vectors (**V_1-V_2-V_3** or **V_1-V_3-V_0**) for sector B are effective in terms of reducing the inverter input current harmonics for sector E, which is an opposite side sector of sector B in regenerative breaking mode. Thus, the optimized voltage space vectors in regenerative braking mode are opposite to those in driving mode.

TABLE II
SELECTED VOLTAGE SPACE VECTORS FOR MINIMUM INVERTER INPUT CURRENT HARMONICS

		Sector of proposed SVPWM					
		A	B	C	D	E	F
Sector of conventional SVPWM	I	**V_6-V_1-V_2** or **V_6-V_7-V_2**	**V_1-V_2-V_3** or **V_1-V_0-V_3**	**V_0-V_1-V_2-V_7**	**V_6-V_1-V_2** or **V_6-V_7-V_2**	**V_1-V_2-V_3** or **V_1-V_0-V_3**	**V_0-V_1-V_2-V_7**
	II	**V_0-V_3-V_2-V_7**	**V_1-V_2-V_3** or **V_1-V_0-V_3**	**V_2-V_3-V_4** or **V_2-V_7-V_4**	**V_0-V_3-V_2-V_7**	**V_1-V_2-V_3** or **V_1-V_0-V_3**	**V_2-V_3-V_4** or **V_2-V_7-V_4**
	III	**V_3-V_4-V_5** or **V_3-V_0-V_5**	**V_0-V_3-V_4-V_7**	**V_2-V_3-V_4** or **V_2-V_7-V_4**	**V_3-V_4-V_5** or **V_3-V_0-V_5**	**V_0-V_3-V_4-V_7**	**V_2-V_3-V_4** or **V_2-V_7-V_4**
	IV	**V_3-V_4-V_5** or **V_3-V_0-V_5**	**V_4-V_5-V_6** or **V_4-V_7-V_6**	**V_0-V_5-V_4-V_7**	**V_3-V_4-V_5** or **V_3-V_0-V_5**	**V_4-V_5-V_6** or **V_4-V_7-V_6**	**V_0-V_5-V_4-V_7**
	V	**V_0-V_5-V_6-V_7**	**V_4-V_5-V_6** or **V_4-V_7-V_6**	**V_5-V_6-V_1** or **V_5-V_0-V_1**	**V_0-V_5-V_6-V_7**	**V_4-V_5-V_6** or **V_4-V_7-V_6**	**V_5-V_6-V_1** or **V_5-V_0-V_1**
	VI	**V_6-V_1-V_2** or **V_6-V_7-V_2**	**V_0-V_1-V_6-V_7**	**V_5-V_6-V_1** or **V_5-V_0-V_1**	**V_6-V_1-V_2** or **V_6-V_7-V_2**	**V_0-V_1-V_6-V_7**	**V_5-V_6-V_1** or **V_5-V_0-V_1**

Table II lists the selected voltage space vectors to minimize the inverter input current harmonics for each combination of the conventional sector and proposed sector. The combinations of voltage space vectors in the white-colored cells represent the optimized combinations of the voltage space vectors to minimize the inverter input current harmonics in driving mode. On the other hand, the voltage space vectors

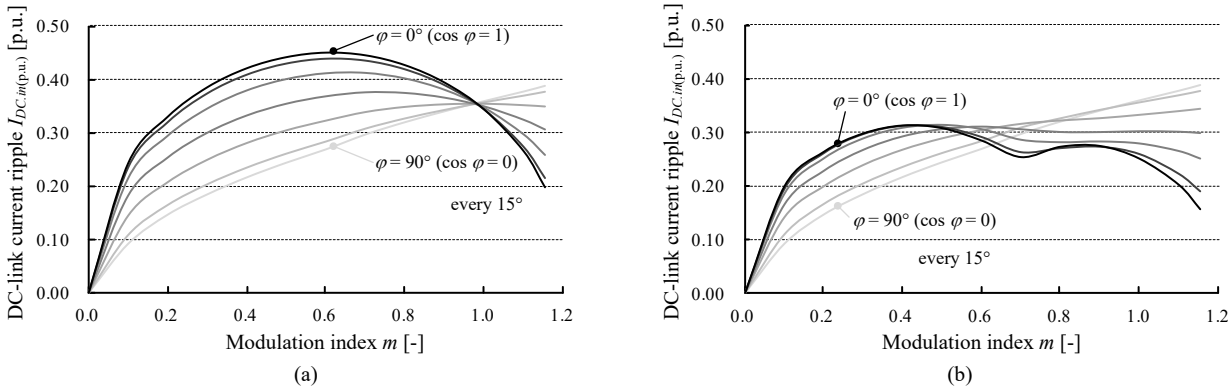


Fig. 15. Analytical results for inverter input current harmonics in driving mode (a) with conventional SVPWM and (b) proposed SVPWM.

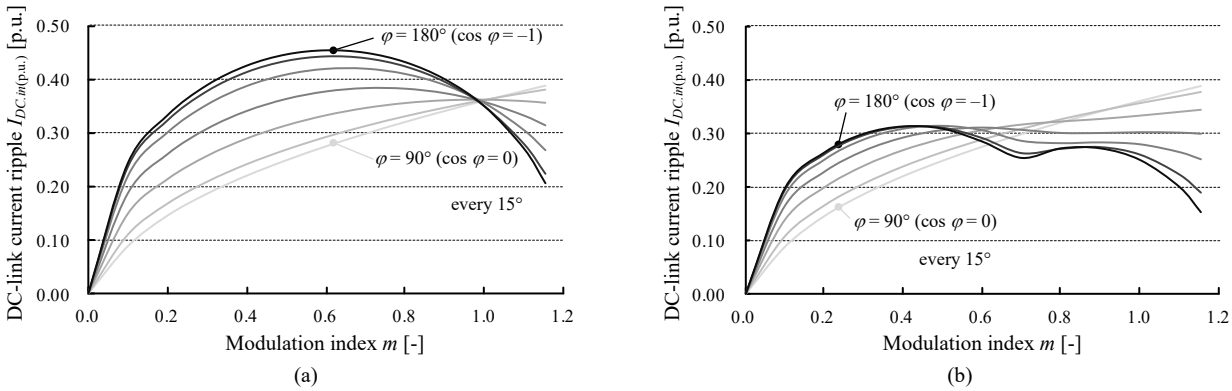


Fig. 16. Analytical results for inverter input current harmonics in regenerative braking mode (a) with conventional SVPWM and (b) proposed SVPWM.

in the light-gray-colored cells represent the optimized combinations in terms of reducing the inverter input current harmonics in regenerative breaking mode. Furthermore, the combinations of the voltage space vectors in conventional SVPWM are listed in the gray-colored cells, i.e. the region where the inverter input current harmonics cannot be reduced with the proposed combinations of the voltage space vectors. Note that in the proposed SVPWM, the load power factor is indirectly detected only by the polarities of the output phase currents and the definition of the proposed sectors. Therefore, the optimized combinations of voltage space vectors to minimize the inverter input current harmonics under any conditions of the load power factor can be simply employed.

V. Analytical Evaluations

The proposed SVPWM was simulated to evaluate the reduction effect on the inverter input current harmonics and compared with conventional SVPWM. In this paper, the inverter input current harmonics is evaluated as the ratio between the RMS value of the inverter input current $i_{DC.in.RMS}$, and the maximum value of the output phase current I_m:

$$I_{DC.in(\text{p.u.})} = \frac{i_{DC.in.RMS}}{I_m} = \frac{1}{I_m}\sqrt{\sum_{k=1}\left(\frac{1}{\sqrt{2}} i_{DC.in.k}\right)^2}, \qquad (11)$$

where k is the harmonic order and $i_{DC.in.k}$ is the k-order component of the inverter input current harmonics. The fundamental component of the inverter input current harmonics is 50 Hz at the rated load. The harmonic components of the inverter input current up to the 20th-order of the switching frequency are considered in this evaluation.

Fig. 15 shows the analytical results of the inverter input current harmonics at load power factor from 0.0 to 1.0, i.e. driving mode. When the conventional SVPWM is applied, the maximum value of $I_{DC.in(\text{p.u.})}$ is 0.450 p.u. at unity load power factor and a modulation index of 0.6. On the other hand, when the optimized combinations of the voltage space vectors for reduction of the inverter input current harmonics are applied, the value of $I_{DC.in(\text{p.u.})}$ at this point can be reduced by 36.7%. Furthermore, it is confirmed that the inverter input current harmonics is reduced under any conditions of the load power factor and modulation index. A higher load power factor enables a greater reduction effect on the inverter input current harmonics to be obtained. This is because the applied ratio of the optimized combinations of voltage space vectors becomes higher as the load power factor becomes higher.

Fig. 16 shows analytical results for the inverter input current harmonics at load power factors from –1.0 to 0.0, i.e. regenerative braking mode. When the load power factor is negative, i.e. regenerative braking mode, the average value of the inverter input current is negative. However, if the modulation index and the absolute values of the load power factor are equal, then the inverter input current harmonics remains unchanged, irrespective of the polarity of the load power factor, due to the same utilization of the voltage space

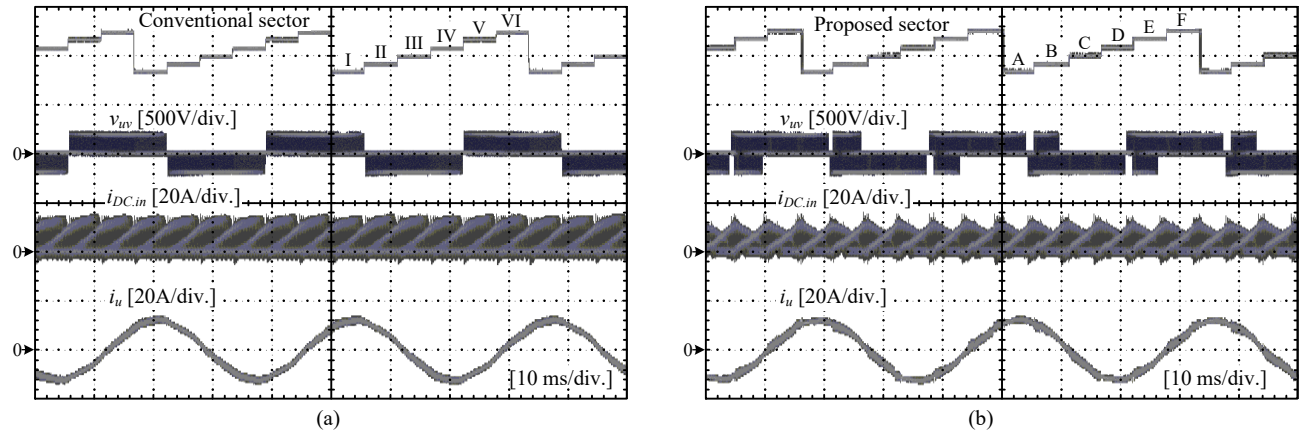


Fig. 17. Experimental waveforms at cos φ = 0.866 (φ = 30°), m = 0.705, i.e. driving mode with high load power factor; sector, output line-to-line voltage, inverter input current and u-phase output current (a) with conventional SVPWM and (b) proposed SVPWM.

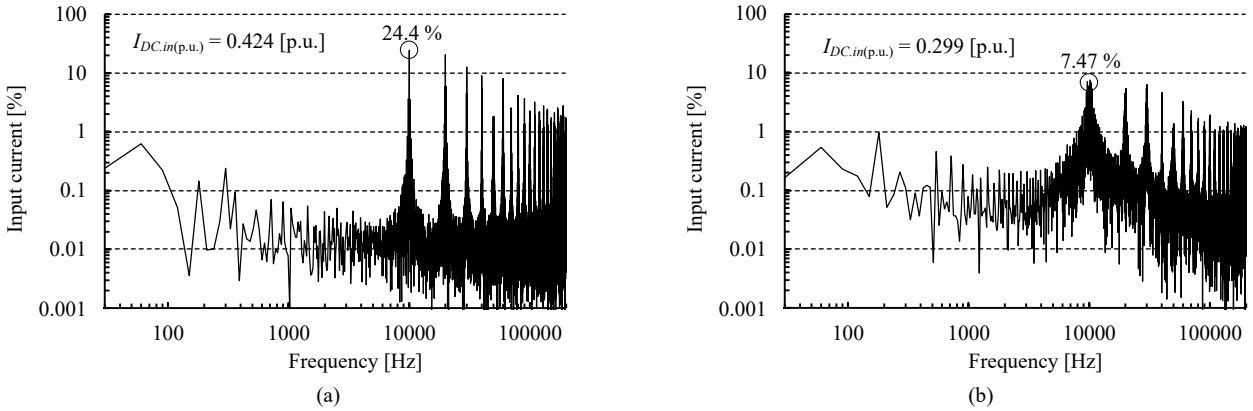


Fig. 18. Harmonic components of inverter input current at cos φ = 0.866 (φ = 30°), m = 0.705, i.e. driving mode with high load power factor (under same conditions as in Fig. 17) (a) with conventional SVPWM and (b) proposed SVPWM.

vectors and same absolute value of the output phase current. Thus, the characteristics of the inverter input current harmonics in regenerative braking mode, as shown in Fig. 16, are similar to those in driving mode shown in Fig. 15. Thus, the inverter input current harmonics is solely dependent on the modulation index m, and the absolute value of the load power factor, |cos φ|.

VI. Experimental Results

The effectiveness of the proposed SVPWM was verified experimentally. In the experiment, a three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.) with a rated power of 3.7 kW was used as the test motor. The test motor was driven by V/f control with the conventional and proposed SVPWM, which were implemented into an evaluation board (TMS320C6713, Texas Instruments). The load power factor was varied by controlling the torque reference of the load motor.

A. Input Current Harmonics

Fig. 17 shows the operating waveforms of the VSI with the conventional and proposed SVPWM at a load power factor of 0.866 (φ = 30°), i.e. driving mode with a high load power factor, and a modulation index of 0.705. When the load power factor is high, the applied ratio of the proposed SVPWM is also high. In particular, the proposed SVPWM is applied at all times with a load power factor of 0.866 (φ = 30°). The results in Fig. 17 confirm that the width of the step change in the inverter input current is reduced by application of the proposed SVPWM. On the other hand, the output phase current with the proposed SVPWM seems to be slightly distorted than that with the conventional SVPWM. Furthermore, the transitions between $+E_{dc}$ to $-E_{dc}$ occur in the line-to-line voltage with the proposed SVPWM. This is because three voltage space vectors, which are not the closest to the voltage reference vector, are used to minimize the inverter input current harmonics in the proposed SVPWM. Note that the averaged line-to-line voltages are sinusoidal waveforms even though such transitions occur. The transition between $+E_{dc}$ to $-E_{dc}$ in the line-to-line voltage leads to the increase of the switching frequency harmonics in the inverter output voltage, which might cause the motor insulation breakdown due to the increase of the motor surge voltage. The effect of the voltage harmonics on the output phase current distortion is considered in a next sub-section.

Fig. 18 shows the harmonic components of the inverter input current under the same conditions as in Fig. 17. The maximum value of the vertical axis (100%) indicates the maximum value of the output phase current. When the conventional SVPWM is applied, the inverter input current

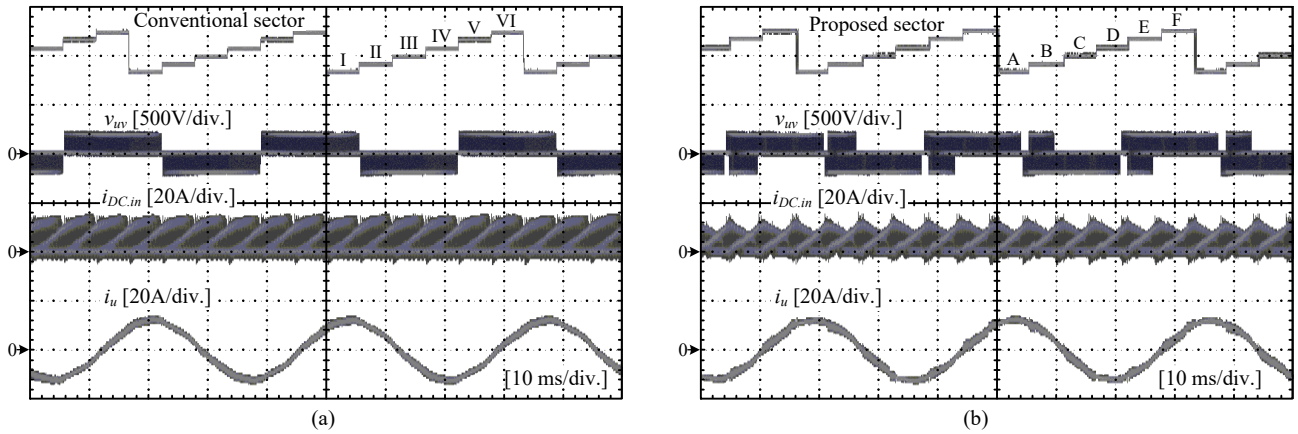


Fig. 19. Experimental waveforms at cos φ = 0.707 (φ = 45°), m = 0.705, i.e. driving mode with low load power factor; sector, output line-to-line voltage, inverter input current and u-phase output current (a) with conventional SVPWM and (b) proposed SVPWM.

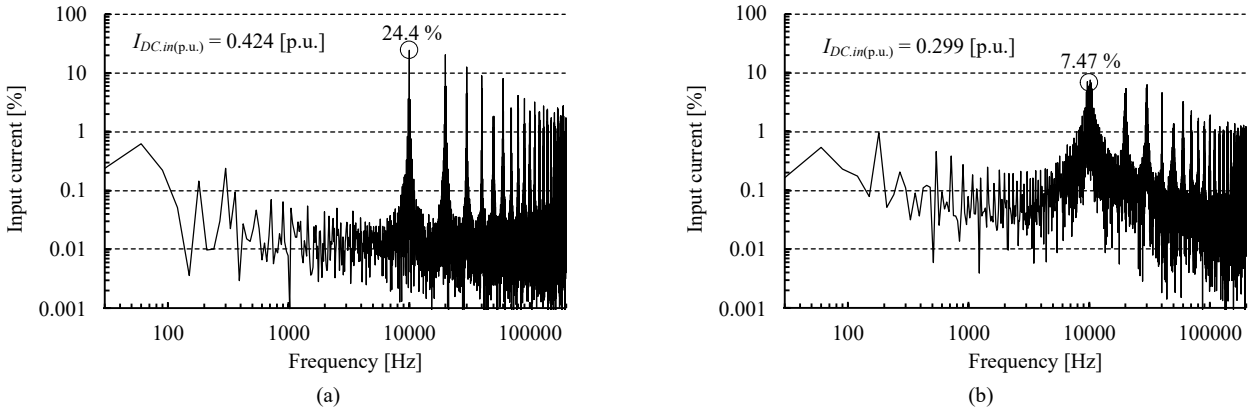


Fig. 20. Harmonic components of inverter input current at cos φ = 0.707 (φ = 45°), m = 0.705, i.e. driving mode with low load power factor (under same conditions as in Fig. 19) (a) with conventional SVPWM and (b) proposed SVPWM.

includes high integer multiples of the switching frequency, the maximum value of which is 24.4%. Application of the proposed SVPWM reduced the switching frequency component by 7.47%. Furthermore, the inverter input current harmonics $I_{DC.in(\text{p.u.})}$, was significantly reduced by 0.299 p.u. when the proposed SVPWM was applied. On the other hand, there are higher low-order harmonics of the inverter input current than those with the conventional SVPWM. This is because the distortions of the output phase current with the proposed SVPWM, which can be observed from Fig. 17, also appear in the inverter input current due to the fact that the inverter input current is the superposition summation of the switched current pulses from each phase leg, expressed as (5). However, even though the application of the proposed SVPWM worsened the low-order harmonics of the inverter input current, the values of those are less than 1% of the rated value. Therefore, the worse low-order harmonics of the inverter input current with the proposed SVPWM are not problem.

Fig. 19 shows the operating waveforms of the VSI with the conventional and proposed SVPWM at a load power factor of 0.707 (φ = 45°), i.e. driving mode with a low load power factor, and a modulation index of 0.705. When the load power is low, both the conventional SVPWM and proposed SVPWM are applied. In particular, the proposed SVPWM is applied within only three-quarters of the entire phase angle region, whereas the conventional SVPWM is applied in the other region at a load power factor of 0.707 (φ = 45°). Fig. 19 confirms that the step change in the inverter input current is partially reduced when the proposed SVPWM is applied.

Fig. 20 shows the harmonic components of the inverter input current under the same conditions as in Fig. 19. When the conventional SVPWM is applied under this low load power factor condition, the twice switching frequency component of the inverter input current harmonics becomes a maximum, the value of which is 22.4%. This value is reduced by 10.6% when the proposed SVPWM is applied. These results demonstrate that the proposed SVPWM is effective in terms of reducing the inverter input current harmonics, even when the load power factor is low.

Fig. 21 shows the measured inverter input current harmonics in driving mode. The inverter input current harmonics can be reduced under any load power factor and modulation index conditions in driving mode. It is also confirmed that as the load power factor becomes higher, the inverter input current harmonics-reduction effect of the proposed SVPWM increases.

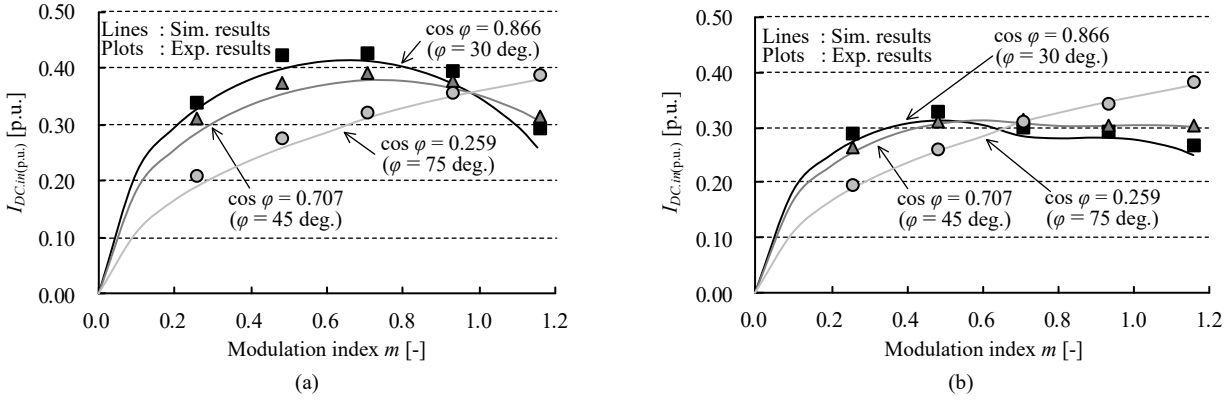


Fig. 21. Measured inverter input current harmonics in driving mode (a) with conventional SVPWM and (b) proposed SVPWM.

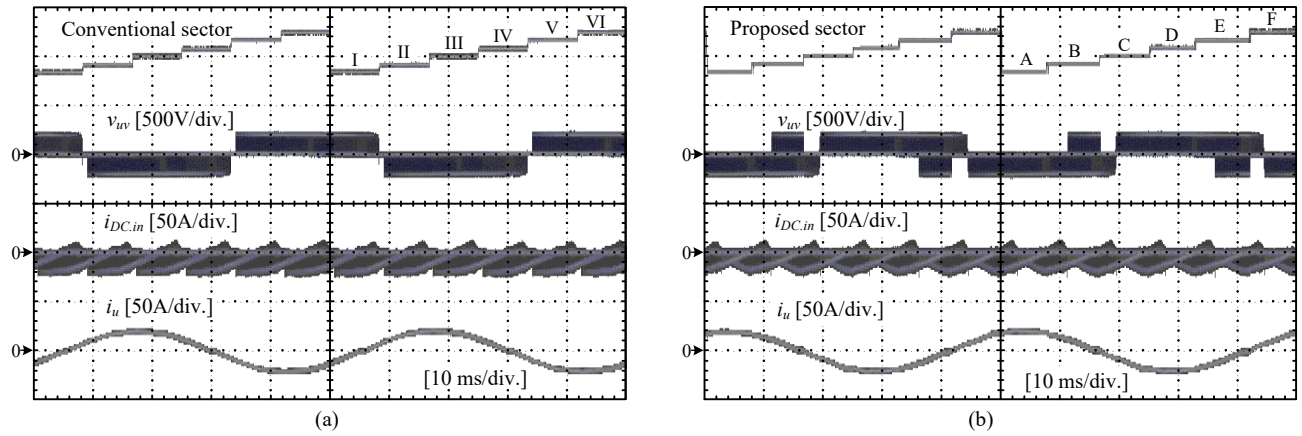


Fig. 22. Experimental waveforms at cos φ = –0.588 (φ = 126°), m = 0.481, i.e. regenerative braking mode; sector, output line-to-line voltage, inverter input current and u-phase output current (a) with conventional SVPWM and (b) proposed SVPWM.

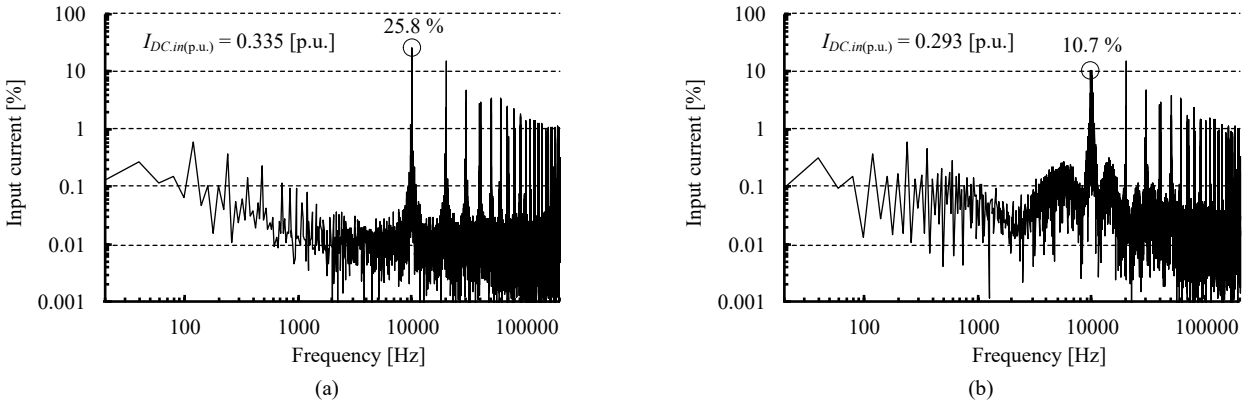


Fig. 23. Harmonic components of inverter input current at cos φ = –0.588 (φ = 126°), m = 0.481, i.e. regenerative braking mode (under same conditions as in Fig. 22) (a) with conventional SVPWM and (b) proposed SVPWM.

Fig. 22 shows the operating waveforms of the VSI with the conventional and proposed SVPWM at a load power factor of –0.588 (φ = 126°), i.e. regenerative braking mode, and a modulation index of 0.481. Even in regenerative braking mode, the proposed SVPWM is also effective in terms of reducing the width of the step change in the inverter input current, which results in a reduction of the inverter input current harmonics.

Fig. 23 shows the harmonic components of the inverter input current under the same conditions as in Fig. 22. When the conventional SVPWM is applied, the maximum value of the switching frequency component of the inverter input current harmonics is 25.8% and the inverter input current harmonics is 0.335 p.u. Fig. 23 confirms that the switching frequency component can be reduced by 10.7% and the inverter input current harmonics can be reduced by 0.293 p.u. by application of the proposed SVPWM, even in regenerative braking mode. The experimental results in Figs. 17–23

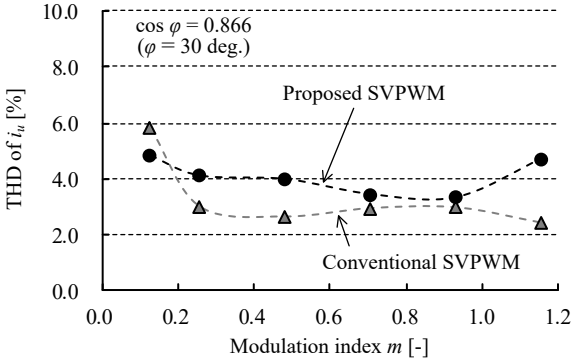


Fig. 24. Measured total harmonic distortion of output phase current i_u at cos φ = 0.866.

confirm that the proposed SVPWM is effective in terms of reducing the inverter input current harmonics for a motor drive system, which has a considerably wide variation of the load power factor.

B. Output Phase Current Harmonics

Fig. 24 shows the total harmonic distortion (THD) of the *u*-phase output phase current at a load power factor of 0.866. Harmonic components of not switching frequency components but up to the 40th-order of the fundamental frequency components are considered in this evaluation. Note that the dead-time error voltage, which is compensated both in the conventional and proposed SVPWM, is estimated from the duty cycle errors due to the dead-time in each sector as shown in Fig. 9. It is shown that the THD of the output phase current obtained with the proposed SVPWM is slightly higher than that obtained with the conventional SVPWM except for the low value of a modulation index. The increase in THD of the output phase current with the proposed SVPWM is caused by the large triplen harmonics of the proposed modulation waveform as shown in Fig. 8 and the current detection error around zero-current-crossing points. In the proposed SVPWM, the detection values of the current polarities are required in order to determine the sectors (A–F) according to Table I. Therefore, the current detection error causes an incorrect selection of the voltage space vectors, and increases the THD of the output phase current, especially around the output phase current zero-crossings. One of the drawbacks of this strategy is the worse output phase current THD which is influenced due to the current polarity detection, which might cause an increase of the iron loss in the load motor.

Fig. 25 shows the simulation results of the harmonic components of the output line-to-line voltage at a load power factor of 0.866 and a modulation index of 0.705. In this simulation, the dead-time is not applied in order to neglect the influence of the dead-time-induced voltage error. The application of the proposed SVPWM worsens the switching frequency harmonic component from 6.85% of the rated voltage (188 V) to 24.3%. Consequently, the increase in the switching frequency component of the line-to-line voltage induces the increase in the same frequency component of the output phase current from 0.360% of the rated current (18 A)

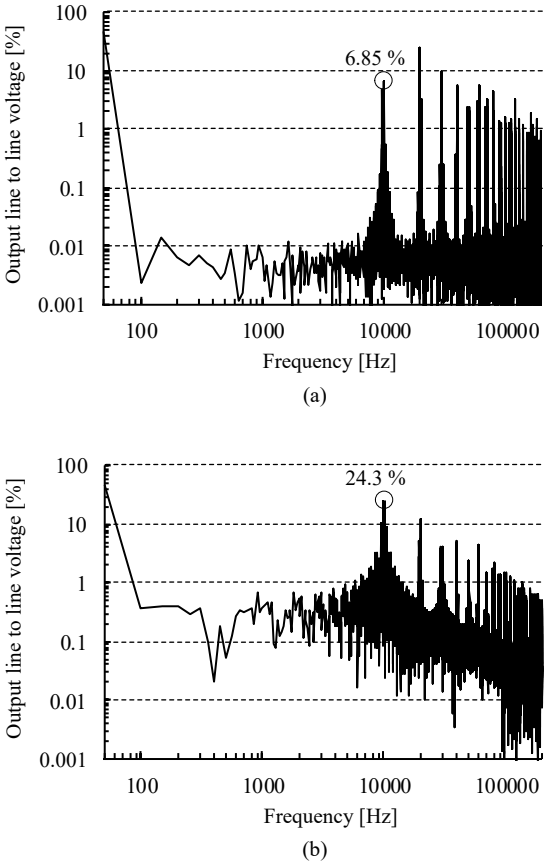


Fig. 25. Simulation results of harmonic components of output line-to-line voltage at cos φ = 0.866, m = 0.705 (a) with conventional SVPWM and (b) proposed SVPWM. 100% of the vertical axis indicates the rated voltage of the test motor (188V). The fundamental frequency is set to 50 Hz, and the switching frequency is set to 10 kHz, respectively.

to 1.28% with the consideration of the switching frequency of 10 kHz, and 1.58 mH leakage inductance per one phase of the test induction motor. Finally, the measured THD of output phase current with the proposed SVPWM at a load power factor of 0.866 and a modulation index of 0.705, the value of which is 3.39% shown in Fig. 24, increases by only 0.234 points (= 3.62% – 3.39%) even though the increase of switching frequency component of the output phase current is considered. It can be concluded that the increase in the switching frequency harmonics in the line-to-line voltage with the proposed SVPWM has a small influence on the distortion in the output phase current.

C. Inverter Efficiency

Fig. 26 shows the inverter efficiency between conventional SVPWM and proposed SVPWM at the load power factor of 0.866. The inverter efficiency was measured using Yokogawa WT1800 power analyzer. The application of the proposed SVPWM leads to a higher inverter efficiency compared to that with the conventional SVPWM due to its less number of switching transitions, which is reduced to two-thirds compared with the conventional SVPWM.

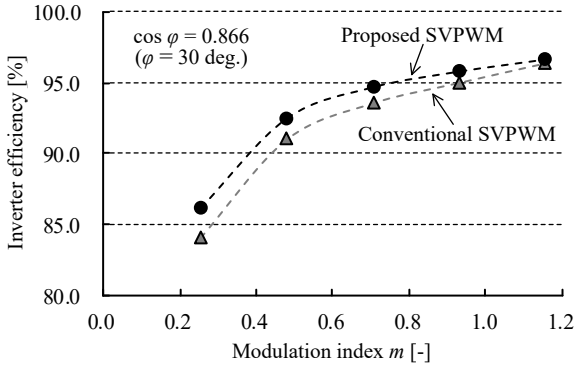


Fig. 26. Inverter efficiency comparison between conventional SVPWM and proposed SVPWM against different modulation index at cos φ = 0.866.

VII. Capacitor Lifetime Comparison

The expected lifetime (L_n) of the electrolytic capacitors is calculated as the multiplication of the lifetime (L_o) at maximum operating temperature of the capacitor at rated ripple current and rated voltage, which is specified on datasheet, by three acceleration rates which are dependent on the ambient temperature (F_T), the ripple current (F_I), and the applied voltage (F_V) [10]. In order to compare the lifetime expectancy of the electrolytic capacitors which is influenced by only the ripple current, the following assumption is conducted:

1) the ambient temperature is constant at the maximum operating temperature of the capacitor (F_T = 1), and
2) the applied voltage (E_{dc}) is constant and below the rated voltage (F_V = 1).

Therefore, the expected lifetime of the electrolytic capacitors can be calculated as follows:

$$L_n = L_o \times F_I, \tag{12}$$

where the L_o is 5000 hours in case of aluminum electrolytic capacitors (NX series, nichicon [25]), which is used as the smoothing capacitor in the prototype.

Table III lists the frequency coefficient of rated ripple current flowing through aluminum electrolytic capacitors [25]. The lifetime of the electrolytic capacitors decreases because of the heat generated inside electrolyte due to power loss when ripple current flows through ESR of the electrolytic capacitors. Meanwhile, ESR of the electrolytic capacitors varies dependently on the current frequency. It is possible to calculate the normalized inverter input current harmonics ($I_{DC.in.freq(\text{p.u.})}$) considering the frequency dependence of the ESR of aluminum electrolytic capacitor by dividing the inverter input current harmonic components by the frequency coefficient (K_f) as follows:

$$I_{DC.in.freq(\text{p.u.})} = \frac{1}{I_m}\sqrt{\sum_{k=1}\left(\frac{1}{\sqrt{2}}\cdot\frac{i_{DC.in.k}}{K_f}\right)^2}. \tag{13}$$

TABLE III
Frequency Coefficient of Rated Ripple Current Flowing Through Aluminum Electrolytic Capacitors

Frequency [Hz]	50	60	120	360	1 k	10 k or more
Coefficient K_f	0.80	0.82	1.00	1.20	1.35	1.40

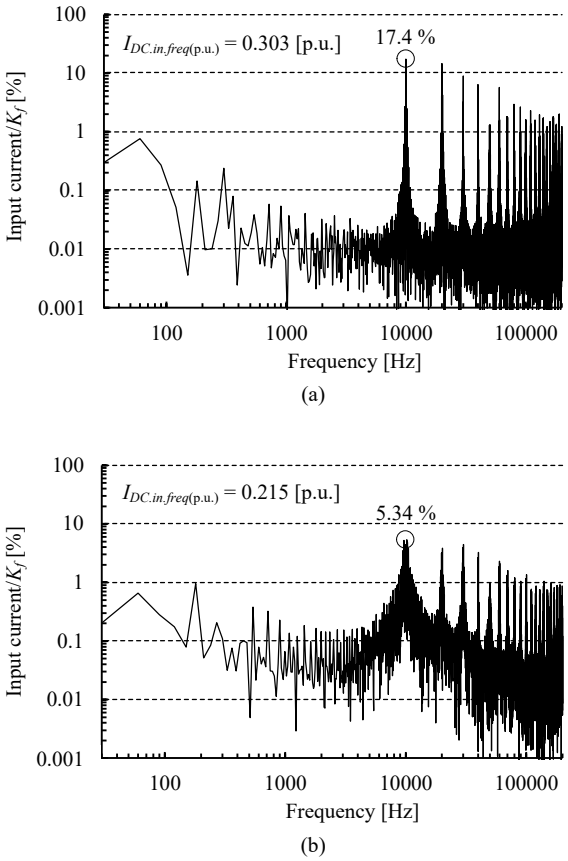


Fig. 27. Harmonic components of inverter input current considering frequency dependence of ESR of aluminum electrolytic capacitor at cos φ = 0.866, m = 0.705 (under same conditions as in Fig. 17) (a) with conventional SVPWM and (b) proposed SVPWM.

Fig. 27 shows the harmonic components of the inverter input current considering the frequency dependence of the ESR of aluminum electrolytic capacitor at a load power factor of 0.866 and a modulation index of 0.705 (under the same conditions as in Fig. 17). The application of the proposed SVPWM reduces the inverter input current harmonics $I_{DC.in.freq(\text{p.u.})}$ by 29.0% when the frequency dependence of the ESR of aluminum electrolytic capacitor is considered. Assuming that the motor is mostly operated at the load power factor of 0.866 and the modulation index of 0.705, and the aluminum electrolytic capacitors in the conventional SVPWM is designed at the worst case of the rated ripple current (i.e., F_I as 1), the lifetime expectancy of the electrolytic capacitor can be given by

$$L_{n\_conv.SVPWM} = L_0 \times 1 = 5\,000 \text{ h}. \tag{14}$$

On the other hand, the application of the proposed SVPWM raises F_I to 1.41 due to a current harmonic reduction of 29.0%. Therefore, the lifetime expectancy of the electrolytic capacitor with the proposed SVPWM can be given by

$$L_{n\_prop.SVPWM} = L_0 \times 1.41 = 7\,050\ \text{h}. \tag{15}$$

Note that the above lifetime calculation is just an example. However, it can be concluded that the application of the proposed SVPWM might extend the lifetime of the electrolytic capacitor about 1.41 times longer at most than that of the conventional SVPWM.

VIII. Conclusion

A novel SVPWM was proposed to reduce the inverter input current harmonics of the three-phase VSI over a wide variation of the load power factor. The inverter input current harmonics was reduced by optimizing combinations of the voltage space vectors to minimize the fluctuation of the inverter input current around the average value. This novel strategy could adapt to a wide range of load power factor by changing the optimized combinations of the voltage space vectors according to the polarities of the output phase currents. It was thus unnecessary to detect the load power factor. The experimental results confirmed that application of the proposed SVPWM reduced the RMS value of the inverter input current by 29.0% at most with the consideration for the frequency dependence of the ESR of aluminum electrolytic capacitor. The 29.0% reduction of the RMS value of the inverter input current might lead to the 1.41 times lifetime extension of the electrolytic capacitors. Moreover, it was confirmed that the inverter input current harmonics was reduced over the entire range of the load power factor, i.e. in both driving mode and regenerative braking mode. Consequently, the proposed SVPWM can be effectively used for the reduction of the constant stress on the smoothing capacitor caused by the inverter input current harmonics, which strongly accelerates the entire lifetime of the motor drive system. On the other hand, this strategy increases the load current THD compared with that obtained using the conventional SVPWM. In addition, the application of the proposed SVPWM worsened the switching frequency harmonics of the inverter output line-to-line voltage.

References

[1] K. Tobari, and Y. Iwaji, "Quick-Response Technique for Simplified Position Sensorless Vector Control in Permanent Magnet Synchronous Motors," *IEEJ Trans. Ind. Appl.*, Vol. 4, No. 5, pp. 582-588, 2015.

[2] T. Nagano, and J. Itoh, "Parallel Connected Multiple Motor Drive System Using Small Auxiliary Inverter for Permanent Magnet Synchronous Motors," *IEEJ Trans. Ind. Appl.*, Vol. 4, No. 1, pp. 40-48, 2014.

[3] K. Sun, Q. Wei, L. Huang, and K. Matsuse, "An Overmodulation Method for PWM-Inverter-Fed IPMSM Drive With Single Current Sensor," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 10, pp. 3395-3404, 2010.

[4] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, "AC/DC/AC PWM Converter With Reduced Energy Storage in the DC-link," *IEEE Trans. Ind. Appl.*, Vol. 31, No. 2, pp. 287-292, 1995.

[5] W.-J. Lee, and S.-K. Sul, "DC-link Voltage Stabilization for Reduced DC-link Capacitor Inverter," *IEEE Trans. Ind. Appl.*, Vol. 50, No. 1, pp. 404-414, 2014.

[6] K. Abe, H. Haga, K. Ohishi, and Y. Yokokura, "Fine Current Harmonics Reduction Method for Electrolytic Capacitor-Less and Inductor-Less Inverter Based on Motor Torque Control and Fast Voltage Feedforward Control for IPMSM," *IEEE Trans. Ind. Electron.*, Vol. 64, No. 2, pp. 1071-1080, 2017.

[7] M. A. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-Cycle Monitoring and Voltage-Managing Unit for DC-link Electrolytic Capacitors in PWM Converters in PWM Converters," *IEEE Trans. Power Electron.*, Vol. 26, No. 2, pp. 493-503, 2011.

[8] M. H. Bierhoff, and F. W. Fuchs, "DC-link Harmonics of Three-Phase Voltage-Source Converters Influenced by the Pulsewidth-Modulation Strategy—An Analysis," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 5, pp. 2085-2092, 2008.

[9] B. P. McGrath, and D. G. Holmes, "A General Analytical Method for Calculating Inverter input current Harmonics," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 5, pp. 1851-1859, 2009.

[10] *Technical Notes on Aluminum Electrolytic Capacitors*, Cat. 8101E-1, nichicon Corp., Tokyo, available via http://www.nichicon-us.com/english/products/pdf/aluminum.pdf

[11] E. Ün, and A. M. Hava, "A Near State PWM Method With Reduced Switching Frequency And Reduced Common Mode Voltage For Three-Phase Voltage Source Inverters," in *Proc. IEEE International Electric Machines & Drives Conf.*, pp. 235-240, 2007.

[12] J. Hobraiche, J.-P. Vilain, P. Macret, and N. Patin, "A New PWM Strategy to Reduce the Inverter Input Current Ripples," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 172-180, 2009.

[13] T. D. Nguyen, N. Patin, and G. Friedrich, "Extended Double Carrier PWM Strategy Dedicated to RMS Current Reduction in DC-link Capacitors of Three-Phase Inverters," *IEEE Trans. Power Electron.*, Vol. 29, No. 1, pp. 396-406, 2014.

[14] H. W. Van Der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and Realization of a Pulsewidth Modulator Based on Voltage Space Vectors," *IEEE Trans. Ind. Appl.*, Vol. 24, No. 1, pp. 142-150, 1988.

[15] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A High-Performance Generalized Discontinuous PWM Algorithm," *IEEE Trans. Ind. Appl.*, Vol. 34, No. 5, pp. 1059-1071, 1998.

[16] A. M. Hava, and E. Ün, "Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters," *IEEE. Trans. Power Electron.*, Vol. 24, No. 1, pp. 241-252, 2009.

[17] D. Casadei, G. Serra, A. Tani, and L. Zarri, "Theoretical and Experimental Analysis for the RMS Current Ripple Minimization in Induction Motor Drives Controlled by SVM Technique," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 5, pp. 1056-1065, 2004.

[18] A. Mehrizi-Sani, and S. Filizadeh, "An Optimized Space Vector Modulation Sequence for Improved Harmonic Performance," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 8, pp. 2894-2903, 2009.

[19] K. Basu, J. S. Siva Prasad, G. Narayanan, H. K. Krishnamurthy, and R. Ayyanar, "Reduction of Torque Ripple in Induction Motor Drives Using an Advanced Hybrid PWM Technique," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 6, pp. 2085-2091, 2010.

[20] J. Holtz, "Pulsewidth Modulation-a Survey," *IEEE Trans. Ind. Appl.*, Vol. 39, No. 5, pp. 410-420, 1992.

[21] T. Takeshita, "Output Voltage Harmonics Suppression of Matrix Converters Using Instantaneous Effective Values," in *Conf. Proc. IEEE Energy Conversion Congress and Exposition*, 270_0839, 2010.

[22] K. Nishizawa, J. Itoh, A. Odaka, A. Toba, and H. Umida, "Reduction of Input Current Harmonics based on Space Vector Modulation for Three-Phase VSI with varied Power Factor," in *Conf. Proc. IEEE Energy Conversion Congress and Exposition*, EC-0318, 2016.

[23] D. G. Holmes, and T. A. Lipo, Pulse Width Modulation for Power Converters. New York: Wiley, 2003.

[24] S. Ahmed, Z. Shen, P. Mattavelli, D. Boroyevich, and K. J. Karimi, "Small-Signal Model of Voltage Source Inverter (VSI) and Voltage Source Converter (VSC) Considering the DeadTime Effect and Space Vector Modulation Types," *IEEE Trans. Power Electron.*, Vol. 32, No. 6, pp. 4145-4156, 2017.

[25] *Datasheet of Aluminum Electrolytic Capacitors (NX series)*, Cat. 8100D, nichicon Corp., Tokyo, available via http://www.nichicon.co.jp/english/products/pdfs/e-nx.pdf.

Koroku Nishizawa (S'16) was born in Nagano, Japan, in 1992. He received the B.S. degrees in electrical, electronics and information engineering in 2015 from Nagaoka University of Technology, Niigata, Japan, where he is currently working toward the Ph.D. degree.

His current research interest includes modulation method of converters.

Mr. Nishizawa is a student member of the Institute of Electrical Engineers of Japan.

Jun-ichi Itoh (M'04–SM'13) was born in Tokyo, Japan, in 1972. He received his M.S. and Ph.D. degree in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan in 1996, 2000, respectively.

From 1996 to 2004, he was with Fuji Electric Corporate Research and Development Ltd., Tokyo, Japan. He was with Nagaoka University of Technology, Niigata, Japan as an associate professor. Since 2017, he has been a professor. His research interests are matrix converters, dc/dc converters, power factor correction techniques, energy storage system and adjustable speed drive systems.

Prof. Itoh received IEEJ Academic Promotion Award (IEEJ Technical Development Award) in 2007. In addition, he also received Isao Takahashi Power Electronics Award in IPEC-Sapporo 2010 from IEEJ, 58th OHM Technology Award from The Foundation for Electrical Science and Engineering, November, 2011, Intelligent Cosmos Award from Intelligent Cosmos Foundation for the Promotion of Science, May, 2012, and Third prize award from Energy Conversion Congress and Exposition-Asia, June, 2013. Prizes for Science and Technology (Development Category) from the Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology, April 2017.

Dr. Itoh is a senior member of the Institute of Electrical Engineers of Japan, the Society of Automotive Engineers of Japan.

Akihiro Odaka (M'00) was born in Saitama, Japan, in 1973. He received the B.S. and M.S. degrees from Tokyo Denki University, Tokyo, Japan, in 1996 and 1998, respectively.

Since 1998, he has been with Fuji Electric Co., Ltd., Tokyo. His interests are static converters and power semiconductor application.

Mr. Odaka is a member of the Institute of Electrical Engineers of Japan.

Akio Toba (M'94) received M.E. degree in 1994 and Ph.D. degree in 2006, both from Tokyo Metropolitan University, Japan.

In 1994, he joined Fuji Electric Co., Ltd., Japan, where he has been conducting research and development of power electronics, motor drives, and electric machines. From 1997 to 1999, he was a visiting researcher of Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) in the University of Wisconsin, Madison, USA.

Dr. Toba is a senior member of the Institute of Electrical Engineers of Japan.

Hidetoshi Umida (M'98) was born in Hiroshima, Japan, in 1956. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1970, 1981, and 1984, respectively.

Since 1984, he has been with Fuji Electric Co., Ltd., Tokyo, Japan. His research interests are in control theory and its application to motor drives and converters.

He is currently a Chief Engineer with Fuji's Corporate R&D Headquarters.

Dr. Umida is a fellow of the Institute of Electrical Engineers of Japan.