Inductance-Independent Nonlinearity Compensation for Single-Phase Grid-Tied Inverter Operating in both Continuous and Discontinuous Current Mode

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Abstract— This paper proposes a control for a single-phase grid-tied inverter operating in both continuous (CCM) and discontinuous current (DCM) to minimize inductors without worsening a current total harmonic distortion (THD). In a conventional CCM/DCM control, an inductance is required in a DCM nonlinearity compensation; consequently, the control becomes inductance-dependent. In the proposed control, a duty ratio at a previous calculation period is utilized to compensate for the DCM nonlinearity and detect current modes independently from the inductance. A 4-kW 100-kHz prototype of the inverter with two designs of the inductor is realized to confirm the effectiveness of the proposed control. When the inductor impedance, which is normalized by an inverter impedance, is reduced from 1.8% to 0.5%, volume and material cost of the inductor are reduced by 51% and 62%, respectively, whereas the loss at a light load of 0.1 p.u. is reduced by 35%. However, due to this inductor minimization, the current THD at a rated load increases from 2.3% to 8.7% with the conventional control, which violates the grid current harmonic constraint regulated by standard IEEE-1547. The proposed CCM/DCM control reduces the current THD from 8.7% to 2.1%, which enables the inductor minimization and satisfies the grid standard.

Index Terms— Current control, Single-phase grid-tied inverters, Continuous current mode, Discontinuous current mode, Nonlinear control systems.

This paper is the updated version of the paper entitled “Mixed conduction mode control for inductor minimization in grid-tied inverter” presented at PEDS2017 (December 12-15, 2017, Hawaii, USA). In the manuscript, all the old experimental results are replaced with the new experimental results and the comparisons with the conventional methods are also demonstrated.

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I. INTRODUCTION

Over last decades, the application of photovoltaic systems (PV) to residential areas has accelerated due to a continuously decrease in solar panel price. In the residential PV systems, single-phase grid-tied inverters are required in order to transmit solar DC power into AC single-phase grid. High efficiency and compact size with low cost are requirements for these inverters in order to further assist the penetration of the PV systems into the residential areas. In such grid-tied inverters, *LCL* filters are generally employed between the output of the inverter and the AC single-phase grid in order to suppress current harmonics and meet grid current harmonic constraints as defined by standards such as IEEE-1547 [1]. Inductors in the *LCL* filters account for major volume and cost of the inverter, which can be decreased by a low-inductance *LCL* filter design [2]-[6]. However, the reduction of the inductance implies a design of a high current ripple due to a high dc-link-voltage-to-inductance ratio. This high current ripple results in a current distortion phenomenon entitled zero-current clamping, in which the current distortion increases notably as the current ripple increases [7]-[12].

When the zero-current clamping occurs, the inverter operation changes from continuous current mode (CCM) to discontinuous current mode (DCM), which is well-known for its strong nonlinear behavior. In particular, the DCM operation exhibits a nonlinear duty-ratio-to-current transfer function, which significantly changes the converter dynamic; consequently, the current distortion increases when the same CCM controller is used to control the DCM current [13]-[15]. In past few years, many researches focusing on compensation methods for the DCM nonlinearity have been reported to solve this problem [14], [16]-[22]. However, a critical penalty of those methods is that the nonlinearity compensation for DCM is dependent on the inductance. In the residential PV systems, the inductors with high tolerance are generally employed in the inverter; furthermore, the grid-tied inverter is required to deal with severe changes of the ambience, i.e. the inductance varies frequently. When actual inductances are different from nominal values, the stability of such inductance-dependent control methods can no longer be guaranteed.

This paper proposes a current control method for the single-phase grid-tied inverter operating in both CCM and DCM, which is independent from the inductance, in order to achieve the inductance reduction without worsening the current total harmonic distortion (THD). The original idea in this paper is that the DCM nonlinearity compensation is constructed by utilizing a duty ratio at a previous calculation period instead of using the inductance. Furthermore, the current mode is also determined without using the inductance by the comparison of the output duty ratios. Consequently, the proposed CCM/DCM current control can be applied widely in the residential PV systems in order to minimize the *LCL* filters and further reduce the cost of the overall system. This paper is organized as follows; in Section II, the zero-current clamping phenomenon is explained together with the problems of the conventional DCM nonlinearity compensation methods, then in section III, the CCM/DCM current control based on the inductance-independent DCM nonlinearity compensation is proposed as the main part of this paper. Finally, the effectiveness of the proposed CCM/DCM current control is confirmed in section IV.

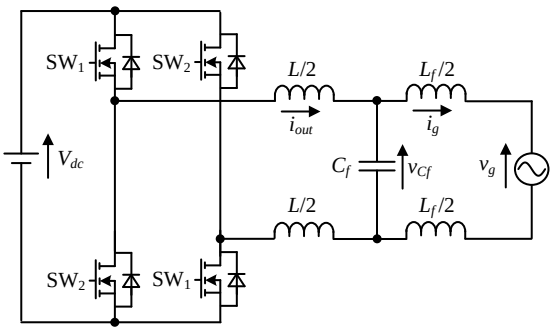


Fig. 1. Single-phase grid-tied inverter. An H-bridge inverter with a *LCL* filter is analyzed due to its simple configuration, which provides high fault-tolerant reliability. The inverter is operated under bipolar modulation and the impedance of each grid line is designed equally in order to minimize a common-mode current.

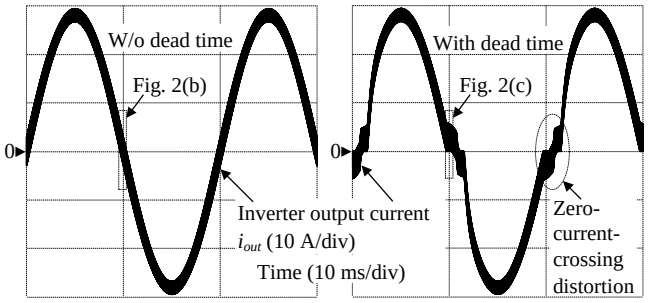
As development steps of the proposed current control, first, the DCM current control method for unipolar inverters has been proposed in [23]; next, this DCM current control method has been modified for bipolar inverters in [24]; finally, the current control method for bipolar inverters operating in both CCM and DCM under different power factor has been proposed in [25]. This paper is an updated version of [25] with additional improvements and substantial contributions such as: detailed analysis guidelines for the DCM nonlinearity compensation which can be applied for numerous topologies are provided in section III; furthermore, new experimental results of inverter dynamic under CCM and DCM operation, analysis on efficiency improvement with loss breakdown, investigation on inductor cost reduction, and comparisons with the conventional current control method on computation time are demonstrated in section IV.

II. Zero-Current Clamping Phenomenon and Problems of Conventional Discontinuous-Current-Mode Nonlinearity Compensation Methods

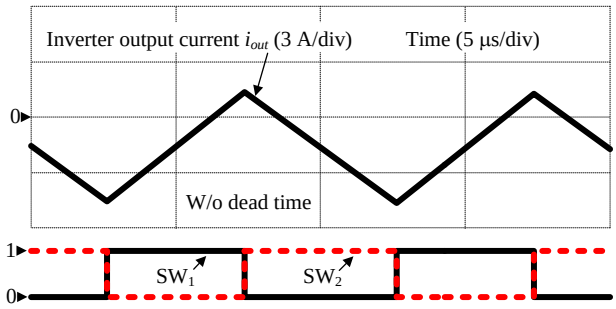
This section presents the cause of the zero-current-crossing distortion in the vicinities of the zero-current crossing and the drawbacks of the conventional DCM nonlinearity compensation methods.

Fig. 1 depicts the circuit configuration of the single-phase grid-tied inverter. Although many DC/AC converter topologies such as, e.g. modular multilevel converters or flying capacitor multilevel converters [26]-[27], have been proposed for the grid-tied inverter, a typical H-bridge inverter is analyzed due to its simple configuration, which provides high fault-tolerant reliability [28]. The *LCL* filter is used as an interface between the inverter and the grid in order to suppress the current harmonics of the inverter output current i_{out}. Compared to *L* filters or *LC* filters, the *LCL* filter can obtain effective switching harmonics attenuation with lower inductance requirements [29]. Meanwhile, in recent years, the application of wide bandgap semiconductor devices such as SiC or GaN enables the inverter to push the switching frequency up to several hundreds of kHz, which further reduces the inductance of the *LCL* filter. However, the low-inductance *LCL* filter design significantly increases the zero-current-crossing distortion, ipso facto, that cannot satisfy the grid current harmonic constraints [7]-[12].

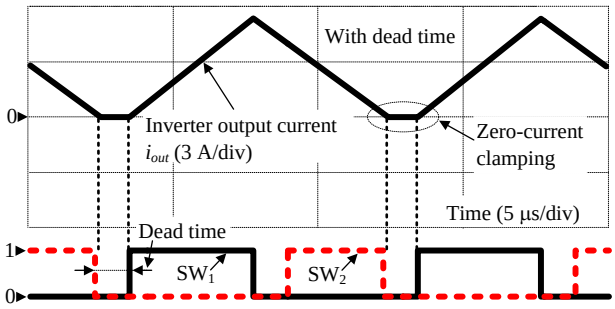
Fig. 2 describes the zero-current clamping phenomenon. When a dead-time is not in use, the inverter output current flows continuously over entire a switching period; hence, a sinusoidal current waveform is obtained. However, the zero-current clamping



(a) Inverter output current w/o dead time and with dead time



(b) Zoom-in current and switching signals w/o dead time



(c) Zoom-in current and switching signals with dead time

Fig. 2. Zero-current clamping phenomenon and zero-current-crossing distortion. The dead-time causes the zero-current clamping phenomenon in the vicinities of the zero-current crossing, which changes the inverter operation from CCM to DCM. The low current loop gain in DCM worsens the current response and causes the zero-current-crossing distortion. Note that the long dead-time is employed for better illustration.

phenomenon occurs during the dead-time interval when the dead-time is applied in order to avoid an instantaneous turn-on of both two switching devices in one leg. Due to this phenomenon, the inverter operation changes from CCM to DCM, which exhibits a nonlinear duty-ratio-to-current transfer function. In particular, the open loop gain in DCM is much lower than that in CCM as shown in Fig. 8 of [14]; consequently, the current distorts in the vicinities of the zero-current crossing due to the low current response in DCM when the same CCM controller is operated under DCM. The length of the zero-current clamping interval depends on the current ripple of the inverter output current i_{out}, the dead-time-to-switching-period ratio, and the power level. Therefore, the zero-current-crossing distortion is severe when the low-inductance design of the *LCL* filter is employed, i.e. the design of the high current ripple. The increase in the inverter-side inductance L and the decrease in the dead time shorten the zero-current clamping interval and might reduce the zero-current-crossing distortion; however, the filter volume becomes large and the dead time is limited by the switching speed of the switching devices.

One of the approaches to deal with the zero-current-crossing distortion is to eliminate the zero-current clamping phenomenon. In [30], the turn-on and turn-off moment of the switching devices are adjusted when the current is in the vicinities of the zero-current crossing in order to maintain the continuous flow of the current over entire a switching period. Hence, the current control performance remains unchanged and the zero-current-crossing distortion does not occur. However, the turn-on and turn-off

moments are varied according to the current ripple, which is a function of the inverter-side inductance *L*, i.e. an inductance-dependent method.

As other solutions, many current control methods for converters operating both in CCM and DCM have been proposed [14], [16]-[22]. A CCM/DCM control for practical applications has to deal with two main challenges; the DCM nonlinearity compensation and the mode detection between CCM and DCM. In the adaptive dead-time compensation method and the turn-off transition compensation method [16]-[17], the dead-time-induced error-voltage compensation is modified and fed forward into the output of the controller in order to compensate for the DCM nonlinearity when the zero-current clamping phenomenon occurs. Nevertheless, both methods exhibit the requirements which restrict the employment over a wide range of application. In particular, adjustment parameters for the adaptive dead-time compensation must be properly tuned for each individual system [16]. Meanwhile, accurate device parameters, e.g. parasitic capacitances, are required for the turn-off transition compensation method [17]. Meanwhile, the conventional CCM grid-voltage feed forward is modified as shown in Fig. 10 of [14] or [22] to compensate the DCM nonlinearity, whereas the mode is simply detected by comparing the output of the feed forward. One of the disadvantages of this method is that, the feed forward for DCM is a function of the inductance, which still makes the control stability sensitive to the circuit parameter.

In [18], the DCM nonlinearity compensation is avoided by the design of a wide bandwidth current controller, whereas the mode detection is achieved by the zero-current detection. The wide bandwidth current controller can deal with the low open loop gain in DCM; however, this design requires a high speed microcontroller per se and is undesirable in term of cost reduction. In addition, the zero-current detection faces the challenge where the current does not remain at zero during the zero-current clamping interval. Instead, the actual current oscillates in the net comprised of the inverter-side inductor and parasitic capacitors of the switching devices [19]. Therefore, the zero-current detection must be tuned whenever any circuit components are changed. In [20]-[21], the DCM nonlinearity compensation is also avoided by the design of a DCM current feed forward control. The principle of the DCM current feedforward control is to design the controller based on the reduced-order model or the full-order model [14]. An advantage of the feedforward control is the unrequired current sensor. However, a mismatch between the nominal values and the actual values of the circuit parameters still results in an instability of the control system. As the motivation for the achievement of the inductance reduction without worsening the current THD, it is necessary to realize the DCM nonlinearity compensation and the mode detection with a feature as inductance-independence.

III. Inductance-Independent Current Control for Continuous Current Mode and Discontinuous Current Mode

This section proposes the inductance-independent current control for the single-phase grid-tied inverter operating in both CCM and DCM as the main part of this paper. First, the derivation of the DCM nonlinearity compensation, in which the use of the inductance is eliminated by the duty ratio at previous calculation period, is explained in section III.A. Next, the mechanism of the

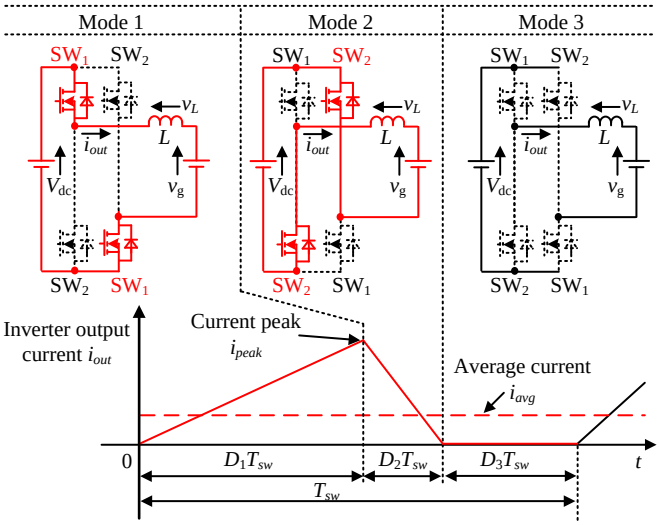


Fig. 3. Current path and inverter output current waveform in DCM when the grid voltage is positive. The zero current interval D_3T_{sw} occurring in DCM introduces the nonlinearities into the transfer function [13]-[15].

mode detection between CCM and DCM without using the inductance is explained in section III.B.

A. Discontinuous-Current-Mode Nonlinearity Compensation by Duty Ratio at Previous Calculation Period

Fig. 3 depicts the current path and the inverter output current waveform in DCM when the grid voltage is positive. The filter inductor L_f and the filter capacitor C_f are omitted due to the simplification. In order to derive the nonlinearity compensation for DCM, the circuit model in DCM is required. First, let D_1, D_2 and D_3 denote the duty ratios of the first, the second and the zero-current interval. Average small signal modeling technique is used to model the inverter for the current control loop design [13]. The inductor voltage in mode 1, mode 2 and mode 3 is given by (1)-(3), respectively,

$$v_{L1} = V_{dc} - v_g \quad \text{.....(1)}$$

$$v_{L2} = -\left(V_{dc} + v_g\right) \quad \text{.....(2)}$$

$$v_{L3} = 0 \quad \text{.....(3)}$$

where V_{dc} is the dc-link voltage and v_g is the grid voltage. Then, the inductor voltage during a switching period is expressed by (4),

$$v_L = D_1 v_{L1} + D_2 v_{L2} + D_3 v_{L3} = D_1\left(V_{dc} - v_g\right) - D_2\left(V_{dc} + v_g\right) \quad \text{.....(4)}$$

The average current and the current peak of the inverter output current are given by (5)-(6), respectively,

$$i_{avg} = \frac{i_{peak}}{2}\left(D_1 + D_2\right) \quad \text{.....(5)}$$

$$i_{peak} = \frac{V_{dc} - v_g}{L} D_1 T_{sw} \quad \text{.....(6)}$$

where T_{sw} is the switching period. Substituting (6) into (5) and solving the equation for the duty ratio D_2, then the duty ratio D_2 is expressed by (7),

$$D_2 = \frac{2Li_{avg}}{D_1 T_{sw}(V_{dc} - v_g)} - D_1 \quad \text{.....(7)}$$

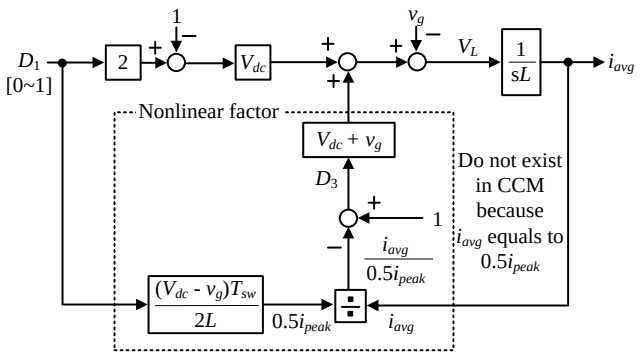


Fig. 4. Circuit model of inverter operating in DCM. The current control loop gain in DCM depends on the average current, i.e. the nonlinearities occurring in the duty-ratio-to-current transfer function and the grid-voltage-to-current transfer function.

Substituting (7) into (4) in order to remove the duty ratio D_2, and representing (4) as a function of the duty ratio D_1, (8) is obtained,

$$L\frac{di_{avg}}{dt} = v_L = V_{dc}\left(2D_1 - 1\right) - v_g + \left(V_{dc} + v_g\right)\left[1 - \frac{2Li_{avg}}{\left(V_{dc} - v_g\right)D_1T_{sw}}\right] \quad \text{.....(8)}$$

Then, the circuit model in DCM is established based on (8) [13].

Fig. 4 illustrates the circuit model of the inverter operating in DCM. The dash line part does not exist when the inverter operates in CCM because the average current i_{avg} equals to the half current peak $i_{peak}/2$; in other words, the CCM operation makes the zero-current interval D_3T_{sw} shown in Fig. 3 disappear. However, the zero-current interval D_3T_{sw} induces the nonlinearity into the transfer functions when the inverter operates in DCM, which worsens the current response in DCM when the same controller is applied for both CCM and DCM [13]-[15]. Therefore, the output of the controller is necessary to be compensated when the inverter operates in DCM. The derivation of the compensation for the DCM nonlinearity is explained as follows. First, the circuit model in Fig. 4 is linearized at steady-state points. In particular, the dc-link voltage, the grid voltage, the average current and the duty ratio when the inverter operates in the steady-state points can be expressed by (9)-(12), respectively,

$$V_{dc} = V_{dc\_s} + \Delta v_{dc} \quad \text{.....(9)}$$
$$v_g = v_{g\_s} + \Delta v_g \quad \text{.....(10)}$$
$$i_{avg} = i_{avg\_s} + \Delta i_{avg} \quad \text{.....(11)}$$
$$D_1 = D_{1\_s} + \Delta D_1 \quad \text{.....(12)}$$

where V_{dc_s}, v_{g_s}, i_{avg_s} and D_{1_s} are the dc-link voltage, the grid voltage, the average current and the duty ratio at the steady-state points, whereas ΔV_{dc_s}, Δv_{g_s}, Δi_{avg_s} and ΔD_{1_s} are the small signals of the dc-link voltage, the grid voltage, the average current and the duty ratio, respectively. The fluctuation of the dc-link voltage is considered to be small; consequently, the small signal of the dc-link voltage, i.e. the dc-link voltage dynamic, ΔV_{dc_s} is negligible. The circuit model in Fig. 4 is linearized at the steady-state points by substituting (9)-(12) into (8) [13].

Fig. 5 depicts the linearized circuit model of the inverter operating in DCM. In order to simplify the coefficients i_{avg_s} in the

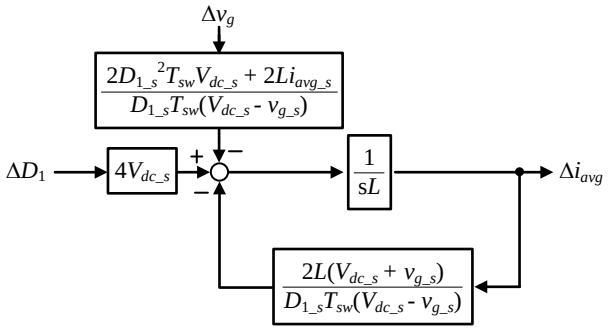


Fig. 5. Linearized circuit model of inverter operating in DCM. The current control of DCM obtains the same dynamic as in CCM by compensating the DCM nonlinearity at the output of the controller.

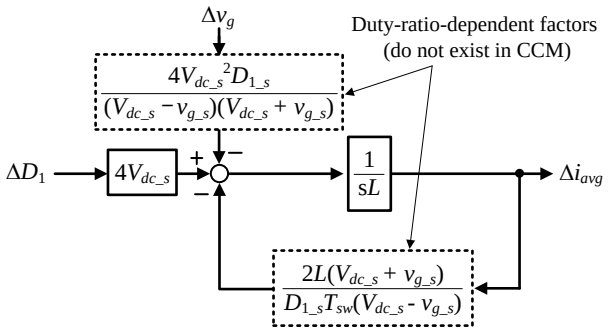


Fig. 6. Simplified and linearized circuit model. The value of the duty ratio D_{1_s} at steady-state points is required in order to compensate for the duty-ratio-dependent factors occurring when the inverter operates in DCM.

linearized circuit model, the relationship between the coefficients i_{avg_s} and the duty ratio D_{1_s} at the steady-state points are derived by substituting the differential of the inductor average current di_{avg}/dt in (8) as zero [13]-[14],

$$i_{avg\_s} = \frac{D_{1\_s}^2 T_{sw} V_{dc\_s} \left(V_{dc\_s} - v_{g\_s}\right)}{L\left(V_{dc\_s} + v_{g\_s}\right)} \quad \text{.....(13)}$$

Then, (13) is substituted into Fig. 5 in order to express all the coefficients as functions of the duty ratio D_{1_s}.

Fig. 6 shows the simplified and linearized circuit model. Two duty-ratio-dependent factors occur in the duty-ratio-to-current transfer function and the grid-voltage-to-current transfer function when the inverter operates in DCM. If these duty-ratio-dependent factors are compensated at the output of the controller, the same CCM current dynamic can be obtained when the inverter operates in DCM; therefore, the value of the duty ratio D_{1_s} at the steady-state points is necessary. In the conventional DCM nonlinearity compensation method [14], the value of D_{1_s} is estimated based on (14), which is derived from (13),

$$D_{1\_s} = \sqrt{\frac{Li_{avg\_s}\left(V_{dc\_s} + v_{g\_s}\right)}{T_{sw} V_{dc\_s}\left(V_{dc\_s} - v_{g\_s}\right)}} \quad \text{.....(14)}$$

where i_{avg_s}, V_{dc_s}, and v_{g_s} are extracted from the detection values of the average current, the dc-link voltage and the grid voltage. It is obvious that (14) is a function of the inductance L; consequently, the conventional DCM nonlinearity compensation method is

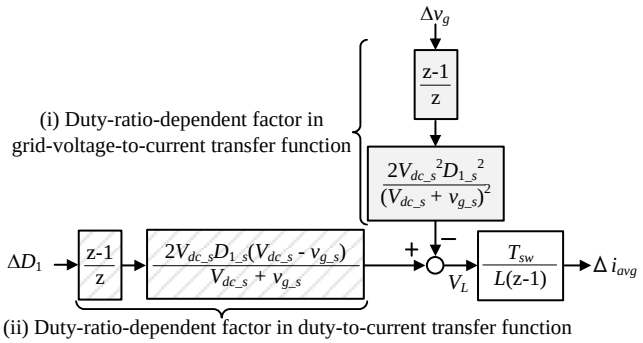
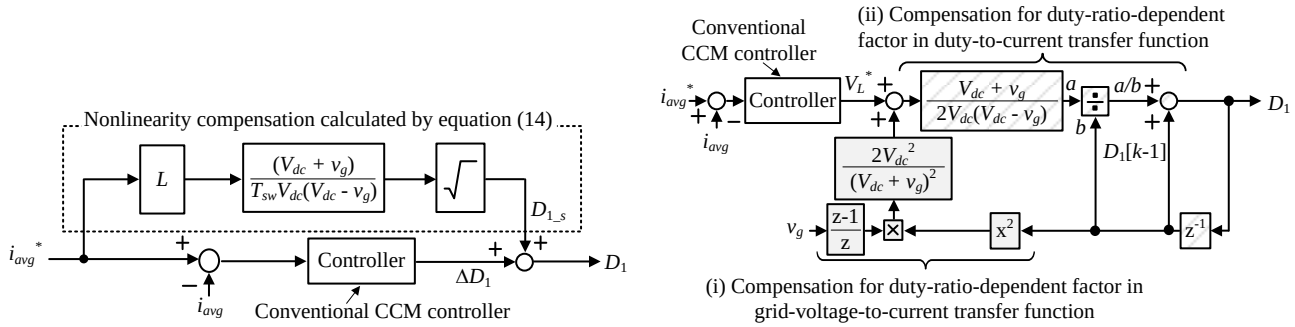


Fig. 7. Discretized circuit model of inverter operating in DCM. The original idea of the DCM nonlinearity compensation is to estimate the duty ratio at the steady-state points by the duty ratio at the previous calculation. Consequently, the inductance is not required in the DCM nonlinearity compensation.



(a) Conventional DCM nonlinearity compensation in [14] (b) Proposed DCM nonlinearity compensation

Fig. 8. Conventional and proposed DCM nonlinearity compensation. The main difference between the conventional and proposed method is that, the DCM nonlinearity compensation is constructed by utilizing the duty ratio at the previous calculation period; hence, this makes the control system inductance-independent.

inductance-dependent. The characteristic of circuit-parameter-dependency prevents the conventional method from the application of the residential PV systems, where the accurate value of L is difficult to obtain as mentioned in section II. On the other hand, the estimation of D_{1_s} by the duty ratio at the previous calculation period is proposed to avoid the dependency of L as the originality of this paper. Hence, the circuit model of the inverter operating in DCM is necessary to be analyzed in the discrete model of Fig. 6.

Fig. 7 depicts the discretized circuit model of the inverter operating in DCM. The duty-ratio-dependent factors in Fig. 7 are necessary to be set as 1 when the circuit operates in DCM in order to compensate the DCM nonlinearity at the output of the controller designed in CCM. In particular, the steady-state values of V_{dc_s} and v_{g_s} are obtained by the detection values of the dc-link voltage and the grid voltage, whereas the steady-state duty ratio D_{1_s} are estimated by the duty ratio $D_1[k\text{-}1]$ at the previous calculation period.

Fig. 8 illustrates the conventional DCM nonlinearity compensation in Fig. 10 of [14], and the proposed DCM nonlinearity compensation. The same principle of two methods is the estimation of D_{1_s} in order to compensate for the DCM nonlinearity. In the conventional method, D_{1_s} is estimated by using the current command i_{avg}^* and (14); consequently, this leads to the inductance-dependence. On the other hand, in the proposed method, D_{1_s} is estimated by using the duty ratio $D_1[k\text{-}1]$ at the previous

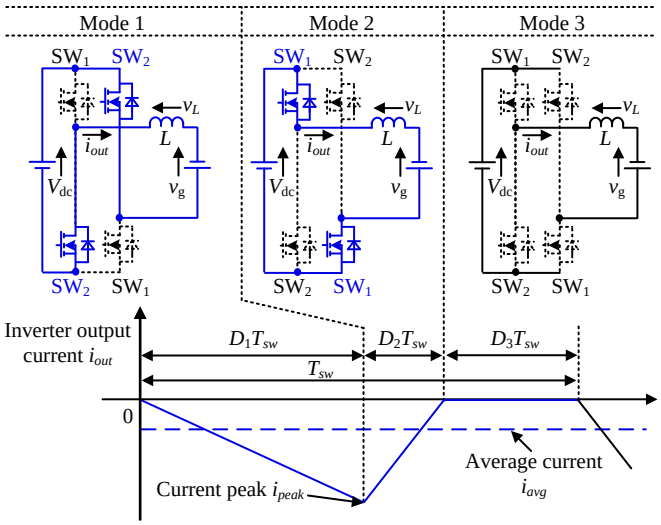


Fig. 9. Current path and inverter output current waveform in DCM when the grid voltage is negative. The same analysis procedure when the grid voltage is positive can be applied with the negative grid voltage.

calculation period, which provides the control system inductance-independence and the same CCM current response when the inverter operates in DCM [15]. Note that the above analysis is conducted when the grid voltage is positive; however, the same analysis procedure can be applied when the grid voltage is negative. For the sake of brevity, the derivation for the circuit model in DCM for the negative grid voltage is simplified as follows.

Fig. 9 depicts the current path and the inverter output current waveform in DCM when the grid voltage is negative. The same circuit model of Fig. 4 is obtained even when the grid voltage is negative; therefore, the similar DCM nonlinearity compensation is applied with the negative grid voltage. However, the applying order of mode 1 and mode 2 in Fig. 9 is flipped compared to that in Fig. 3, which implies that the output of the controller system D_1 in Fig. 8(b) has to be applied to the switch SW_1 when the grid voltage is positive, and inversely, D_1 has to be applied to the switch SW_2 when the grid voltage is negative. This switching signal generation is the main difference between the DCM operation and the CCM operation, where the switching signal of SW_2 in CCM is the inverse switching signal of SW_1. In the DCM operation, the inverse switching signal of each switch does not equal to the switching signal of the other switch due to the occurrence of the zero-current interval D_3T_{sw}. Meanwhile, the polarity of v_g in Fig. 8(b), which should always be positive, becomes negative when the grid voltage is negative because v_g is extracted from the detection value of the grid voltage. Therefore, the simple solution is to modify v_g in Fig. 8(b) into the multiplication of v_g and the polarity of i_{avg}^*.

Fig. 10 illustrates the proposed DCM current control for the grid-tied inverter and the variation of the duty ratio in DCM. Compared to Fig. 8(b), the multiplication of v_g and the polarity of i_{avg}^* is used in the compensation of the duty-ratio-dependent factors in order to obtain the DCM current dynamic as same as CCM regardless of the polarity of the grid voltage. The determination in which the output of the control system should be applied to SW_1 or SW_2, can be carried out by the comparison of

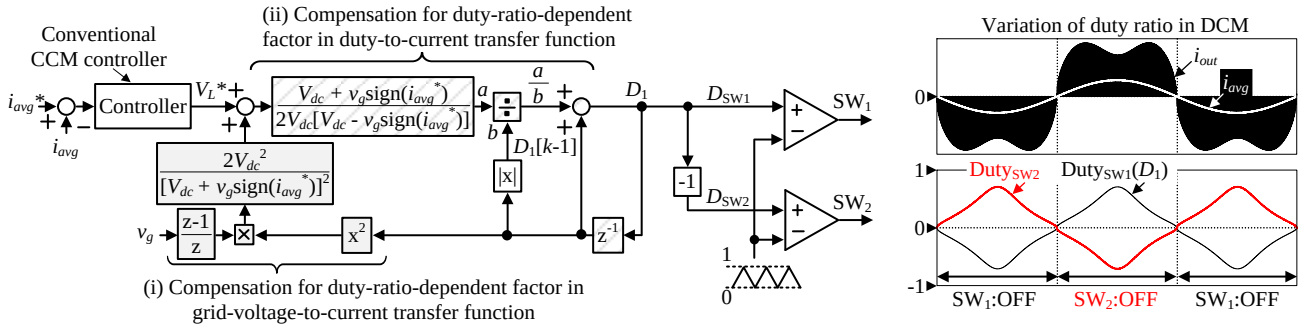


Fig. 10. Proposed DCM current control system for single-phase grid-tied inverter and variation of duty ratio in DCM. The polarity of D_1 is used to determine if D_1 should be applied to SW_1 or SW_2 in order to avoid the interruption of the continuous change of D_1.

the polarity of the grid voltage v_g or the current command i_{avg}^*. However, this method might interrupt the continuous change of D_1, because the actual current phase i_{avg} is lag compared to that of the current command i_{avg}^*. Instead, the polarity of D_1 is used to determine if D_1 should be applied to SW_1 or SW_2 in order to avoid the interruption of the continuous change of D_1. As mentioned above, the switching signal generation in DCM differs from that in CCM because both the switches SW_1 and SW_2 must be turned off during the zero-current interval D_3T_{sw}, which cannot be realized by the use of the inverse switching signal as in CCM. Therefore, the idea to operate the inverter under DCM is the alternate switching of SW_1 or SW_2 dependently on the polarity of D_1. Meanwhile, another difference between the CCM operation and the DCM operation observed from the variation of the duty ratio is that, the duty ratio of CCM only varies only around the value of 0.5, whereas the duty ratio in DCM decreases to zero when the average current reaches zero. The reason of the difference in the duty ratio variation is that the duty-ratio-to-current transfer function in CCM is linear, which implies the duty ratio does not relate to the average current but only the change of the average current, whereas the duty-ratio-to-current transfer function in DCM is nonlinear, which means the duty ratio depends on the average current. The proposed DCM current control system is employed when the inverter is operated entirely in DCM even at a rated load. However, this design results in an extremely high current ripple, which significantly increases a conduction loss in the switching devices and requires a larger heat sink [6], [30]. Therefore, a design of a moderate current ripple, in which the inverter operates in both CCM and DCM, is preferred in order to minimize the *LCL* filter without increasing the inverter loss.

B. Current Mode Determination

Fig. 11 indicates the relationship among the CCM duty, the DCM duty and the current mode. The current mode detection between CCM and DCM is necessary when the inverter is designed to operate in both CCM and DCM. One of the conventional current mode detection method is the detection of the zero current in DCM [18]. However, the zero current detection faces many challenges in practical applications, one of which is the current oscillation during the zero-current interval D_3T_{sw} shown in Fig. 3 and Fig. 9. In particular, this current oscillation is caused by the energy oscillation between the inductor L and the parasitic capacitance of the switches, which becomes more severe with a low inductance L and a high switching frequency [19]. As another

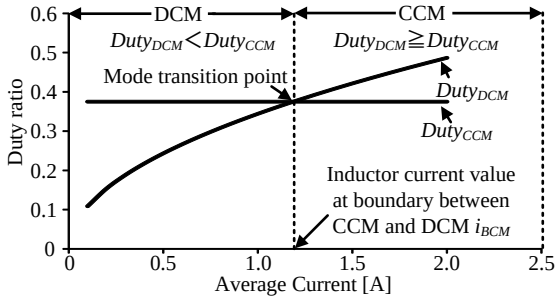
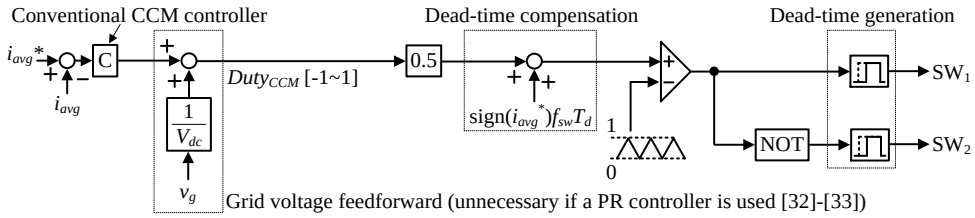


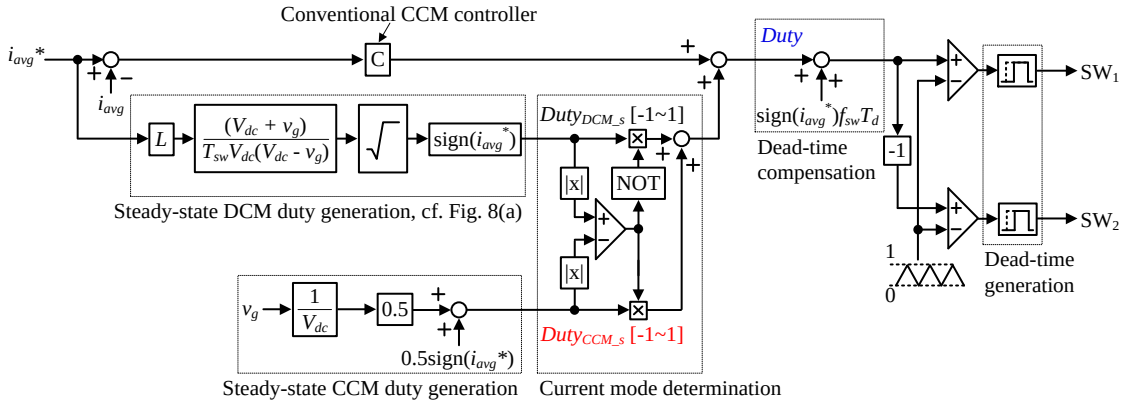
Fig. 11. Relationship among CCM duty, DCM duty and current mode. When the circuit operates in DCM, the DCM duty becomes smaller than the CCM duty and vice versa. The current mode determination is realized independently from the inductor value by using this relationship of the duty ratios.

typical approach, the detection value of the average current i_{avg} or the average current command i_{avg}^* is compared with the current value i_{BCM} at the boundary between CCM and DCM; if i_{avg} is larger than i_{BCM}, CCM is determined as the operation mode and vice versa [20]. However, the inductance is used in the calculation of i_{BCM} which implies the current mode determination is inductance-dependent. Consequently, when the actual inductor value is different from the nominal value, the current mode cannot be accurately determined by the conventional method. On the other hand, the proposed current mode determination focuses on the relationship among the CCM duty $Duty_{CCM}$, the DCM duty $Duty_{DCM}$ and the current mode. In particular, if $Duty_{CCM}$ is larger than $Duty_{DCM}$, DCM becomes the operation mode and vice versa. Note that $Duty_{CCM}$ is independent from the average current, whereas $Duty_{DCM}$ changes with the variation of the average current (cf. Fig. 10 of section III.A). In general, $Duty_{CCM}$ is the output value of the controller, which implies the calculation for $Duty_{CCM}$ is independent from the inductance. If the proposed DCM nonlinearity compensation in section III.A is employed, the calculation for $Duty_{DCM}$ also becomes inductance-independent. Consequently, if the relationship between $Duty_{CCM}$ and $Duty_{DCM}$ is used to determine the current mode, the inductance-independent current mode determination is achieved. In other words, the proposed inductance-independent DCM nonlinearity compensation in section III.A leads to the inductance-independent current mode determination.

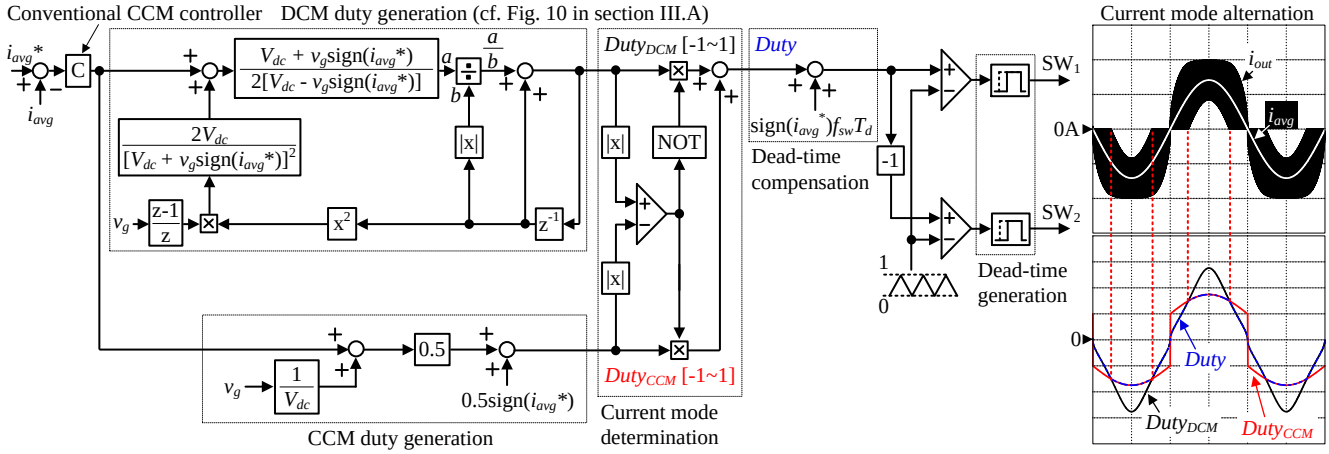
Fig. 12 describes the conventional CCM current control system, the conventional CCM/DCM current control system, and the proposed inductance-independent CCM/DCM current control system with the waveform of the current mode alternation. In the conventional CCM current control system, when a typical PI controller is employed, the grid voltage feedforward is required in order to enhance the disturbance suppression. Although the inductance might be used in the design of the controller, the conventional CCM current control system is inductance-independent per se if the bandwidth of the controller is properly designed [31]. Note that the grid voltage feedforward can be eliminated if the proportional-resonant (PR) controller is applied [32]-[33]. Meanwhile, a typical two-level dead-time compensation is employed to compensate the dead-time-induced error voltage [34]-[35]. Nevertheless, the conventional CCM current control system cannot compensate for the DCM nonlinearity when the zero-current phenomenon becomes noticeable as the current ripple increases. In the conventional CCM/DCM current control system, first, both



(a) Conventional CCM current control system



(b) Conventional CCM/DCM current control system, cf. Fig. 10 of [14]



(c) Proposed inductance-independent CCM/DCM current control system with waveform of current mode alternation.

Fig. 12. Conventional CCM current control system, conventional CCM/DCM current control system, and proposed inductance-independent CCM/DCM current control system with waveform of current mode alternation. The constant-gain conventional CCM current control system cannot compensate for the DCM nonlinearity, whereas the conventional CCM/DCM current control system is dependent on the inductance. On the other hand, the proposed CCM/DCM current control system compensates for the DCM nonlinearity and determines the current mode independently from the inductance.

the steady-state DCM duty $Duty_{DCM\_s}$ and the steady-state CCM duty $Duty_{CCM\_s}$ are generated. Then, these two duty ratios are compared to each other; the smaller duty ratio is feed forward to the output of the controller to compensate for the grid voltage disturbance in CCM or the nonlinearity in DCM. It is obvious that the conventional CCM/DCM current control system is

TABLE I
EXPERIMENTAL PARAMETERS.

Circuit Parameter		
V_{dc}	Dc-link voltage	350 V
v_g	Grid voltage	200 Vrms
P_n	Nominal power	4 kW
Switching device (SiC MOSFET)		SCT303AL (ROHM)
Core material and Litz wire		Ferrite N87, 504/ϕ0.1
f_g	Grid frequency	50 Hz
C_{dc}	Dc-link capacitance	2720 μF
C_f	Filter capacitance	4 μF
L_f	Filter inductance	20 μH
f_{sw}	Switching frequency	100 kHz
Current Controller Parameter		
f_{samp}	Sampling frequency	25 kHz
ζ	Damping factor	1.2
f_c	Cutoff frequency	1 kHz
T_d	Dead time	500 ns

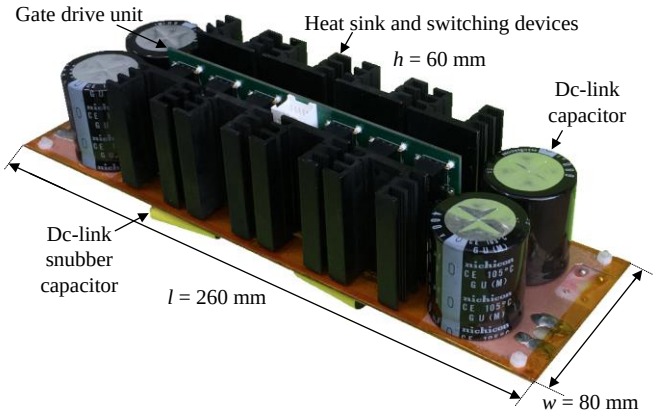
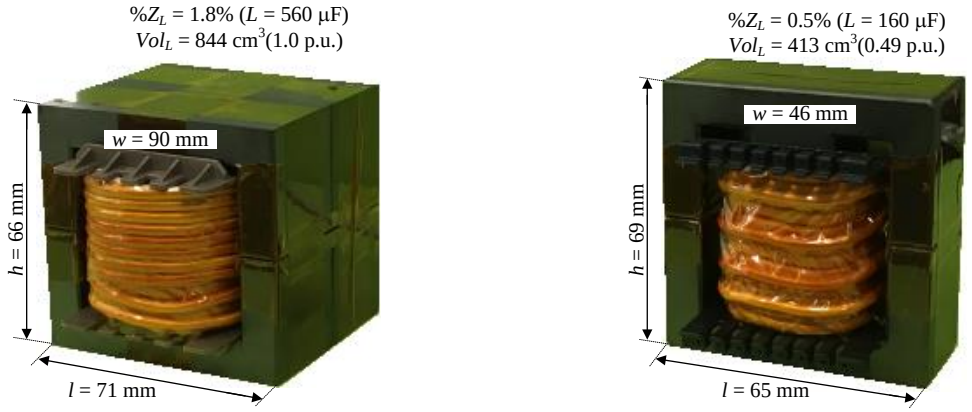


Fig. 13. 4-kW 100-kHz prototype of single-phase grid-tied inverter. SiC switching devices are chosen to operate the inverter at high switching frequency of 100 kHz, whereas two switching devices are connected in parallel to reduce the conduction loss in each device and enable the employment of natural cooling. Meanwhile, four electrolytic capacitors of 680-μF are connected in parallel at the dc link to absorb the single-phase power fluctuation and maintain a low dc-link voltage ripple.

dependent on *L*. In the proposed CCM/DCM current control system, first, both the DCM duty $Duty_{DCM}$ and the CCM duty $Duty_{CCM}$ are generated. Then, the absolute value of these two duty ratios are compared to each other; the smaller duty ratio is used to generate the switching signal for the switches. Note that the absolute operators are used with the consideration of the negative grid voltage as shown in the waveform of the current mode alternation in Fig. 12(c). The original idea of the inverter control for the operation in both DCM and CCM is that as first step, the duty ratio at the previous calculation period is used to compensate the DCM nonlinearity regardless of *L*, then two outputs of the inductance-independently generated duty ratios are compared to each other in order to determine the current mode. Consequently, the CCM/DCM current control system can perform the current control independently from *L*.

IV. LABORATORY SETUP

Table I depicts the experimental parameters, whereas Fig. 13 shows the 4-kW 100-kHz prototype of the single-phase grid-tied



(a) First design with inverter-side inductor impedance of 1.8%

(b) Second design with inverter-side inductor impedance of 0.5%

Fig. 14. Prototypes of inverter-side inductors under different conditions of inductor impedance. Note that only one inductor in one line indicated by $L/2$ in Fig. 1 is shown, whereas the impedance, the inductance and the inductor volume (including bobbins) are calculated from two inductors in two lines. In particular, the inductor volume is reduced by 51% due to the reduction of the inverter-side inductor impedance %Z_L from 1.8% to 0.5%.

inverter. With a relatively mature development, SiC switching devices are chosen to operate the inverter at the high switching frequency of 100 kHz; consequently, the *LCL* filter can be minimized due to a design of a high cutoff frequency. A natural cooling method is preferred for the residential PV systems in order to eliminate a periodic maintenance of cooling fans. Electrolytic capacitor with high ratio between the capacitance and volume is chosen to absorb the single-phase power fluctuation as a passive energy buffer method [27]. These capacitors are designed with a consideration of a capacitor current ripple to avoid a temperature rise due to an equivalent series resistance of capacitors, which is the main cause of the lifetime decrease of the electrolytic capacitor [36]. Note that the operation frequency of the microcontroller is synchronized with the sampling frequency of 25 kHz despite of the high switching frequency of 100 kHz; this enables the use of general-purpose microcontrollers. Furthermore, PI controller is chosen to use in the residential PV system due to its mature development and research. The dead time design is conducted in consideration of the following factors: the maximum drain current of 60 A, the gate resistor of 3 Ω, the maximum ambient temperature of 50ºC, and the high-volume production.

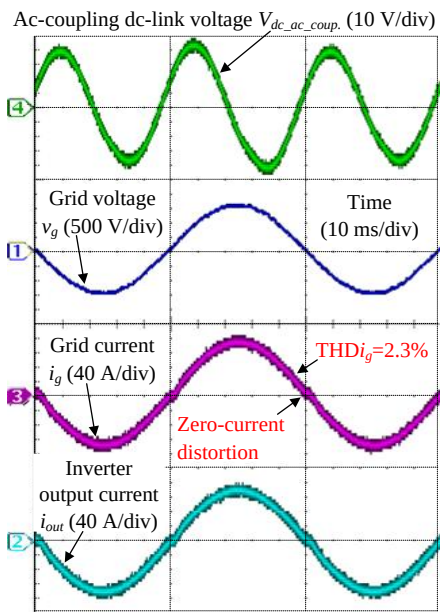
Fig. 14 depicts the prototypes of the inverter-side inductors L under different conditions of the inductor impedance %Z_L. Note that in the *LCL* filter design, the inductor impedance, which is normalized by the inverter total impedance, is generally used to compare the inductance. Ferrite is chosen to be the core material in order to minimize the core loss at the switching frequency of 100 kHz, whereas Litz wire is used to minimize the winding loss coming from the proximity effect and the skin effect [37]. The inverter-side inductor impedance is minimized with the consideration of the increase in the conduction loss of the switching devices due to the high inductor current ripple [30]. It can be observed that the inductor volume (including bobbins) is reduced by 51% when the inverter-side inductor impedance %Z_L is reduced from 1.8% to 0.5%. Note that the minimization of the inverter-side inductor impedance is also restricted due to the practical limits of the sampling frequency, the current sensor measurement, and the

current control bandwidth. For instance, the grid-tied inverter is required to meet the fault-ride-through (FRT) requirements of the grid code [38]; one of the regulations is that the current overshoot rate below 150% of the maximum current at rated load must be maintained even when the grid faults occur, e.g. the short-circuit of the grid. In the practical application, there is delay time in the current detection due to the current sensor or the sampling frequency. Consequently, the smaller the inductance is reduced, the more difficult to achieve the current overshoot rate below 150% of the maximum current at the rated load it becomes during the grid faults.

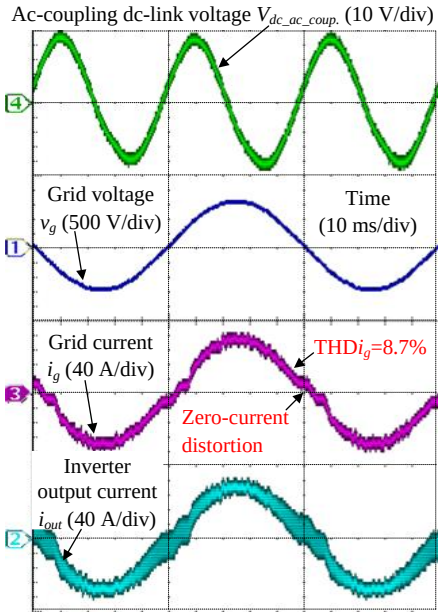
A. Operation Verification

Fig. 15 describes the inverter operation waveforms with the conventional CCM current control at a rated load of 4 kW and at a light load of 2 kW under two conditions of $\%Z_L$. Fig. 15(a)-(b) shows the operation waveforms at the rated load of 4 kW, whereas Fig. 15(c)-(d) shows the operation waveforms at the light load of 2 kW. Fig. 15(a), (c) shows the operation waveforms with $\%Z_L$ of 1.8%, whereas Fig. 15(b), (d) shows the operation waveforms with $\%Z_L$ of 0.5%. The grid current THD (up to 40^{th} order of the harmonic component) is measured by a YOKOGAWA WT1800 power meter. As mentioned in section II, the length of the zero-current clamping interval depends on the current ripple of the inverter output current i_{out}, the dead-time-to-switching-period ratio, and the power level. Note that the low-inductance design leads to the high switching current ripple; therefore, when $\%Z_L$ is reduced from 1.8% to 0.5%, the grid current THD at the rated load of 4 kW increases from 2.3% to 8.7% as shown in Fig. 15(a)-(b). Similarly, comparing Fig. 15(a)-(b) with Fig. 15(c)-(d), when the power level decreases from 4 kW to 2 kW, the grid current THD increases from 2.3% and 8.7% to 3.9% and 12.4%, respectively. According to standards such as IEEE-1547 [1], the grid current THD at the rated load must be lower than 5%; hence, the inductor impedance design of 0.5% with the conventional CCM current control system, of which the grid current THD at the rated load is 8.7%, does not satisfy the harmonic constraint. Consequently, it is confirmed by experimental results that the inductance reduction with the conventional CCM current control, of which the aim to achieve the small volume and low cost of the inductors, is limited due to the zero-current distortion.

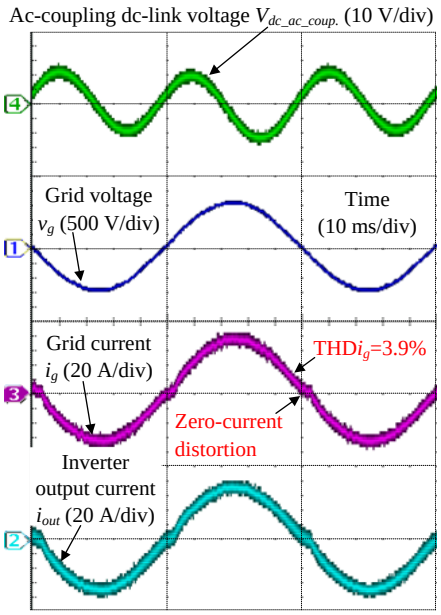
Fig. 16 describes the inverter operation waveforms with the proposed CCM/DCM current control at the rated load of 4 kW and at the light load of 2 kW under two conditions of $\%Z_L$. Fig. 16(a)-(b) shows the operation waveforms at the rated load of 4 kW, whereas Fig. 16(c)-(d) shows the operation waveforms at the light load of 2 kW. Fig. 16(a), (c) shows the operation waveforms with $\%Z_L$ of 1.8%, whereas Fig. 16(b), (d) shows the operation waveforms with $\%Z_L$ of 0.5%. It can be observed clearly from Fig. 16(b), (d) that the inverter is intentionally operated under DCM in the vicinities of the zero-current crossing. Due to the DCM nonlinearity compensation, the same current dynamic as CCM is achieved during the DCM interval; consequently, the zero-current distortion is eliminated. In particular, the proposed CCM/DCM current control reduces the grid current THD at the rated load from 8.7% to 2.1% compared to that of the conventional CCM current control with $\%Z_L$ of 0.5%. Therefore, the proposed CCM/DCM current control enables the minimization of the inverter-side inductor impedance without violating the harmonic constraint



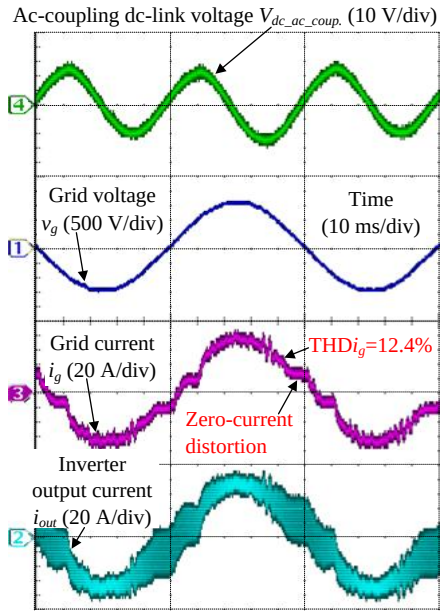
(a) Conventional CCM control, %Z_L=1.8%, rated load of 4 kW



(b) Conventional CCM control, %Z_L=0.5%, rated load of 4 kW



(c) Conventional CCM control, %Z_L=1.8%, light load of 2 kW

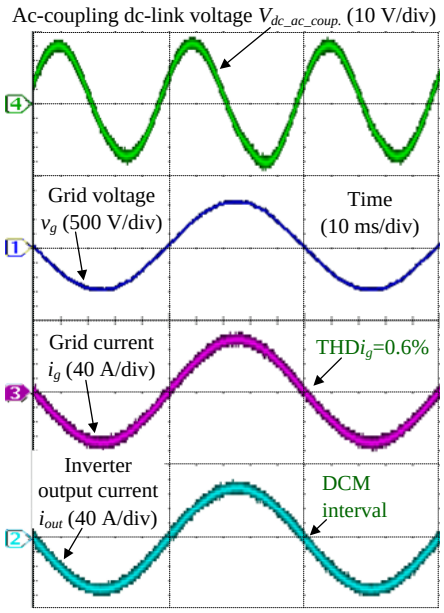


(d) Conventional CCM control, %Z_L=0.5%, light load of 2 kW

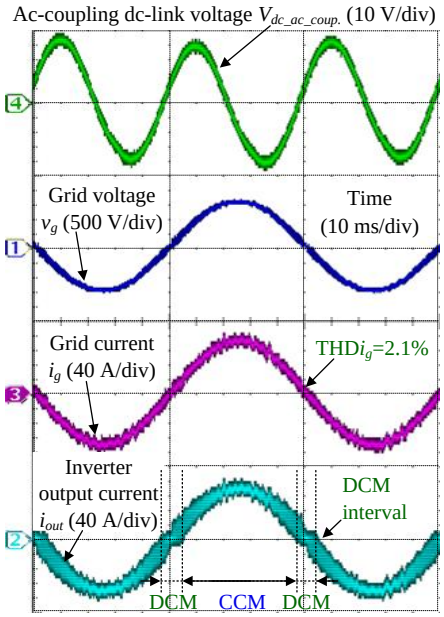
Fig. 15. Operation waveforms of conventional CCM control at rated load of 4 kW and at light load of 2 kW under two conditions of %Z_L. The low-inductance design results in the high current ripple, which increases the zero-current distortion with the conventional CCM control. Consequently, the grid current THD of 8.7% at the rated load with %Z_L of 0.5% does not satisfy the harmonic constraint regulated by standards such as IEEE-1547 [1].

regulated by standards such as IEEE-1547 [1].

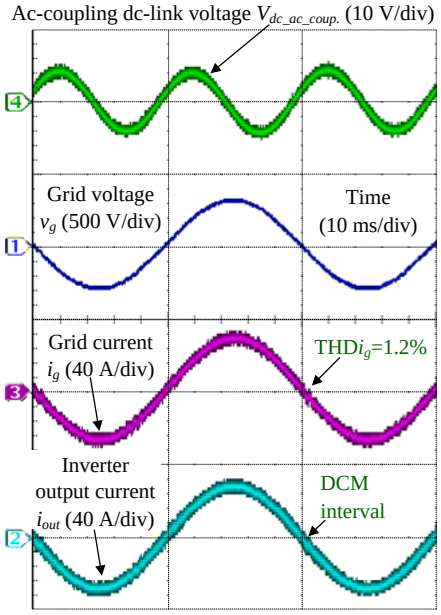
Fig. 17 depicts the comparison of the grid current THD and the power factor characteristics of the conventional CCM current control and the proposed CCM/DCM current control. Fig. 17(a)-(b) shows the grid current THD with %Z_L of 1.8% and 0.5%, whereas Fig. 17(c)-(d) shows the power factor with %Z_L of 1.8% and 0.5%, respectively. In Fig. 17(a)-(b), the proposed



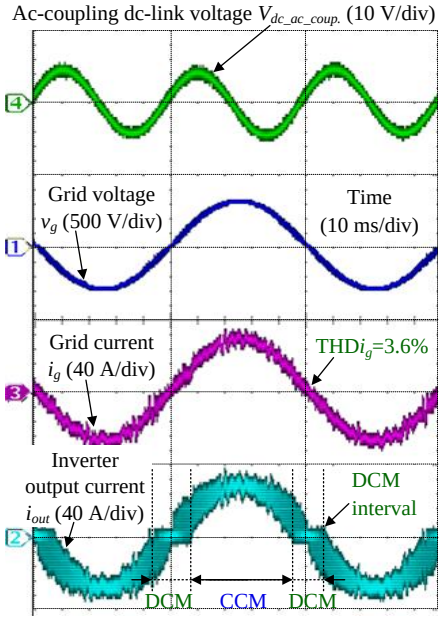
(a) Proposed CCM/DCM control, %Z_L=1.8%, rated load of 4 kW



(b) Proposed CCM/DCM control, %Z_L=0.5%, rated load of 4 kW



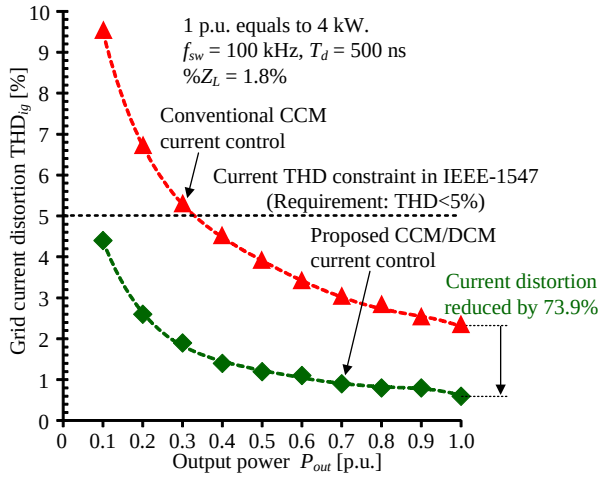
(c) Proposed CCM/DCM control, %Z_L=1.8%, light load of 2 kW



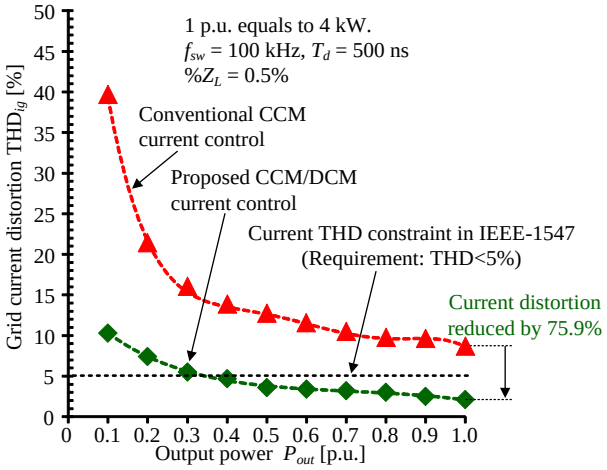
(d) Proposed CCM/DCM control, %Z_L=0.5%, light load of 2 kW

Fig. 16. Operation waveforms of proposed CCM/DCM control at rated load of 4 kW and at light load of 2 kW under two conditions of %Z_L. Even with %Z_L of 0.5%, the proposed CCM/DCM current control can still maintain the grid current THD at the rated load below 5%, which satisfies the harmonic constraint regulated by standards such as IEEE-1547 [1].

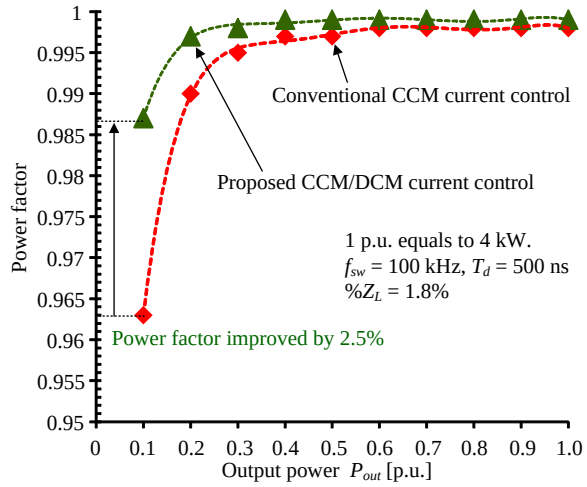
CCM/DCM current control reduces the current distortion at the rated load by 73.9% and 75.9% with %Z_L of 1.8% and 0.5% compared to those of the conventional CCM current control, respectively. Moreover, the grid current THD over entire load range from 0.1 p.u. to 1.0 p.u. is reduced with the proposed CCM/DCM current control. Consequently, the power factors of the proposed CCM/DCM current control over entire load range from 0.1 p.u. to 1.0 p.u. with %Z_L of 1.8% and 0.5% are improved compared to



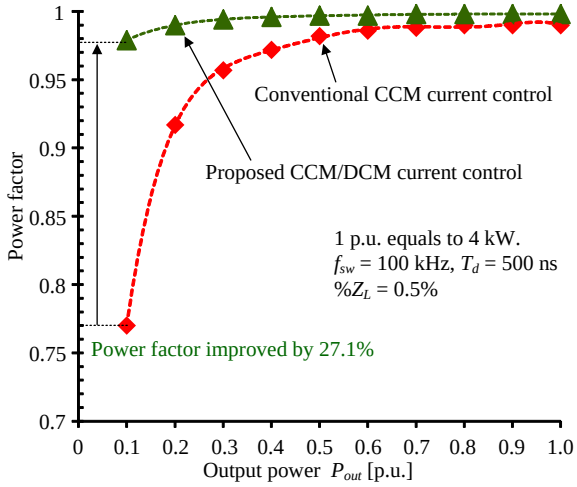
(a) Grid current THD characteristic of %Z_L=1.8%



(b) Grid current THD characteristic of %Z_L=0.5%



(c) Power factor characteristic of %Z_L=1.8%



(d) Power factor characteristic of %Z_L=0.5%

Fig. 17. Grid current THD and power factor characteristics of conventional CCM current control and proposed CCM/DCM current control. The proposed CCM/DCM current control reduces the current distortion at the rated load by 73.9% and 75.9% with %Z_L of 1.8% and 0.5% compared to those of the conventional CCM current control, respectively. Furthermore, the power factors of the proposed CCM/DCM current control over entire load range from 0.1 p.u. to 1.0 p.u. with %Z_L of 1.8% and 0.5% are also improved compared to those of the conventional CCM current control.

those of the conventional CCM current control as shown in Fig. 17(c)-(d), respectively. In particular, the power factor at the light load of 0.1 p.u. with %Z_L of 0.5% is improved by 27.1% when the proposed CCM/DCM current control is applied.

Fig. 18 describes the inverter operation waveforms with the proposed CCM/DCM current control under low power factor with %Z_L of 0.5%. During normal operation, the grid-tied inverter is required to operate at unity power factor with maximum power point tracking in order to extract as much energy as possible from the PV panels [32]. However, when the grid variations occur, i.e. frequency instability or grid voltage sag, the grid-tied inverter is also necessary to operate under low power factor [33]. As shown in Fig. 18, the proposed CCM/DCM current control still maintains a low grid current THD under the low power factor.

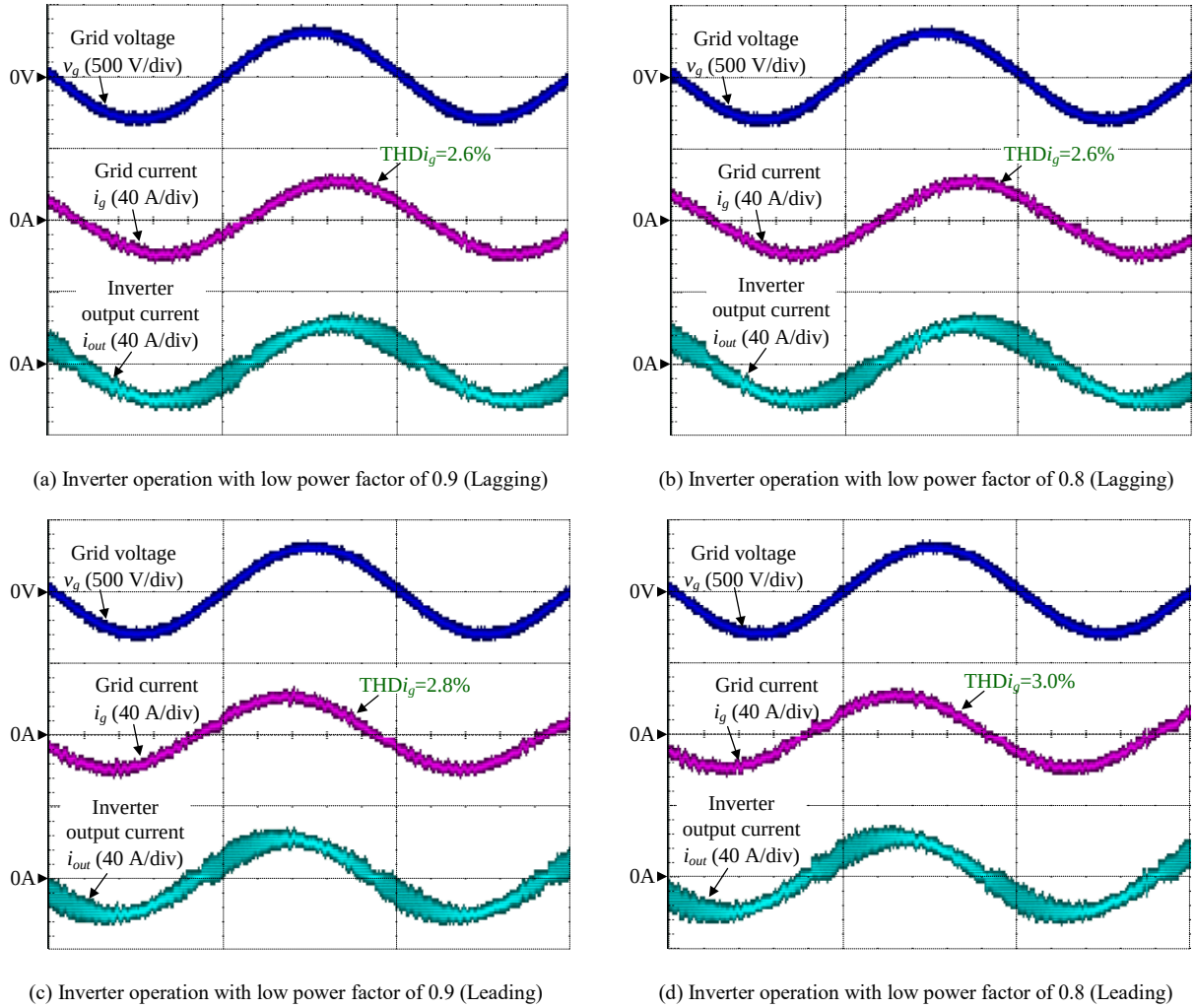
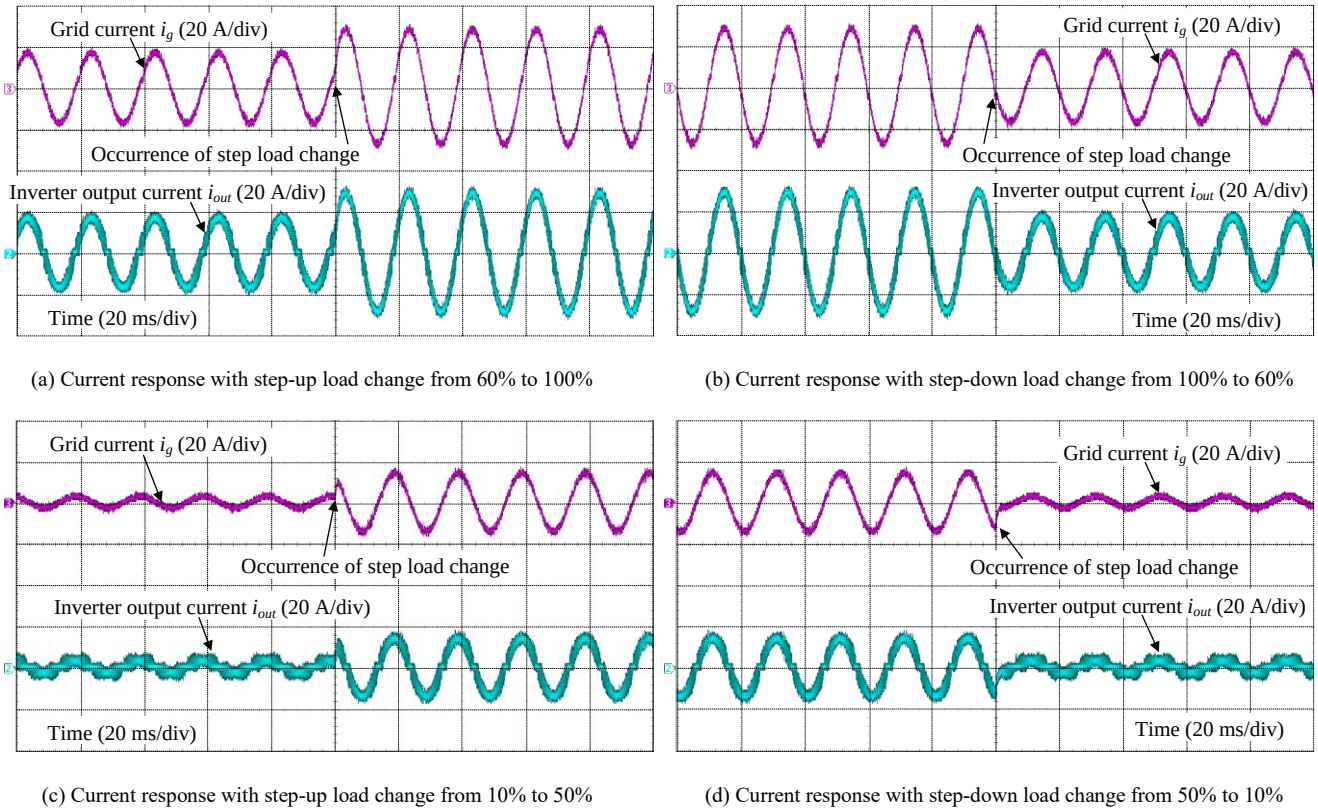


Fig. 18. Proposed CCM/DCM current control operation under low power factor with %Z_L of 0.5%. When the grid variations occur, i.e. frequency instability or grid voltage sag, the grid-tied inverter is necessary to operate under a low power factor in order to avoid more serious events, e.g. power outage or voltage flickering.

Fig. 19 describes the inverter operation waveforms with the proposed CCM/DCM current control under step load change with %Z_L of 0.5%. Fig. 19 (a)-(b) shows the current response with the step load change from 60% to 100% and vice versa, whereas Fig. 19 (c)-(d) depicts the current response with the step load change from 10% to 50% and vice versa, respectively. Note that the step load change in Fig. 19 (a)-(b) occurs in the vicinities of the zero-current crossing, i.e. the DCM interval, whereas the step load change in Fig. 19 (c)-(d) occurs at the current peak, i.e. the CCM interval. It is observed that the transient waveform has low overshoot and fast convergence regardless of the moment of the step load change occurrence.

B. Comparison of Efficiency, Inductor Material Cost and Computation Time

Fig. 20 depicts the efficiencies and the loss distribution with the proposed CCM/DCM current control with %Z_L of 1.8% and 0.5%. The efficiencies are measured by a YOKOGAWA WT1800 power meter, whereas the semiconductor device losses and the inductor losses are obtained from simulators, i.e. PLECS and GeckoMAGNETICS. In Fig. 20(a), the maximum efficiency of 97.9% is achieved with %Z_L of 0.5% from the load range of 0.6 p.u. to 0.9 p.u., whereas the efficiency at the rated load of 4 kW is



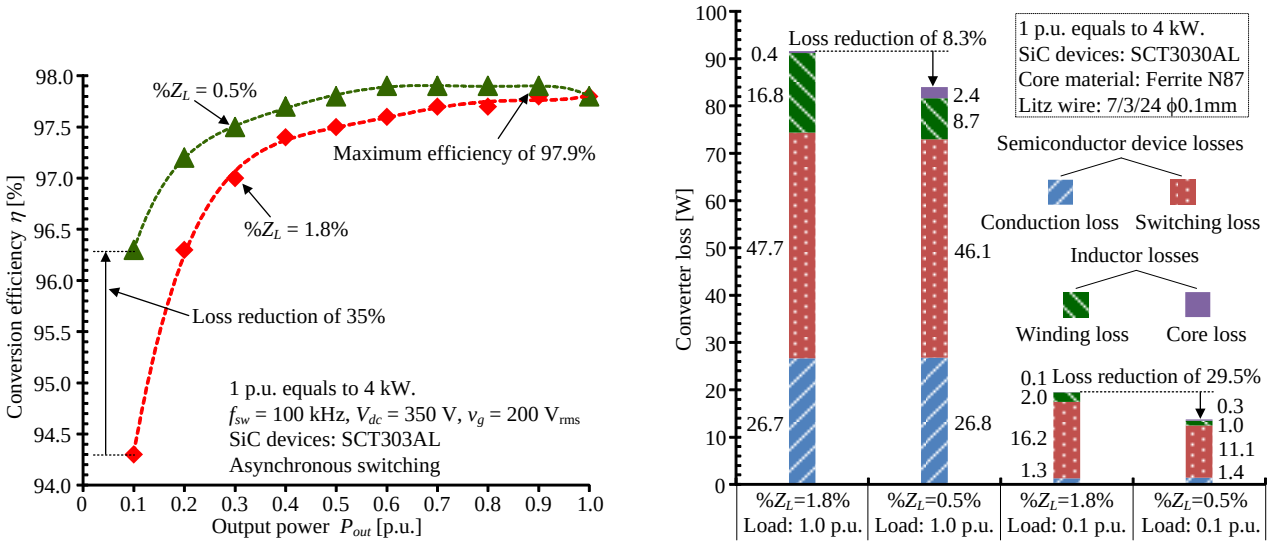
(a) Current response with step-up load change from 60% to 100%

(b) Current response with step-down load change from 100% to 60%

(c) Current response with step-up load change from 10% to 50%

(d) Current response with step-down load change from 50% to 10%

Fig. 19. Proposed CCM/DCM current control operation under step load change with %Z_L of 0.5%. The transient waveform has low overshoot and fast convergence when the step load change occurs either in the vicinities of the zero-current crossing, i.e. the DCM interval, or at the current peak, i.e. the CCM interval.



(a) Efficiency characteristics

(b) Loss distribution

Fig. 20. Efficiency and loss distribution with proposed CCM/DCM current control with %Z_L of 1.8% and 0.5%. The maximum efficiency of 97.9% is achieved over a wide load range from 0.6 p.u. to 0.9 p.u.. The switching loss and conduction loss of SiC devices occupies for a majority of the converter loss. Therefore, the efficiency might be further improved by the application of GaN devices to reduce the switching loss and the employment of the synchronous switching to reduce the conduction loss.

97.8%. The efficiency with $\%Z_L$ of 0.5% is higher than that with $\%Z_L$ of 1.8% over entire load range; in specific, the loss at the light load of 0.1 p.u. with $\%Z_L$ of 0.5% is reduced by 35% compared to that with $\%Z_L$ of 1.8%. This efficiency improvement especially benefits the PV application with a frequent variation between the light load operation and the heavy load operation. In Fig. 20(b), the converter losses with $\%Z_L$ of 1.8% and 0.5% at the rated load of 1.0 p.u. and the light load of 0.1 p.u. are demonstrated. At the rated load of 1.0 p.u., compared to $\%Z_L$ of 1.8%, the conduction loss and the core loss with $\%Z_L$ of 0.5% increase, whereas the switching loss and the winding loss with $\%Z_L$ of 0.5% decrease. The increase in the conduction loss and the core loss occurs due to the increase of the current ripple when $\%Z_L$ is reduced from 1.8% to 0.5%. On the other hand, the reduction of $\%Z_L$ requires less winding wire in the inductor; consequently, the winding loss of the inductor decreases. Regarding to the switching loss, there are two main factors causing the decrease in the switching loss when $\%Z_L$ is reduced from 1.8% to 0.5%: the increase in the current ripple, and the DCM operation in the vicinities of the zero-current crossing. First, compared to the low current ripple, the high current ripple makes the semiconductor devices turn off at higher current and turn on at lower current, which results in the increase in the turn-off switching loss and the decrease in the turn-on switching loss. In SiC-MOSFET, the turn-on switching loss are usually higher than the turn-off switching loss due to the occurrence of the diode reverse recovery and the parasitic capacitance discharge at the turn on. Hence, the increase in the current ripple benefits the reduction in the switching loss. Second, during the DCM operation, the turn-on loss is significantly reduced due to zero-current turn-on. Hence, the increase in the current ripple results in longer DCM intervals around the zero-current crossing points, which helps to reduce the switching loss. This switching loss reduction effect with the DCM operation is clearly observed at the light load of 0.1 p.u., where the DCM interval becomes longer. In particular, at the light load of 0.1 p.u., compared to $\%Z_L$ of 1.8% (low current ripple, short DCM intervals), the switching loss of $\%Z_L$ of 0.5% (high current ripple, long DCM intervals) is reduced from 16.2 W to 11.1 W. Furthermore, it can be concluded from Fig. 20(b) that the switching loss and conduction loss of SiC devices occupies for a majority of the converter loss. Therefore, the efficiency might be further improved by the application of GaN devices to reduce the switching loss and the employment of the synchronous switching to reduce the conduction loss. Note that the difference in the loss reduction between Fig. 20(a) and (b), occurs due to the loss calculation error in the simulators.

Fig. 21 describes the cost breakdown of the inverter-side inductor material under two designs of $\%Z_L$. The ferrite core material can provide a lower core loss at the high switching frequency of several hundreds of kHz compared to other core materials such as, e.g. silicon steel, amorphous iron or nanocrystals [41]-[42]. Nevertheless, a ferrite characteristic of a low saturation flux density requires a large amount of the core material. Consequently, the core material cost dominates the overall inductor material cost.

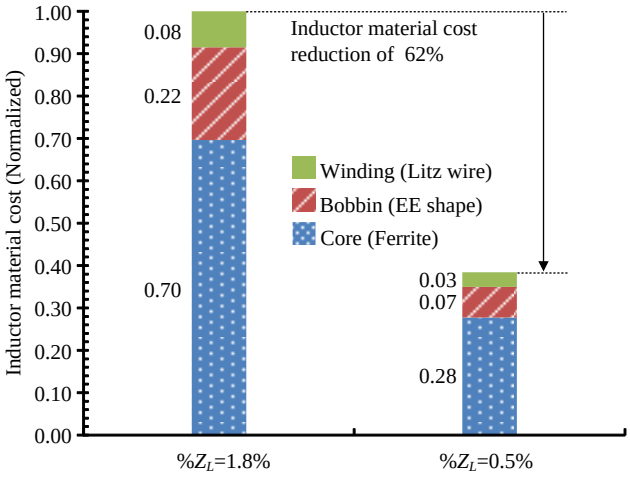


Fig. 21. Cost breakdown of inverter-side inductor material under two designs of %Z_L. A cost reduction of 62% in the inductor material is achieved when decreasing the inverter-side inductor impedance from 1.8% to 0.5%. Note that the cost calculation is based on the actual price of the prototype components, and is normalized by the %Z_L design of 1.8%.

TABLE II
COMPUTATION TIME IN CLOCK CYCLES OF CURRENT CONTROL LOOP.

Computation time [clock cycles]	Conventional CCM control (cf. Fig. 12(a))	Conventional CCM/DCM control (cf. Fig. 12(b))	Proposed CCM/DCM control (cf. Fig. 12(c))
PI controller	15	15	15
Grid voltage feedforward	4	0	0
CCM duty generation	0	8	9
DCM duty generation	0	36	37
Current mode determination	0	12	12
Dead-time compensation	8	8	8
Total	27 (1 p.u.)	79 (2.9 p.u.)	81 (3.0 p.u.)

Furthermore, a cost reduction of 62% in the inductor material is achieved with the decrease in the inverter-side inductor impedance from 1.8% to 0.5%.

Table II shows the approximate computation time for all the arithmetic operations in three current control loops shown in Fig. 12. Both division and square root digital calculations are time-consuming computation involving multiple clock cycles. In particular, when a STM32 Cortex-M4 microcontroller is applied to process 32-bit floating-point single-precision data, 14 clock cycles are required for a division or square root calculation, whereas 1 clock cycle is required for an addition or subtraction and 3 clock cycles are required for a multiplication [43]. Note that the computation time for the division calculations can be shorten by using a look-up table [44]. In the conventional CCM current control, only additions and multiplication are required for three operations, i.e. the PI

controller, the grid voltage feedforward and the dead-time compensation. Therefore, the computation time of the conventional CCM current control is the shortest with 27 clock cycles. In the conventional CCM/DCM current control, a square root calculation is required to compute the DCM duty ratio as shown in Fig. 12(b), and two additional operations, i.e. the DCM duty generation and the current mode determination, are necessary. Meanwhile, in the proposed CCM/DCM current control, a square root calculation is unnecessary; however, multiple additions and multiplications are required in order to generate the DCM duty as shown in Fig. 12(c). Therefore, the computation time of the conventional and proposed CCM/DCM current control becomes approximately 3 times longer than that of the conventional CCM current control. Hence, the minimization of the inverter-side inductor is a trade-off between the computation time and the grid current THD.

V. Conclusion

This paper presented a current mode control for the single-phase grid-tied inverter operating in both CCM and DCM in order to reduce the filter inductance without worsening the grid current THD. The proposed CCM/DCM current control satisfied the harmonic constraint defined in the grid standard such as IEEE-1547 even when the inverter-side inductor impedance is significantly reduced from 1.8% to 0.5%. The proposed CCM/DCM current control was compared with the conventional CCM current control and the conventional CCM/DCM current control.

First, with the employment of the conventional CCM current control, the grid current THD increased from 2.3% to 8.7% due to the zero-current clamping phenomenon when the inductor impedance was minimized from 1.8% to 0.5%. The conventional CCM current control could not compensate for the DCM nonlinearity to maintain the same current dynamic when the zero-current clamping occurred. On the other hand, the proposed CCM/DCM current control compensated for the DCM nonlinearity and reduced the grid current THD from 8.7% to 2.1% even with the low inductor impedance of 0.5%. Consequently, this inductor impedance minimization achieved the reductions of 51%, 62% and 35% in the inductor volume, the inductor material cost and the inverter loss at the light load of 0.1 p.u., respectively. However, these improvements was traded off by the long computation time of the proposed CCM/DCM current control which was 3 times longer than that of the conventional CCM current control.

Second, in the conventional CCM/DCM current control, the inductance must be used in the DCM nonlinearity compensation, which made the control system dependent on the circuit parameter. This restricted the application of the conventional CCM/DCM current control method to the residential PV systems, where the accurate value of the inductance was generally difficult to obtain. On the other hand, the proposed CCM/DCM current control utilized the duty ratio at the previous calculation in order to both compensate for the DCM nonlinearity and detect the current modes regardless of the inductance.

A further research topic in this field is the development of the CCM/DCM current control for other topologies where the operation in both CCM and DCM can provide improvements such as, e.g. boost converters, three-phase grid-tied inverters,

modular multilevel converters or flying capacitor multilevel converters, etc. The analysis procedure of the DCM nonlinearity and the approach of the CCM/DCM current control in this paper are demonstrated in detail for the single-phase grid-tied inverter. However, the derivation steps of the proposed CCM/DCM current control in this paper can be contributed as analysis guidelines for other converters.

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