Optimization for the Number of Parallel-connected Switching Devices in High-efficiency High-power Converters

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Abstract

This paper proposes an optimal design method for a high-efficiency and high-power converters. The system efficiency is improved by the design of the converters with the some small-current-rating parallel-connected devices, which achieve fast switching and low switching loss. The optimal number of parallel-connected SiC-MOSFETs for the maximum system efficiency is determined to achieve the reduction in both the conduction and the no-load loss due to drain-source parasitic capacitance of a SiC-MOSFET. The experimental results confirm that the optimal number of parallel-connected SiC-MOSFETs which leads to the smallest total device losses exists.

1 Introduction

Recently, grid-tied inverters such as photovoltaic systems, wind turbine systems have been actively studied for energy conservation [1]–[3]. The grid-tied inverter must have a small volume to increase the power density of the system. The wide band gap device such as silicon carbide metal-oxide-semiconductor field-effect transistor (SiC-MOSFET) allows a lower device loss and higher switching frequency; consequently, the heatsink and the interconnected inductors can be shrunk [4]–[5]. In high-power converter applications, several SiC-MOSFET chips, connected in parallel, are necessary for an increase of the converter current capacity.

In a parallel drive of SiC-MOSFETs, steady and transient current imbalance, leading a low system reliability, might occur between these paralleled SiC-MOSFETs due to the device parameters (such as R_{on} and V_{th}) and circuit stray inductance mismatches [6]. Then, some research works tried to balance the transient current imbalance [7]–[8]. As noted above, the parallel-connected SiC-MOSFETs has to deal with many challenges; thus, the number of parallel-connected SiC-MOSFETs should be only large enough to allow the system rated current, i.e. the minimum required number.

On the other hand, new design method to improve the system efficiency by increasing the number of parallel-connected power devices and reducing the conduction loss has been proposed [9]. This design method is based on the premise that the total switching loss are unchanged even when the number of parallel-connected devices increases. However, the turn-on loss actually includes voltage-current cross-over loss and so-called “no-load loss” due to the discharge of the drain-source parasitic capacitance of SiC-MOSFET [10]. Furthermore, the gate drive loss increases as the number of driven SiC-MOSFETs increase. Therefore, it is necessary to determine the optimal number of parallel-connected devices for a high system efficiency with the aim of the reduction in not only the conduction loss but also the no-load loss and the gate drive loss.

This paper presents the analysis about the relationships between each losses in the paralleled SiC-MOSFETs and the number of parallel-connected SiCMOSFETs. In addition, the relationship between the required cooler performance and the parallel number is also clarified. The calculation results based on the 50 kW three-phase grid-tied inverter confirm that the low-current-rating SiC-MOSFET achieves the low switching losses and be advantageous for the high system efficiency. Furthermore, the experimental results using 4 kW three-phase inverter confirm that the number of parallel-connected SiC-MOSFETs should be carefully

selected for achieving the high system efficiency with the considerations of all the conduction loss and the no-load loss due to the drain-source parasitic capacitance and the gate drive loss.

2 Relationship between Losses and Number of Parallel-Connected Devices

Power device losses can be classified into the conduction loss P_{cond} which is proportional to the square of the current, the switching loss P_{sw} which is proportional to the current, and the current-independent no-load loss P_{Cds}.

$$P_{loss} = P_{cond} + P_{sw} + P_{Cds}. \tag{1}$$

2.1 Conduction Loss

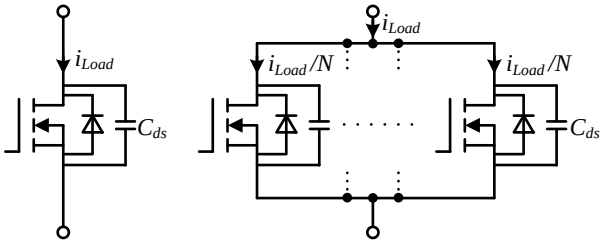
Fig. 1 shows the configuration examples of parallel-connected switches. The stray resistances and inductances are neglected and the load current i_{Load} are assumed to be equally divided by the paralleled SiC-MOSFETs. In addition, the on-resistances of SiC-MOSFETs are sufficiently small and the forward voltage drop of the body diode is high due to the large bandgap of SiC [11]; therefore, both the forward and inverse currents flow in MOSFET except for the dead-time period. Assuming that the dead-time is sufficiently short and negligible, the conduction loss of a body diode during the dead-time is also negligible. Under these assumptions, the conduction loss of the paralleled SiC-MOSFETs can be calculated as

$$\begin{aligned} P_{cond} &= N \times \frac{1}{2} r_{on} \left(\frac{1}{N} \cdot \frac{I_m}{\sqrt{2}} \right)^2 \\ &= \frac{r_{on} I_m^2}{4N} \end{aligned} \tag{2}$$

where N is the number of parallel-connected SiC-MOSFETs, r_{on} is the on-state resistance, and I_m is the maximum value of the load current. The conduction loss is inversely proportional to the number of parallel-connected SiC-MOSFETs.

2.2 Switching Loss

Fig. 2 shows the relationship between switching loss energies of SiC-MOSFET (SCT3080KL, Rohm) and a drain current [12]. In this paper, the switching loss is defined as the sum of turn-on loss, turn-off loss, and body diode reverse recovery loss. The body diode of SiC-MOSFET is a P-N junction diode with short minority carrier lifetime [11]. This fact enables a fast recovery performance; thus, the diode reverse recovery loss is negligible. The switching loss of the paralleled SiC-MOSFETs can be calculated as



(a) 1 device / 1 arm. (b) N devices / 1 arm.

Fig. 1: Arm configuration examples.

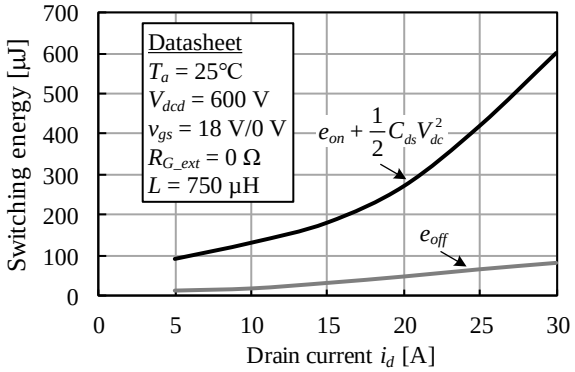


Fig. 2: Switching loss energies of SCT3080KL, Rohm versus drain current.

$$\begin{aligned} P_{sw} &= N \cdot \left\{ \frac{V_{dc} \left(e_{on} + e_{off} \right) f_{sw}}{V_{dcd} I_{md}} \right\} \cdot \frac{1}{2\pi} \int_0^{2\pi} \left| \frac{I_m}{N} \sin(\theta + \varphi) \right| d\theta \\ &= \left\{ \frac{V_{dc} I_m \left(e_{on} + e_{off} \right) f_{sw}}{V_{dcd} I_{md}} \right\} \cdot \frac{1}{2\pi} \int_0^{2\pi} \left| \sin(\theta + \varphi) \right| d\theta \end{aligned} \tag{3}$$

where V_{dc} is the DC-link voltage, e_{on} and e_{off} are the voltage-current cross-over turn-on and turn-off energies per one switching transition, V_{dcd} and I_{md} are the voltage and current when e_{on} and e_{off} are measured, and f_{sw} is the switching frequency. Assuming that the turn-on and turn-off losses are almost proportional to the drain current, the total switching loss is unchanged even when the number of parallel-connected SiC-MOSFETs changes.

2.3 No-load Loss due to Discharge of Drain-Source Parasitic Capacitance

When the SiC-MOSFET turns off with the voltage applied between the drain and source, the drain-source parasitic capacitance C_{ds} is charged. Consequently, the energies stored in the parasitic capacitance are consumed as the joule loss in the on-state resistance at the next turn-on hard switching [10]. Therefore, the no-load loss is described with the turn-on loss as the black line in Fig. 2 and calculated as

$$P_{Cds} = N \times \frac{1}{2} C_{ds} V_{dc}^2 f_{sw}. \quad (4)$$

The no-load loss is proportional to the number of parallel-connected SiC-MOSFETs.

2.4 Gate Drive Loss

In addition to the power device losses in (1), the power consumed by the SiC-MOSFET gate drive circuit also contributes the system efficiency. The power consumption of the gate drive circuit can be calculated as [13]

$$P_{drive} = N \times Q_g V_{gs} f_{sw} \quad (5)$$

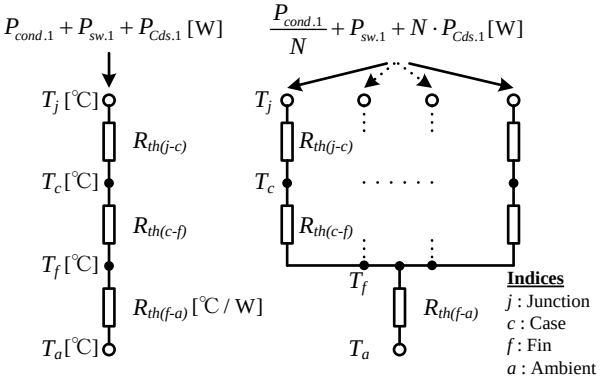
where Q_g is the total gate charge, and V_{gs} is the gate-source voltage. The gate drive loss is also proportional to the number of parallel-connected SiC-MOSFETs as the no-load loss.

3 Relationship between Required Cooler Performance and Number of Parallel-Connected Devices

Fig. 3 shows the heat equivalent circuits of each arm with thermal resistances R_{th}. The case where only one switch is attached to the heatsink is shown in Fig. 3(a), and the case where the plural parallel-connected switches are attached to the heatsink is shown in Fig. 3(b), respectively. In this section, the required thermal resistance of heatsink $R_{th(f\text{-}a)}$ is calculated as the required cooler performance. Besides, the thermal resistance between case and fin $R_{th(c\text{-}f)}$ is neglected. In the case where one switch is attached to the heatsink shown in Fig. 3(a), the relationship between the junction temperature and the power device losses can be expressed as

$$T_j = \left(P_{cond.1} + P_{sw.1} + P_{Cds.1}\right) \cdot \left(R_{th(j-c)} + R_{th(f-a)}\right) + T_a \quad (6)$$

where $P_{cond.1}$, $P_{sw.1}$, and $P_{Cds.1}$ are the conduction loss, switching loss, and no-load loss in the case



(a) 1 device / 1 arm. (b) N devices / 1 arm.

Fig. 3: Heat equivalent circuits of each arm with thermal resistances.

where the arm consists of only one switch. The required heat sink thermal resistance $R_{th(f\text{-}a).req}$ such that the junction temperature does not exceed its absolute maximum rating $T_{j.\max}$ can be calculated as

$$R_{th(f-a).1.req} \le \frac{T_{j.\max} - T_a}{P_{cond.1} + P_{sw.1} + P_{Cds.1}} - R_{th(j-c)}. \quad (7)$$

The required heatsink thermal resistance in the case where the arm consists of plural switches connected in parallel shown in Fig. 3(b) can be calculated in the same way above as

$$R_{th(f-a).N.req} \le \frac{T_{j.\max} - T_a}{\frac{P_{cond.1}}{N} + P_{sw.1} + N \cdot P_{Cds.1}} - \frac{R_{th(j-c)}}{N}. \quad (8)$$

Expressions (7) and (8) confirm that the heatsink of which thermal resistance is higher is applicable as the number of parallel-connected devices increases in case where the sum of the conduction loss and the no-load loss can be reduced by increasing the parallel number. Besides, the first term of (8) becomes dominant as the parallel number increases. The cooler of the power converter is generally designed at the maximum power and the maximum loss point, where the conduction loss is dominant. For the above reasons, the required heatsink thermal resistance in (8) can be regarded as roughly proportional to the parallel number N. Therefore, the heatsink becomes shrunk as the parallel number increases compared to the case where the arm consists of only one switch.

4 System Efficiency Dependence on SiC-MOSFET Current-Rating

In this section, the system efficiency of 50 kW three-phase 2-level grid-tied inverter, of which specifications are listed in Table 1, is analyzed with the several current-rating SiC-MOSFETs using PLECS circuit simulator. The operating point at 25 kW (0.5 p.u.) is considered.

Table 2 lists the efficiency-related parameters of the 1200 V-class SiC-MOSFETs released from ROHM Co., Ltd. Five TO-247 package SiC-MOSFETs and two full SiC power modules with different current-ratings are selected for comparison [12], [14]–[19]. All of them have the gate trench and source trench structures, i.e. all of them are ROHM 3rd generation SiC-MOSFET.

N_{min} means the minimal required number of parallel-connected devices to increase the current capacity of each arm by 1.5 times the rated current of 50 kW inverter.

$R_{DS(on)}$ is the on-resistance of SiC-MOSFET, the related parameter to the conduction loss P_{cond}. On-resistance of each device tend to be smaller as the current-rating of which increases. Note that an actual on-resistance of each arm consisted of plural switches connected in parallel is $R_{DS(on)}/N$.

$P_{sw(Pout=25\ kW)}/f_{sw}$ means the total switching loss energies of the three-phase inverter, of which the device parallel number is N_{min}, at the output power of 25 kW. This parameter is calculated based on the datasheet using PLECS loss analysis. The analysis results confirm that an application of the small-current-rating SiC-MOSFET saves the total switching loss energies due to its fast switching speed. As mentioned in sub-section 2.2, the switching losses are theoretically unchanged in any device parallel number; therefore, the multiple parallel connection of the small-current-rating devices is advantageous for the switching loss reduction.

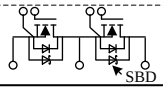
Table. 1: Specification list of 50 kW three-phase grid-tied inverter.

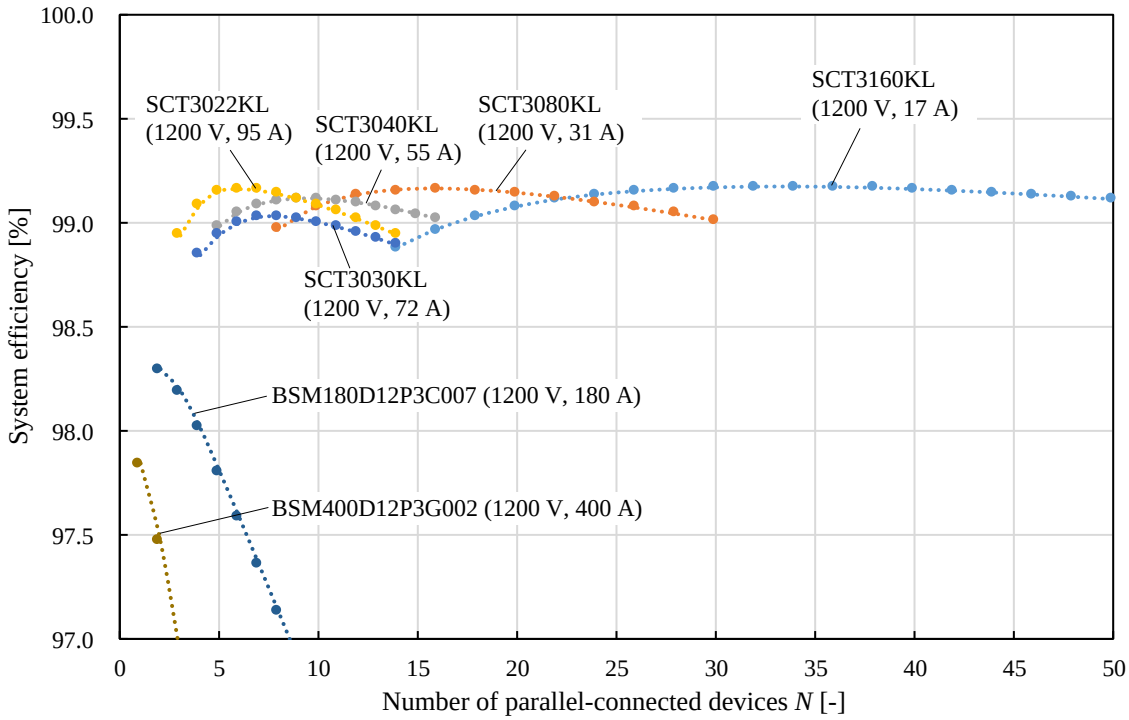
Rated output power	P_n	50 kW
DC-link voltage	V_{dc}	400 V
Line to line voltage	v_{ac}	200 V_{rms}
Power factor	cos φ	0.96
Rated grid current	i_{gn}	150 A_{rms}
Switching frequency	f_{sw}	20 kHz

$C_{ds(Vds=400\ V)}$ is the drain-source parasitic capacitance when the DC-link voltage of 400 V is applied between drain and source, the related parameter to the no-load loss P_{Cds}. In discrete switches which have only the body diode, C_{ds} is almost proportional to the device current-rating. On the other hand, in power modules, the schottky barrier diode is connected in parallel to the SiC-MOSFETs. Therefore, C_{ds} of these power modules is higher than the value which is inferable from the proportional relationship between C_{ds} of SBD-less discrete device and current-rating.

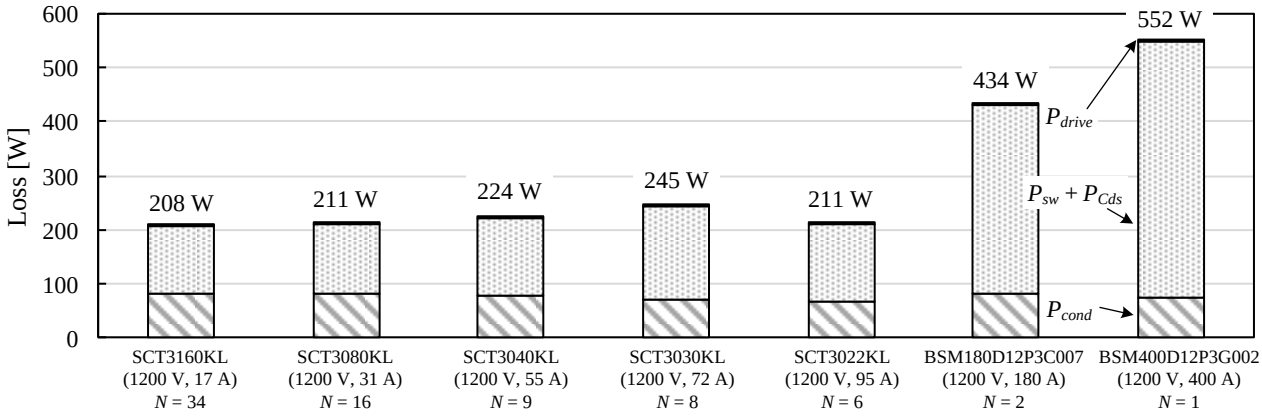
$Q_{g(Vgs=18\ V)}$ is the total gate charge at the gate-source voltage of 18 V, the related parameter to the gate drive loss P_{drive}. As with C_{ds}, Q_g is almost proportional to the current-rating in discrete switches; but this relationship does not hold between discrete switch and power module. This fact indicates that the power module consists of several SiC-MOSFET chips with some current-capacity margin and the chip parallel number is decided with the consideration for the current imbalance due to the chip parameter mismatch and stray component mismatch.

Table. 2: Parameters list of 1200 V-class SiC-MOSFETs released from ROHM Co., Ltd.

SiC-MOSFET	V_{DSS} [V]	I_D [A]	N_{min} [-]	$R_{DS(on)}$ [mΩ]	$P_{sw(Pout=25kW)}/f_{sw}$ [mJ]	$C_{ds(Vds=400V)}$ [pF]	$Q_{g(Vgs=18V)}$ [nC]	Equivalent circuit
SCT3160KL [14]	1200	17	14	160	2.10	23	42	
SCT3080KL [12]	1200	31	8	80	2.46	50	60	
SCT3040KL [15]	1200	55	5	40	3.87	60	102	
SCT3030KL [16]	1200	72	4	30	5.36	90	131	Body diode
SCT3022KL [17]	1200	95	3	22	4.94	119	178	
BSM180D12P3C007 [18]	1200	180	2	10	11.3	790	610	
BSM400D12P3G002 [19]	1200	400	1	4.3	15.7	1730	1100	SBD



(a) System efficiency versus number of parallel-connected devices.



(b) Loss distribution at maximum efficiency point.

Fig. 4: Loss analysis results of 50 kW three-phase VSI with several current-rating SiC-MOSFETs at operating point of 25 kW (0.5 p.u.).

Fig. 4 shows the loss analysis results of the 50 kW three-phase VSI with several current-rating SiC-MOSFETs, listed in table 2. The system efficiency is calculated with the consideration for P_{cond}, P_{sw}, P_{Cds}, and P_{drive}. Fig. 4(a) confirms that the system efficiency improves as the number of parallel-connected devices is increased from N_{min}; then, the efficiency worsens after exceeding a certain parallel number in the case of discrete switches. This characteristic is attributed to the fact that the increased amount of the no-load loss and gate drive loss becomes higher than the decreased amount of the conduction loss when N exceeds the certain parallel number. On the other hand, the system efficiency does not improve even when the parallel number is increased from N_{min} in the case of power modules, of which no-load loss and gate drive loss are inherently large. In addition, Fig. 4(a) confirms that the higher maximum system efficiency can be obtained with the SiC-MOSFETs whose current-rating is small. In particular, the efficiency can be improved at most when the 34 switches whose current-rating is the minimum between the candidates (SCT3160KL) are

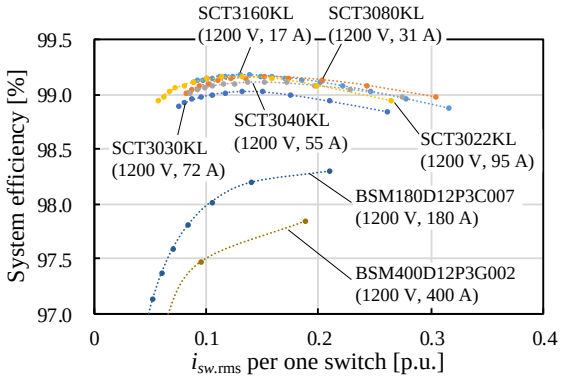
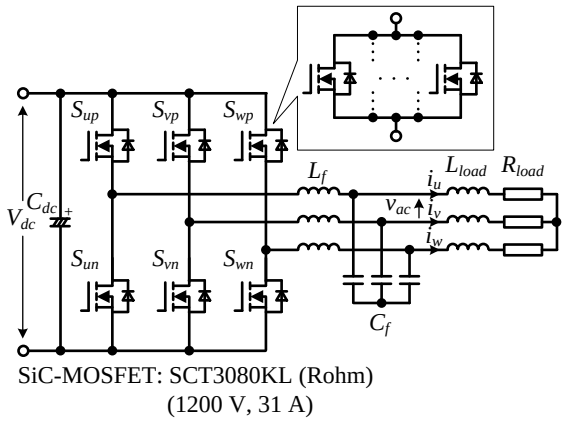


Fig. 5: System efficiency versus normalized rms current value per one switch.



SiC-MOSFET: SCT3080KL (Rohm)
(1200 V, 31 A)

Fig. 6: 2 kW three-phase VSI with LC filter.

Table. 3: Experimental conditions.

Rated output power	P_n	2 kW
DC-link voltage	V_{dc}	400 V
Line to line voltage	v_{ac}	200 V_{rms}
DC-link Capacitor	C_{dc}	680 µF
Filter inductor (%Z)	L_f	3 mH (3.1%)
Filter capacitor (%Y)	C_f	2.2 µF (1.4%)
Load Power factor	cos φ	0.96
Number of parallel-connected devices	N	1, 2, 4
Switching frequency	f_{sw}	10, 20 kHz
Dead-time	t_d	0.5 µs

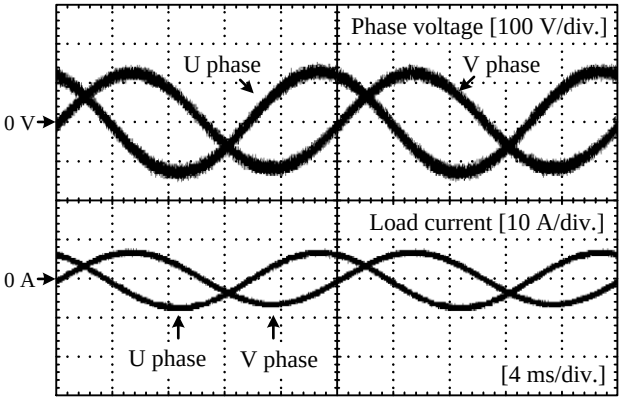


Fig. 7: VSI operating waveforms at N = 4, f_{sw} = 20 kHz.

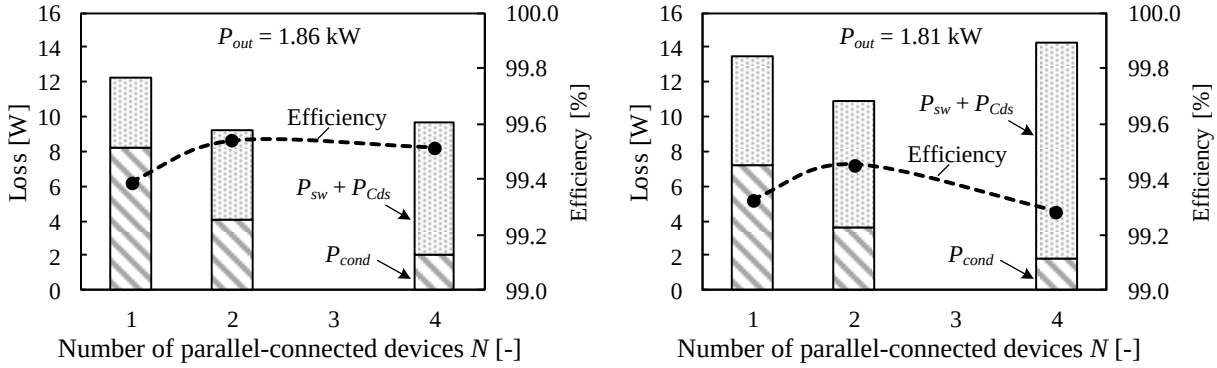
connected in parallel. Fig. 4(b) confirms that the conduction losses P_{cond} at the maximum efficiency points are almost equal at around 100 W regardless of the current-rating of the applied SiC-MOSFET. This fact indicates that a high on-resistance, which is a disadvantage of a small-current-rating SiC-MOSFET, is conquerable by increasing the parallel number and equivalently increasing the chip area. Furthermore, Fig. 4(b) confirms that the gate drive loss P_{drive} are almost equal at around 3 W regardless of the current-rating. Therefore, P_{drive} does not degrade the system efficiency even if the small-current-rating SiC-MOSFETs are driven by multiple parallel connections because these total gate charges are sufficiently small. As a conclusion, the design of the converters in the configuration with the multiple small-current-rating parallel-connected SiC-MOSFETs, whose switching speed is faster than those of the large-current-rating SiC-MOSFETs, is suitable for pushing up the system efficiency.

Fig. 5 shows the relationship between the analyzed system efficiency and the rms current value per one switch. The horizontal axis means the flowing current rms value per one switch which is normalized by the maximum drain current rating of each switch. This results confirm that the optimal drain current derating pushes up the system efficiency. In particular, about 85% drain current derating is the optimal for the high efficiency.

5 Experimental Verification of Optimized Number of Parallel-Connected Devices

Fig. 6 shows the experimental setup of the 2 kW three-phase VSI with the LC filter and the RL-load. The experimental conditions are listed in Table 3. The three-phase VSI system efficiency is measured using Yokogawa WT 1800 power analyzer with regard to N of 1, 2, 4 and f_{sw} of 10 kHz, 20 kHz. The VSI is driven by the triangular-carrier comparison PWM with the sinusoidal modulating signals whose modulation index of 0.86 and the fundamental frequency of 50 Hz.

Fig. 7 shows the VSI operating waveforms at the number of parallel-connected device of 4 and the



(a) f_{sw} = 10 kHz. (b) f_{sw} = 20 kHz.

Fig. 8: Measured inverter losses and system efficiency versus number of parallel-connected SiC-MOSFETs against different switching frequency.

switching frequency of 20 kHz. Similar waveforms are observed even when the number of parallel-connected devices and the switching frequency are changed.

Fig. 8 shows the relationship between the measured VSI losses, efficiency, and the number of parallel-connected SiC-MOSFETs against different switching frequency. In the case of f_{sw} = 10 kHz shown in Fig. 8(a), the conduction loss decreases in inverse proportion to the number of parallel-connected devices. In contrast, the sum of the switching loss and no-load loss increases with large number of parallel-connected devices because the equivalent drain-source parasitic capacitance becomes large. In particular, in the comparison between N = 2 and 4, a decrease in the conduction loss and an increase in the no-load loss are almost same, leading to the almost same system efficiency level. On the other hand, in the case of f_{sw} = 20 kHz shown in Fig. 8(b), the increased amount of the sum of the switching loss and no-load loss by increasing N becomes larger than the case of f_{sw} = 10 kHz. As a result, the maximum system efficiency is obtained at N = 2. These results confirm that it is necessary to determine the number of parallel-connected SiC-MOSFETs with the consideration of both the conduction loss and the no-load loss in order to achieve the higher system efficiency.

6 Conclusion

This paper clarified the relationships between losses of the parallel-connected SiC-MOSFETs applied in the power converters and the number of parallel-connected number. In addition, the relationship between the required cooler performance and the number of parallel-connected devices was also clarified. Then, the system efficiency and the power device losses of 50 kW three-phase grid-tied inverter were calculated with several SiC-MOSFETs whose current-ratings are different. These calculation results confirmed that the multiple small-current-rating parallel-connected SiC-MOSFETs achieve the low switching losses and are advantageous for the high system efficiency. Lastly, the 2 kW three-phase VSI system efficiency was measured with regard to the different number of parallel-connected devices and the switching frequency. This experimental results confirmed that the theory of relationships between losses of the parallel-connected SiC-MOSFETs and the parallel number was correct, and the optimal number of parallel-connected SiC-MOSFETs which led to the smallest total device losses existed. Based on these works, the design guideline for the converter configuration to achieve high-efficiency was clarified.

In an actual system, the multiple parallel-connection of SiC-MOSFETs leads to some challenging problems such as the complexity of the circuit wiring patterns, the mismatches of the circuit stray components, and the current imbalance between the parallel-connected devices. Therefore, countermeasures against these problems are necessary, and will be considered as the future work.

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