Converter Loss Evaluation of Flyback Converter Applying Power Decoupling Capability with ZVS operation

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Abstract

In this paper, the converter loss analysis of a fly-back converter with an active power decoupling capability is discussed. The proposed fly-back converter achieves the double-line frequency power ripple compensation using small capacitor without the additional components and the complicate control. Furthermore, the fly-back converter is operated under the Zero Voltage Switching (ZVS) by the quasi-resonance (QR) control based on the Boundary Current Mode (BCM). In this paper, the converter loss analysis of the proposed converter focusing on the conduction loss is demonstrated by the mathematical formula. As an experimental result, the constant input power is obtained by small DC-link capacitor of 30 μF when the output power is the 300 W. In addition, the 96.0% of the maximum efficiency is obtained including fly-back converter and the voltage source inverter. Finally, it is confirmed that the calculation value of the conduction loss is approximately matched to the simulation result.

1. Introduction

Recently, a photovoltaic systems (PVs) are actively researched as a sustainable power solution due to the attractive characteristics such as; flexibility, high-system efficiency, and low manufacturing cost. The utilization of the micro-inverters promisingly become a trend for the future PV system instead of using large capacity inverters [1]-[4]. In particular, the micro-inverter with the high reliability is required because a large number of converter units are adopted to the PV generation system. However, in the conventional PV system, the electrolytic capacitors are usually employed owing to the requirement of the large capacitance. These capacitor limits the life-time of the converter, which results in low reliability.

In the converter topologies for the micro-inverter, the fly-back converter has been studying for following advantages; (i) Simple configuration and low manufacture cost, (ii) galvanic isolation, (iii) high voltage boost-up, and (IV) small volume. In this case, the configuration with the fly-back converter and the unfolding bridge is the center of attention because the unfolding bridge is switched at the line-frequency and the switching loss can be reduced drastically in comparison with that of two-stage isolated DC/AC converter.

However, the large electrolytic capacitor is required in order to compensate the double-line frequency power ripple owing to single-phase AC grid. As a result, the life-time of the converter is limited due to the large buffer capacitor, which results in low reliability.

In order to solve this problem, the active power decoupling topologies for electrolytic capacitor-less converters have been researched actively [5]-[6]. The active power decoupling can reduce the capacitance for the double-line frequency power ripple compensation, which enables to use of film or ceramic capacitors instead of the electrolytic capacitor. However, the additional components such as the switching device and the passive components are required. Although the low cost is the one of the advantages of the fly-back micro-inverter, these components increase complexity of the circuit configuration and the cost.

The authors have been proposed fly-back converter applying active power decoupling capability without additional components and complicate control [7]. However, the detail of the loss analysis does not considered on previous study.

In this paper, the conduction loss of the low voltage side MOSFETs are clarified mathematically. Furthermore, the new power decoupling method to ensure compatibility with the Quasi-Resonance control (QR control) is proposed in order to improve the conversion efficiency.

This paper is organized as follows; first, the configuration of the conventional micro-inverter with fly-back converter is explained. Next, the proposed converter and a control block diagram are described. After that, the operation mode of the fly-back converter is considered focus on the power decoupling. In addition, the conduction losses of the fly-back converter is considered based on the loss expression. Finally, the experimental result and are demonstrated in order to confirm the validity of the proposed power decoupling control.

2. Conventional fly-back micro-inverter topology

Figure 1 shows the typical configuration for the micro-inverter topology with a fly-back converter. The primary side switch is switched at the high frequency in order to reduce the volume of the transformer. In this control, the duty command is adjusted to obtain the full-wave rectification waveform in synchronized with the grid voltage. After that, the secondary switches are switched at the half cycle of the grid frequency.

Strong advantages of this configuration is a small number of the main circuit components. However, the bulky electrolytic capacitor C_{buf} is necessary on the primary side of the transformer because the double-line frequency power ripple comes from the single-phase AC grid.

Figure 2 shows the fly-back converter with the conventional active power decoupling circuit [8]. In order to reduce the capacitance of C_{buf}, the small buffer capacitor C_{apd} and the auxiliary circuit are added on the transformer secondary side. In this case, the C_{apd} is charged and discharged in synchronized with the double-line frequency power ripple. As a result, the DC side capacitor C_{buf} becomes small. However, these additional components complex the circuit configuration. In addition, the manufacturing cost will be increased by the additional component for active power decoupling.

3. Proposed converter and control method

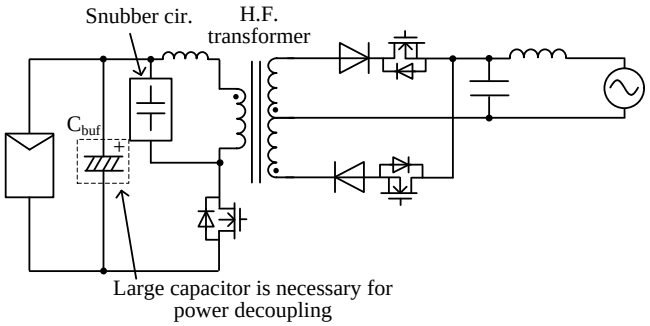


Fig. 1: Typical configuration of micro inverter.

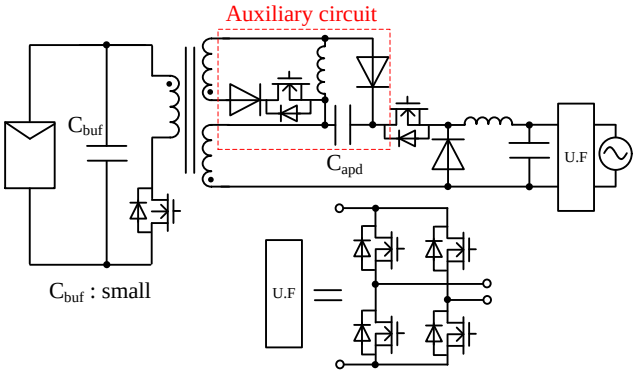


Fig. 2: Fly-back converter with conventional active power decoupling circuit.

3.1 Proposed converter

Figure 3 shows the proposed converter which consists of the fly-back converter, synchronous rectifier, and the voltage source inverter (VSI) and the small buffer capacitor C_{buf}. The fly-back converter isolates between the PV and the single-phase grid, and boosts the input voltage. After that, PV panel is connected to the single-phase grid by the VSI. In the proposed converter, the double-line frequency power ripple is compensated by the C_{buf}, and the additional components such as the switching device and the passive components does not require in order to achieve the power decoupling.

In the proposed converter, the active clamp circuit is applied in order to reduce the snubber loss. The leakage energy of the transformer is absorbed by the small snubber capacitor C_{clamp}. The clamp switch S_{clamp} is operated under the ZVS condition because the parasitic capacitor of S_{clamp} is discharged during the dead time between the main switch S_1 and S_{clamp}. S_{clamp} and the Synchronous rectifier S_{rec} are switched during the discharge of the magnetizing current.

3.2 Principle of power decoupling

Figure 4 shows the principle of the power decoupling between the DC and single-phase AC sides. When both the output voltage and current waveforms are sinusoidal, the instantaneous output power p_{out} is expressed as

$$p_{out} = \frac{V_{acp} I_{acp}}{2}(1-\cos 2\omega t) \quad (1)$$

where V_{acp} is the peak voltage, I_{acp} is the peak current, and ω is the angular frequency of the output voltage. From (1), the power ripple that contains double-line frequency of the power grid, appears at DC link.
In order to absorb the power ripple, the instantaneous power p_{buf} should be controlled by

$$p_{buf} = \frac{1}{2} V_{acp} I_{acp} \cos 2\omega t \quad (2)$$

where the polarity of the p_{buf}, is defined as positive when the buffer capacitor C_{buf} discharges. Note that the active power of C_{buf} should be zero. Owing to the power decoupling capability, the input power is matched to the output power. Thus, the relationship between the input and output power is expressed as

$$p_{in} = \frac{1}{2} V_{acp} I_{acp} = V_{PV} I_{PV} \quad (3)$$

3.3 Operation mode of fly-back converter

Figure 5 shows the operation modes of the fly-back converter. The detail of each mode are described in the following.
Mode 1:
In mode 1, the main switch S_1 is turned-on, and the active clamp switch S_{clamp} is remaining off-state. The DC input voltage is applied to the transformer and each energy storage. The magnetizing current linearly increases until the end of the mode 1, and the energy is stored both leakage inductance and magnetizing inductance.

Mode 2: (dead-time):
This mode starts when the main switch S_1 is turned-off. In this mode, the energy of the leakage inductance L_{leak} is transferred to the parasitic capacitor C_{ds_s1}. In this mode, the synchronous rectifier switch S_{rec} and the parallel diode of S_{rec} is remaining off-state. Thus, the primary side composes the series resonance circuit with L_m, L_{leak} and C_{ds_s1}. Note that C_{ds_s1} is very small, and it is charged quickly.

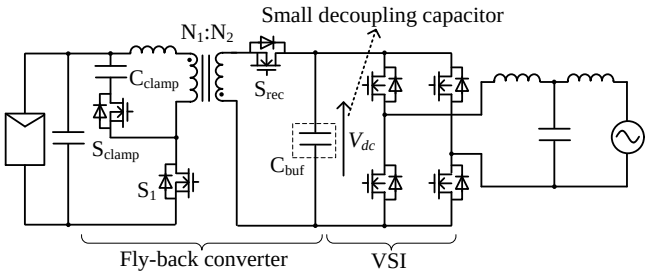


Fig. 3: Proposed fly-back converter. Double-line frequency power ripple is compensated by DC-link capacitor C_{buf}.

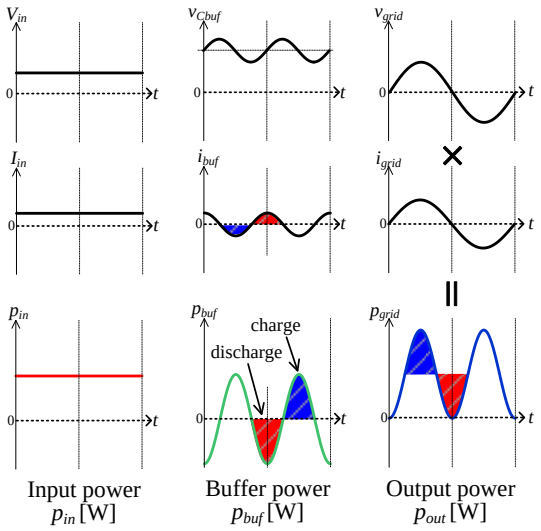


Fig. 4: Principle of power decoupling between DC and single-phase AC.

When the charge of C_{ds_s1} is completed, the free-wheeling diode of S_{clamp} and S_{rec} are turned-on. In this period, the parasitic capacitor of S_{clamp} and S_{rec} are fully discharged.

Mode 3:
This mode starts when S_{rec} and S_{clamp} is turned-on. The period of this interval is set to the energy release period of the magnetizing inductance, and it is expressed as

$$T_{dis} = \frac{N V_{in}}{V_{dc}} T_{on} \quad (4)$$

where I_{peak} is the magnetizing peak current, N is the turn ratio of the transformer, L_m is the magnetizing inductance, and the V_{dc} is the DC link voltage. S_{clamp}

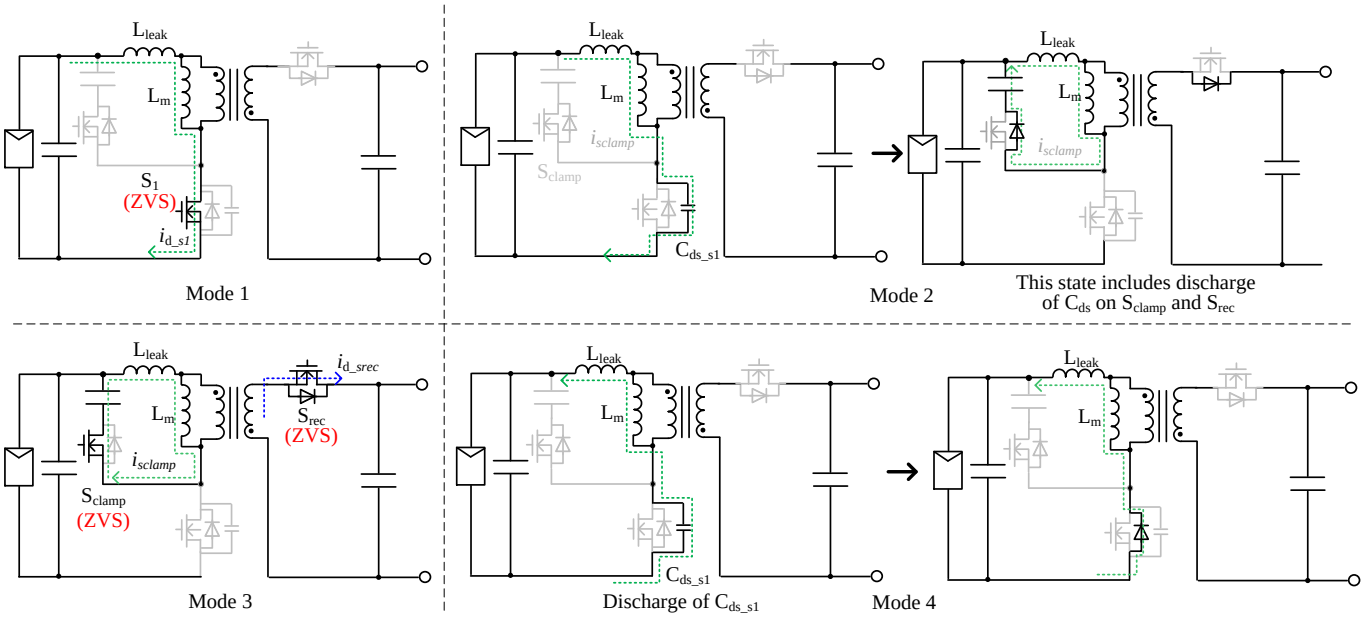


Fig. 5: Operation mode of fly-back converter.

and S_{rec} achieve the ZVS because the parasitic capacitors are already discharged in mode 2.

Mode 4: (dead-time)

In this mode, the parasitic capacitor of S_1 is discharged utilizing the resonance between the magnetizing inductance and the C_{ds_s1}. When the fly-back converter is operated under the discontinuous mode (DCM), the resonance voltage occurs during the zero current period. The QR-control synchronizes the turn-on timing to the resonance voltage by the Pulse Frequency Modulation (PFM). In this case, the C_{ds_s1} is discharged due to the resonance current. As the result, the ZVS is obtained at mode1.

3.4 Power decoupling control

3.4.1 Conventional power decoupling with DCM

In this chapter, the problem of the conventional power decoupling using DCM condition, and the proposed power decoupling control is demonstrated.

Firstly, the average primary current on DCM is expressed as

$$I_{ave\_DCM} = \frac{I_{peak}}{2} D_{on} \tag{5}$$

$$I_{peak} = \frac{V_{in}}{L_m} D_{on} T_{sw} \tag{6}$$

where V_{in} is the PV input voltage, L_m is the magnetizing inductance, D_{on} is the on-duty of S_1, T_{sw} is the switching period. In the DCM operation, the primary average current is decided from the primary side parameter only from (6). Note that, in this power decoupling method, D_{on} and the switching frequency is always set to constant value in order to keep the constant average current. This control method is very simple for the power decoupling operation. However, the conduction losses becomes large in comparison with the CCM and BCM. In addition, the hard switching condition exist due to the resonance voltage during the zero current period. Therefore, it is difficult to keep the high efficiency in the wide load range. The authors proposed the ZVS operation using synchronous rectifier in [8]. However, it is not enough to improve the conversion efficiency because the large current still occurs by DCM.

3.4.2 Proposed power decoupling with QR-control

The QR-operation is the good solution in order to improve the conversion efficiency of the fly-back converter. In this method, the main switch S1 is switched under the ZVS condition using the bottom resonance voltage. In addition, the conduction losses is reduced by BCM. However, the power decoupling capability becomes incompletion due to the DC-link voltage fluctuation.

Figure 6 shows the magnetizing current waveform and the DC link voltage under the Boundary Current Mode (BCM). In the DC to single-phase AC application, the DC-link voltage is fluctuated at the double-line frequency due to the single-phase power ripple when the small DC-link capacitor is installed as shown in Fig.7. The BCM is achieved by the Pulse Frequency Modulation (PFM), and the turned-on timing of the main switch S_1 is synchronized to the neighborhood of the zero of the magnetizing current.

The On-state of the main switch T_{on} is provided directly from the controller, and the peak current of the magnetizing current is obtained from (6).

The average current I_{ave_BCM} is also obtained from (5) and (6). However, the switching period T_{sw} is changed due to the DC-link voltage fluctuation. I_{ave_BCM} is expressed as

$$I_{ave\_BCM} = \frac{V_{in} T_{on}^{\ 2} f_{sw}}{2L_m} \tag{7}$$

where f_{sw} is the switching frequency. Note that, the relationship between T_{on} and the off- state T_{off} have to satisfy following condition under BCM condition

$$f_{sw} = \frac{1}{T_{on} + T_{off}} \tag{8}.$$

Note that, T_{off} is obtained from (4). Finally, I_{ave_BCM} is decided as

$$I_{ave\_BCM} = \frac{V_{in}}{2L_m\left(1 + \frac{NV_{in}}{V_{dc}}\right)} T_{on} \tag{9}.$$

According to (9), I_{ave_BCM} does not become the constant value when the DC-link voltage is fluctuated at the double-line frequency.

Figure 7 shows the control block diagram of the fly-back converter. In this paper, the power decoupling control with QR-operation is proposed. The proposed method adjust the T_{on} to keep the constant average current of I_{ave_BCM}. In order to decide the compensation value for power decoupling, the fluctuation ratio α is defined, and α is expressed as

$$\alpha = \frac{V_{dc\_ave}\left(V_{dc\_det} + NV_{in\_det}\right)}{V_{dc\_det}\left(V_{dc\_ave} + NV_{in\_det}\right)} \tag{10}$$

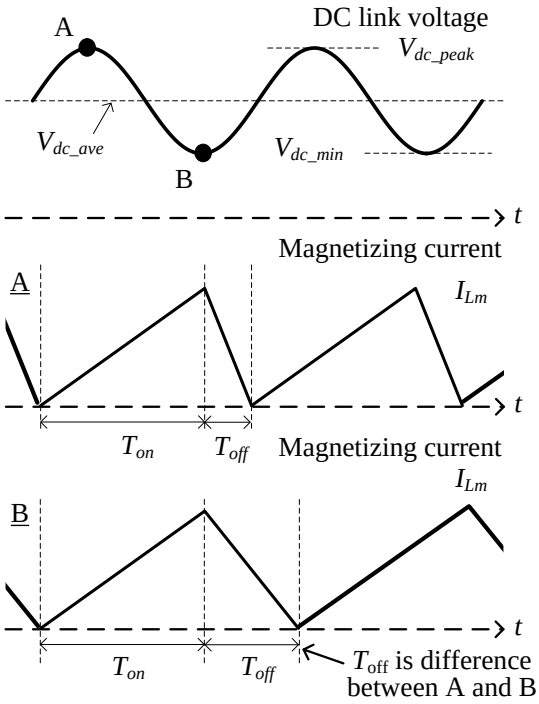


Fig. 6: Waveforms of magnetizing current when DC-link voltage is fluctuated due to the single-phase power ripple.

where V_{dc_ave} is the average voltage of the DC-link voltage, V_{dc_det} is the detection value of V_{dc}, V_{in_det} is the detection value of V_{in}. In the proposed method, T_{on} fluctuates at the double-line frequency to cancel the fluctuation of the I_{ave_BCM}. Finally, the T_{on} with the power decoupling is obtained as

$$T_{on\_decoupling} = \alpha T_{on} \tag{11}.$$

Note that, V_{dc_ave} is used from the voltage command value of the voltage control on the VSI.

The gate signals of active clamp MOSFET S_{clamp} and the synchronous rectifier S_{rec} are generated from the Off-state calculation which means discharge period of the magnetizing inductance. In order to avoid the short circuit between S_1 and S_{clamp}, the turned-on timing is delayed based on the delay time T_{dead}.

The QR-control achieves ZVS using the resonance between the self-inductance and the parasitic capacitor of S_1. The resonance period T_{res} is expressed as

$$T_{res} = 2\pi\sqrt{\left(L_{leak} + L_m\right)C_{ds}} \tag{12}.$$

This resonance states when the S_{clamp} and S_{rec} are turned-off, and the drain-source voltage V_{ds_S1} is decreased. In order to adjust the turned-on timing of S_1 to the bottom of the resonance voltage, turned-on of S_1 is started before the delay time T_{delay}. T_{delay} is set to the half of the resonance period of T_{res}, and it is expressed as

$$T_{delay} \approx \frac{T_{res}}{2} \tag{13}$$

note that the resonance frequency is fluctuated due to the junction temperature condition because the parasitic capacitance depends on the temperature condition.

4. Converter loss calculation

Figure 8 shows the each waveforms of the fly-back converter. The ZVS is the important operation in order to improve the conversion efficiency. The proposed fly-back converter is operated using QR control based on the PFM. The QR control utilizes the resonance between the magnetizing inductance L_m and the parasitic capacitor of S_1 during the zero current period.

The MOSFET of the active clamp S_{clamp} and the S_{rec} are switched during the discharge period of the magnetizing inductance. Note that, both switch are also active ZVS because the drain current is conducted from the source side. That means discharge of the parasitic capacitor of each MOSFETs. Therefore, the all switches of the fly-back converter is switched under the ZVS condition.

In the proposed converter, the loss reduction of the fly-back converter including the transformer is important in order to achieve the high efficiency. In this paper, the conduction losses of the primary side MOSFETs are evaluated by the loss formula because the all MOSFET of the fly-back converter achieves ZVS. Especially, the primary side has the large current due to the low voltage input from the PVs. Each conduction losses are expressed as

$$P_{cond} = R_{on} I_{rms}^{\ 2} \tag{14}$$

where R_{on} is the on-resistor, I_{rms} is the effective current of the MOSFET.

The effective current of S_1 is calculated easily, and the effective current I_{rms_S1} is expressed as

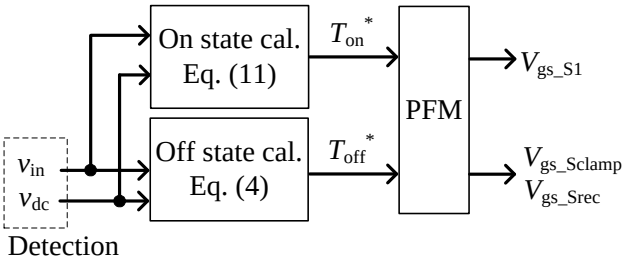


Fig. 7: Control block diagram of fly-back converter.

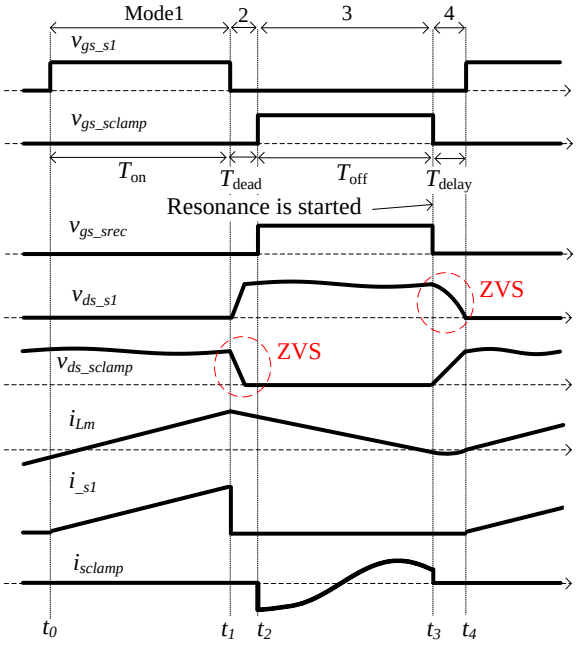


Fig. 8: Key waveforms of fly-back converter. Main switch S_1 achieves ZVS by QR-control. Active clamp switch S_{clamp} and synchronous rectifier S_{rec} also achieve ZVS.

$$I_{rms\_S1} = I_{peak}\sqrt{\frac{D_{on}}{3}} \tag{15}$$

where I_{peak} is the peak current of the magnetizing current, D_{on} is the on duty of S_1. In fact, the initial current should be considered because the small negative current for ZVS occurs before the turned-on of S_1.

The effective current of S_{clamp} is calculated from the LCR equivalent circuit, and the effective current I_{rms_Sclamp} corresponds to the transient current waveform of the LCR circuit. I_{rms_Sclamp} and angular frequency are expressed as

$$i_{Sclamp}(t) =$$

$$e^{-\frac{R_{on}}{2L_{leak}}t}\left\{I_{(t2)}\cos\omega t - \frac{N\left(V_{cclamp(t2)} + 0.5I_{(t2)}R_{on}\right) - V_{dc}}{N\omega L_{leak}}\sin\omega t\right\} \quad (16)$$

$$\omega = \sqrt{\frac{1}{C_{clamp}L_{leak}} - \left(\frac{R_{on}}{2L_{leak}}\right)^2} \quad (17)$$

where $I_{(t2)}$ is initial drain current, $V_{cclamp(t2)}$ is the initial voltage of the clamp capacitor. According to (16) and (17), the I_{rms_Sclamp} is expressed as

$$I_{sclamp\_rms} = \sqrt{\frac{1}{T_{sw}}\int_0^{t3-t2} i_{Sclamp}(t)^2\,dt} \quad (18)$$

Figure 9 and 10 show the calculation result of the conduction loss of S_1 and S_{clamp}. The calculation result and the simulation result are approximately matched within 5% error. The reason of this error is the mismatch of the initial current condition between calculation result and the simulation result. In the calculation result, the bottom value of the magnetizing current is set to zero. On the other hand, in the simulation result, the small negative current occurs due to the QR-operation. In this paper, the parasitic capacitor of S_{rec} does not be considered for simplification. In fact, the initial current of I_{sclamp} is decreased due to the parasitic capacitor current when the synchronous rectifier is applied.

5. Experimental result

Table. 1 shows the experimental parameters. This chapter presents experimental results using 300 W prototype drawn in Figure 3 to confirm the active power decoupling operation. Note that, the DC-link voltage control and inverter output current control are applied to the VSI. The decoupling capacitor is selected to 30μF in order to apply the small film capacitor.

Figure 11 shows the input and output waveforms. According to Figure 11(a), the input current fluctuates at the double-line frequency due to the DC link voltage fluctuation. On the other hand, according to figure 11(b), the Input current is regulated under the constant value by the proposed power decoupling control. In addition, the sinusoidal inverter output current with low THD is obtained.

Figure 12 shows the input current harmonics analysis result. According to Figure12, the second

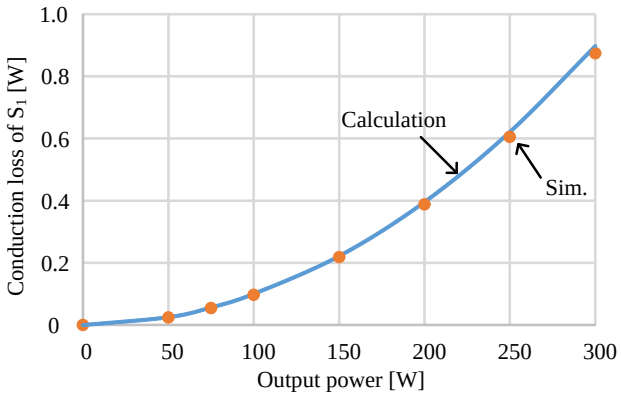


Fig. 9: Conduction loss evaluation result of Main switch S_1.

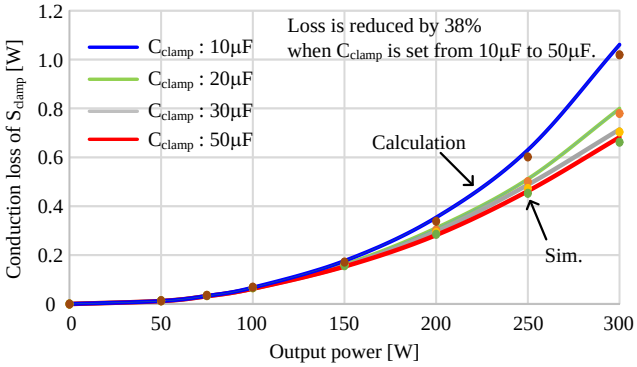
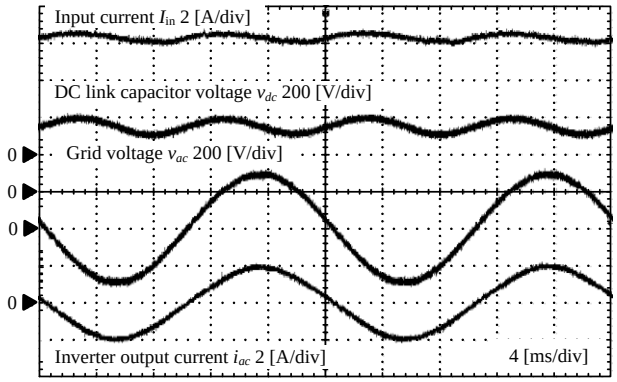


Fig. 10: Conduction loss evaluation result of active clamp switch S_{clamp}.

Table.1: Experimental parameter.

Symbol	Quantity	value
V_{in}	Input voltage	50 V
P_{in}	Input power	300 W
L_m	Magnetizing inductance	11 μH
L_{leak}	Leakage inductance	250 nH
C_{oss}	Parasitic capacitor of S_1	1100 pF
C_{clamp}	Clamp capacitor	20 μF
C_{buf}	Decoupling capacitor (DC link cap.)	30 μF
V_{ac}	Grid voltage	200 V_{rms}
f_{ac}	Grid frequency	50 Hz



(a) Without power decoupling

order harmonics of 100 Hz is reduced by 70.3% by the power decoupling control. From this result, the power decoupling operation with 30μF is confirmed by experiment.

Figure 13 shows the efficiency characteristics of the proposed converter with R-L load. According to Figure 13, the maximum efficiency including the fly-back converter and VSI reach to 96.0% when the output power is 150 W. Especially, the fly-back converter achieves maximum efficiency of 96.8% due to the ZVS operation.

Conclusion

This paper described the power loss analysis of the fly-back converter applying the power decoupling capability and the ZVS operation. As the result, it was confirmed that the error rate between the calculation and the simulation result is less than 5%. From the experimental result, the second order harmonics of 100 Hz is reduced by 70.3% by the proposed power decoupling. Finally, the maximum efficiency including the fly-back converter and VSI reach to 96.0% when the output power is 150 W.

In the future work, the transformer design will be considered in order to improve the conversion efficiency.

Acknowledgment

This study was supported by New Energy and Industrial Technology Development Organization (NEDO) of Japan.

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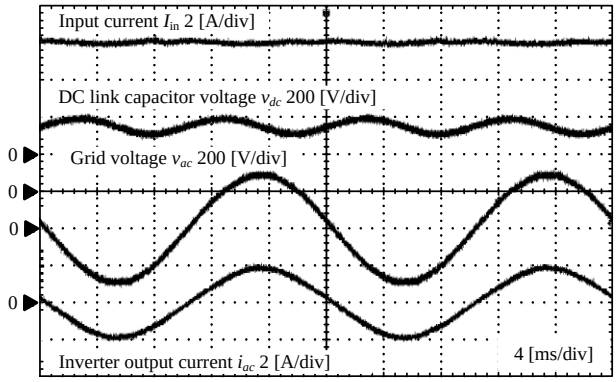

(b) With power decoupling

Fig. 11: Experimental result.

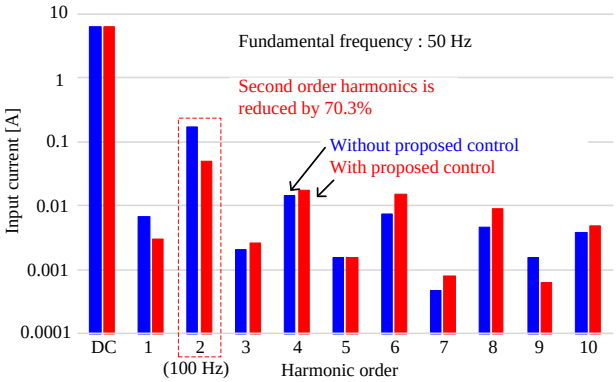

Fig. 12: Harmonic analysis result.

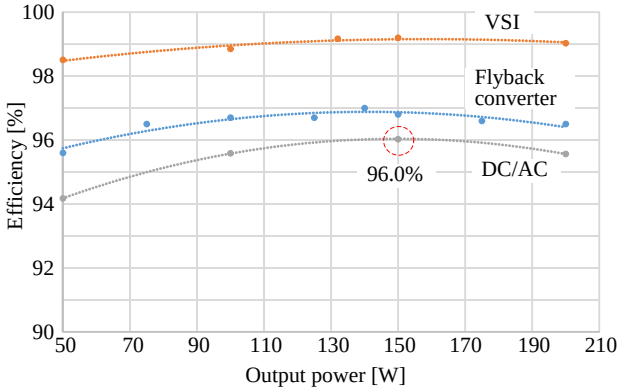

Fig. 13: Efficiency curves with R-L load condition.

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