Loss Analysis of T-type NPC Inverter with Active Power Decoupling Capability Operated in Discontinuous Current Mode

Akiyoshi Omomo, Hoai Nam Le, Keisuke Kusaka and Jun-ichi Itoh
Dept. of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Niigata, Japan
itoh@vos.nagaokaut.ac.jp

***Abstract*—This paper proposes an active power decoupling (APD) method based on discontinuous current mode (DCM) in T-type NPC inverter. The long lifetime is expected because electrolytic capacitors are not required in the system. In addition, the APD control is achieved without any additional inductors. The operation of the APD control is confirmed by the experiment with a prototype. The 100-Hz component of the input current is reduced by 89.1% compared to the result without APD control whereas THD of the output current is 1.81%. Finally, the power loss of the system is theoretically calculated with the calculation and the simulation. The calculated power loss shows the good agreement with the measured loss with an error rate of less than 10%.**

Keywords—DC micro grid, discontinuous current mode, active power decoupling, T-type NPC inverter

I. INTRODUCTION

Nowadays, DC micro grid systems have been actively studied for the effective use of renewable resources and efficient conversion [1–7]. In the initial stage of the DC grid employment, the use of conventional households appliances is expected. However, conventional appliances can be connected to only AC input. Thus, single-phase inverters are required between DC grids and the appliances. In single-phase inverters, the power ripple occurs in their DC-link stage due to the difference in instantaneous power between the input and output power. In order to suppress the power ripple, bulky electrolytic capacitors are generally used in the DC-link stage. However, the employment of the electrolytic capacitors shortens the system lifetime [8–9].

In order to eliminate electrolytic capacitors, the active power decoupling (APD) method which uses only small capacitance, is proposed [10–13]. The system lifetime becomes longer by the employment of long lifetime capacitors e.g., film or ceramic capacitors, instead of electrolytic capacitors. However, the additional circuit is required to control the buffer capacitor voltage. In particular, the additional inductors in the additional circuit restricts the system minimization and efficiency improvement.

So far, the APD method based on discontinuous current mode (DCM) for a T-type NPC inverter has been proposed [14]. As the feature of the method, the additional inductors are not required to control the buffer capacitor voltage. The output current and neutral point current which achieves APD control, are simultaneously controlled by using the time-sharing technology of DCM. In [14], the operation of the proposed method has been confirmed with the experimental result.

In this paper, the system loss characteristics are analyzed to contribute to the optimal circuit design depends on the circuit parameters. In the proposed method, the current flowing to the inverter side and the current flowing to the capacitors, are changed when the DC-capacitors are changed. The power losses on the switching devices and the capacitors regarding the capacitance for APD is analyzed.

II. OPERATION PRINCIPLE

In this section, the simultaneously operation method to achieve output current control and APD control is explained. The output power is expressed as

$$p_{out} = \frac{V_{out} I_{out}}{2}\left(1-\cos 2\omega t\right) \quad (1),$$

where V_{out} and I_{out} are the amplitudes of the output voltage and the current, respectively, and ω is the angular grid frequency. In the case of the single-phase inverters, the output power fluctuates whereas the input power is constant.

Figure 1 shows the principle of the APD method. The power ripple is suppressed by controlling the active buffer power that equals to the difference between the input and output power.

Figure 2 shows the circuit configuration of the T-type NPC inverter. The APD control is achieved by oscillating two capacitor voltages in opposite phases. The two capacitor voltages V_{C1} and V_{C2} are expressed as,

$$V_{C1} = \frac{V_{dc}}{2} + V_m \sin(\omega t + \delta) \quad (2),$$

$$V_{C2} = \frac{V_{dc}}{2} - V_m \sin(\omega t + \delta) \quad (3),$$

where V_{dc} is the DC-link voltage, V_m is the amplitude of the capacitor voltages, δ is the initial phase difference. The capacitor voltages are fluctuated by controlling the capacitor current. The capacitor currents are calculated by,

$$i_{C1} = C\frac{dV_{C1}}{dt} = C\omega V_m \cos(\omega t + \delta) \quad (4),$$

$$i_{C2} = C\frac{dV_{C2}}{dt} = -C\omega V_m \cos(\omega t + \delta) \quad (5).$$

As shown in the above capacitor current equations, the capacitor voltage control is achieved by controlling the neutral-point current i_n. In addition, according to (2)-(5), the active buffer power is expressed as

$$p_C = C\omega {V_m}^2 \sin(\omega t + \delta)\cos(\omega t + \delta)$$
$$= \frac{1}{2} C\omega {V_m}^2 \sin(2\omega t + 2\delta) \quad (6).$$

According to (6), p_C must be the same as the fluctuation component in (1). In (6) and (1), the variable is the sinusoidal function term. Thus, the constant value and the variable are respectively compared. The constant value, which indicates the amplitude, and the fluctuation values, which indicates the phase, are respectively compared in (7)-(8),

$$-\cos(2\omega t) = \sin(2\omega t + 2\delta) \quad (7),$$

$$V_{out} I_{out} = C\omega V_m^{\,2} \quad (8).$$

According to (7), the initial phase difference of the neutral point current δ is calculated. In constant, the amplitude of the capacitor voltage V_m is determined according to (8). Then, V_m is expressed as

$$V_m = \sqrt{\frac{V_{out} I_{out}}{C\omega}} \quad (9).$$

Note that V_m must not exceed the half of the DC-link voltage V_{dc} because the DC-link voltage is the sum of the two capacitor voltages.

According to (4)-(5) and (9), the neutral point current which flows to the neutral point is calculated as

$$i_n = 2\sqrt{V_{out} I_{out} C\omega}\cos\left(\omega t - \frac{\pi}{4}\right) \quad (10).$$

Figure 3 shows the inductor current waveform in one switching period. In case that APD method is employed in inverters, the additional inductors are generally required to control the current of the active buffer. In contrast, the additional inductors are not required in the T-type NPC inverters. The output current and the neutral point current which achieves the APD control, are simultaneously controlled by the output filter inductor. As shown in Fig. 3, the output current is controlled in a very short time in a switching period. The zero current period appears after output current control. The other current which is the neutral point current is controlled in the remained zero current period. Therefore, two current controls do not interfere with each other.

III. Experimental Result

Table I shows the experimental parameters. Generally, the percentage impedance $\%Z_L$ of the grid-tied inductor is designed around 5%. However, as shown in Table I, the output filter inductor of the prototype is 45 μH (the series connection of two 22.5-μH inductors). Therefore, $\%Z_L$ is 0.16%. Furthermore, the additional inductor which is required for conventional power decoupling control is unnecessary.

Figures. 4 (a) and (b) show the waveforms of the output voltage, the output current, inductor current, and the input current with and without the proposed power decoupling method at a 1-kW load, respectively. The output voltage is controlled resulting in the sinusoidal waveform at 50 Hz whereas the fluctuation of the input current is compensated by the proposed method. Total harmonics distortion (THD) of the output current is 1.81%.

Figure 5 shows the harmonic analysis of the input current. According to Fig. 5, by using the proposed method, the fluctuation component of 100 Hz, i.e. twice the grid frequency, is reduced by 89.1% compared to that without the APD method. In addition, any other harmonic components do not exceed 10%.

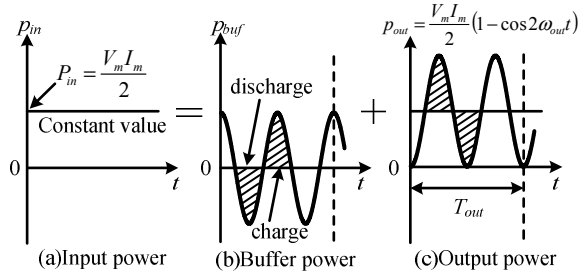


Fig. 1. Principle of power ripple compensation in single-phase DC-AC converter.

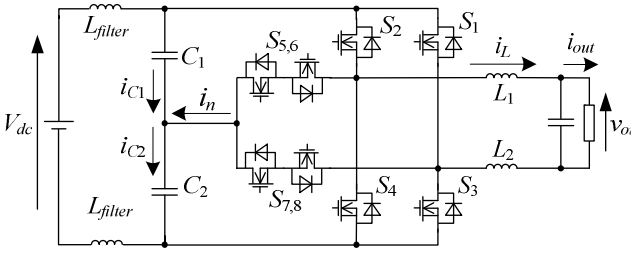


Fig. 2. Single phase T-type NPC inverter. The output current and neutral point current are controlled by only inducotors L_1 and L_2

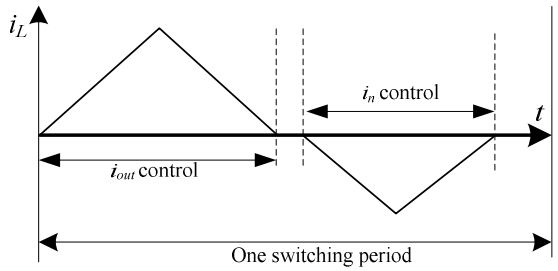


Fig. 3. Waveforms of inductor current. The output current and the neutral point current are simultaneously controlled by one inductor.

TABLE I. SYSTEM PARAMETERS

Parameter	Symbol	Value
Output power	P_{out}	1000 W
Output voltage	v_{ac}	100 V
Output frequency	f_{out}	50 Hz
DC link voltage	V_{dc}	400 V
Capacitor	C_1,C_2	120 μF
Inductor	L_1,L_2	22.5 μH

IV. Loss Analysis

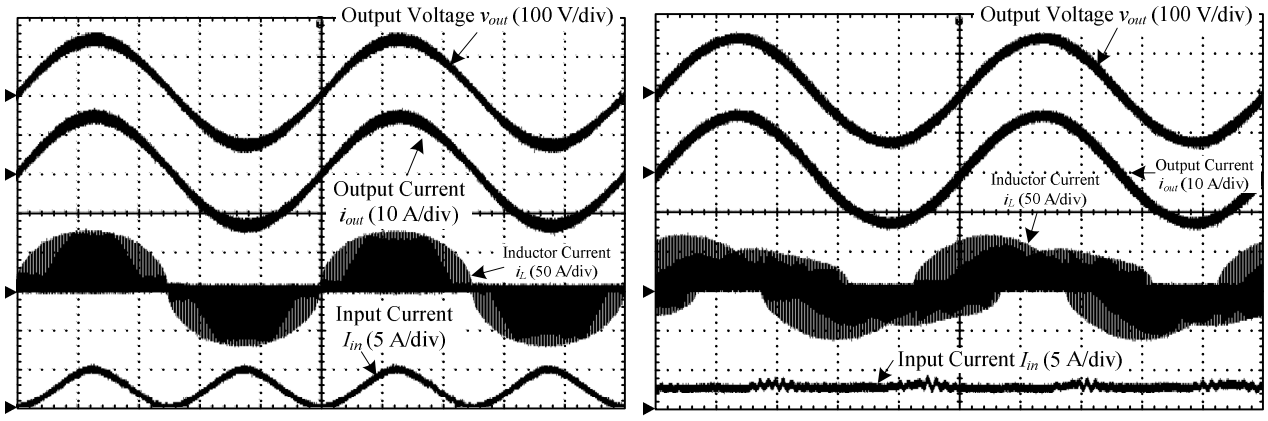
In this section, the loss analysis of the system losses is introduced. The losses in the system can be divided into the conduction losses, the switching losses, and the inductor losses.

The conduction losses of the on-resistance in the switching devices and the ESR of capacitors are calculated by

$$P_{cond} = RI_{RMS}^{\,2} \quad (11).$$

The current which flows to the devices and the capacitors are same as a part of the inductor current. The DCM inductor current is expressed as

$$I_{L\_RMS} = \sqrt{f_{grid}\sum_{m=1}^{4}\sum_{n=1}^{f_{sw}/f_{grid}}\int_0^{T_{sw}d_m}\left(\frac{V_n}{L}t\right)^2 dt} \quad (12),$$



(a) Operation without power decoupling control. (b) Operation with power decoupling control.

Fig. 4. Waveforms of input current, output voltage, output current and inductor current in steady state.

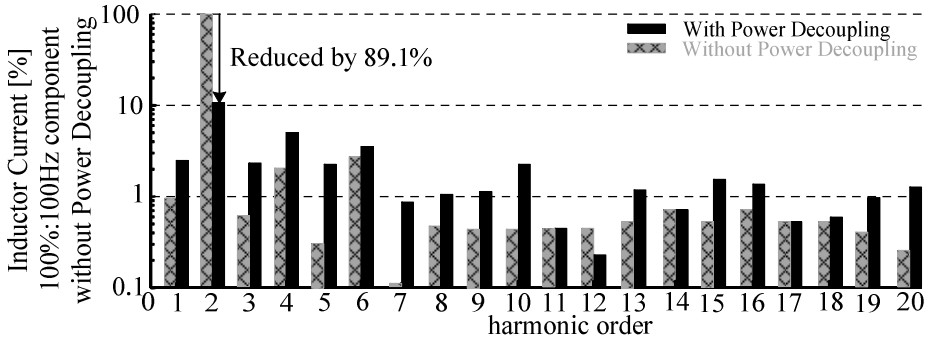


Fig.5 Harmonic components of input current

where f_{grid} is the grid frequency, f_{sw} is the switching frequency, T_{sw} is the switching period, d is the duty of device on time, V_n is the potential difference between both ends of inductors and L is the filter inductor. The summation of the integral terms is the same as the RMS current of the devices and DC-link capacitors, which are determined by the switching patterns. For instance, when the polarity of the output current is positive, the current flows to SW1 in the term during d_1,d_2, Hence, the RMS current of SW1 is calculated as

$$I_{SW1\_RMS} = \sqrt{\frac{f_{grid}}{2}\sum_{m=1}^{2}\sum_{n=1}^{f_{sw}/f_{grid}}\int_0^{T_{sw}d_m}\left(\frac{V_n}{L}t\right)^2 dt} \qquad (13).$$

The other switches and capacitor's RMS current are calculated by the common manner.

The calculation of the switching losses based on DCM is difficult due to its nonlinearity. Thus, in this paper, the circuit simulation software "PLECS" is used to calculate the switching losses. The turn-on and turn-off losses are extracted from a datasheet of the devices that is used in the prototype.

Similarly, the inductor losses in DCM is obtained by the analysis software "Gecko-simulations". The specification of the inductor is based on the inductor which is used in the prototype.

V. Loss Comparison and Capacitance Design

A. Loss comparison

Figure 6 shows the loss comparison result between the calculation and the experimental result. As shown in Fig. 6, the error rate between the calculated loss and the measured loss is less than 10%. Furthermore, it can be observed that the conduction losses of the switching devices and the inductor copper loss dominates a large proportion of the system loss. There, these losses should be focused to be reduced to further improve the efficiency of the system.

B. Capacitance design for highest efficiency

According to (9)-(10), the current flowing to the inverter side i_{inv} is expressed as

$$i_{inv} = V_{out}I_{out}/V_{DC} - \sqrt{\omega C V_{out}I_{out}}\cos(\omega t + \delta) \qquad (14).$$

According to (11), the conduction loss increases when the DC-link capacitor C is increased because the amplitude of i_{inv}, i_{C1}, and i_{C2} are increased. However, the capacitor ESR loss is reduced by paralleling capacitors because the ESR of the capacitors is reduced. In this paper, the relationship between the device loss and the capacitor ESR loss is clarified.

Figure 7 shows the characteristics of the total loss versus the DC-link capacitance. According to (2)-(3), V_m must not surpass the half of DC-link voltage V_{DC}/2. According to (9), Vm is in inverse proportion to $C^{0.5}$ when the rated power is decided. In this paper, the lower limit of the capacitance is designed as 100 μF that V_m is lower than 90% of V_{DC}/2.

The horizontal axis of Fig. 7 shows the parallel number of the capacitors and the capacitance simultaneously. In Fig. 7, the conduction loss dominates the system loss in any cases.

According to (14), the amplitudes of i_{inv}, i_{C1}, and i_{C2} change by changing the capacitance. Thus, the loss reduction is expected by reducing the capacitance. Meanwhile the effect of the capacitance variation on the switching loss is small because the charging and discharging energy of the capacitor is constant. Note that the capacitor loss causes due to its ESR.

The capacitor ESR loss is reduced by paralleling the capacitors due to the reduction of ESR. However, according to (10) and (14), the reduction of the capacitor ESR loss is small because the amplitudes of i_{C1}, and i_{C2} are increased by paralleling capacitors.

Consequently, the relation between the conduction loss and the capacitor loss is a trade-off relation. However, the variation of the conduction loss is dominant in total losses. Therefore, it can be concluded that a small capacitor for the DC-capacitor will decrease the total power loss according to (9) and (14).

VI. Conclusion

This paper presented the APD method for the T-type NPC inverter operated in DCM. The achievement of the APD control without additional magnetic components has been confirmed in the experiment. The calculated system loss is compared to the measured loss. The error rate between the calculated loss and the measured loss is less than 10%. In addition, the total loss of switching devices versus the capacitance of the DC-link capacitors, was analyzed. As a result, the total loss of switching devices was reduced in accordance with the capacitance reduction of the DC-link capacitors. In future work, the efficiency will be further improved.

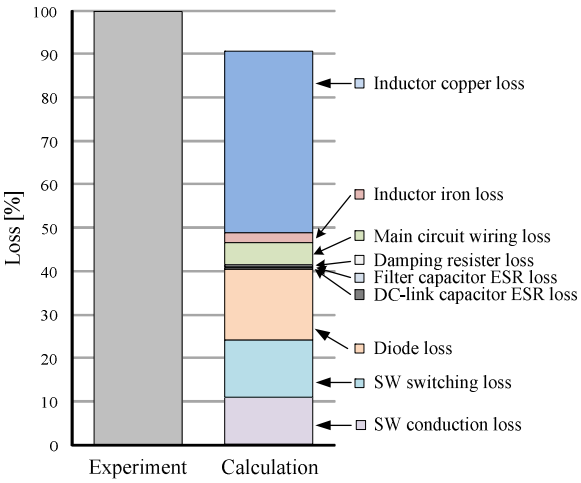


Fig. 6. Loss comparison between experiment and calculation. The error rate between Experiment and calculation is less than 10%.

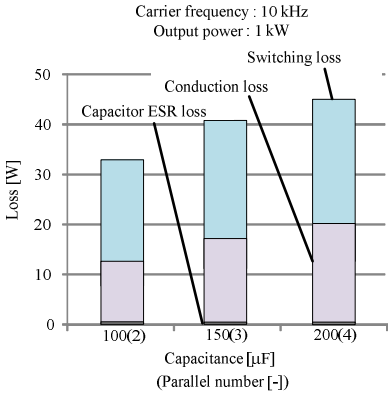


Fig. 7. Loss analysis result. The total loss is reduced in accordance with minimizing *C*.

References

[1] Y. Ito, Z.Yang, and H. Akagi, "DC micro-grid based distribution power generation system", IEEE Int. Power Electron. Motion Control Conf., Vol. 3, pp. 1740–1745 (2004)

[2] X. Lu, J. M. Guerrero, K. Sun, "An Improved Droop Control Method for DC Microgrids Based on Low Bandwidth Communication With DC Bus Voltage Restoration and Enhanced Current Sharing Accuracy", IEEE. Trans Vol. 29, pp. 1800-1812 (2014)

[3] T. Dragičević, J. M. Guerrero, J. C. Vasquez, "Supervisory Control of an Adaptive-Droop Regulated DC Microgrid With Battery Management Capability", IEEE. Trans, Vol. 29, pp. 695-706 (2014)

[4] X. Lu, K sun, J. M. Guerrero, J. C. Vasquez, "State-of-Charge Balance Using Adaptive Droop Control for Distributed Energy Storage Systems in DC Microgrid Applications", IEEE. Trans, Vol. 61, pp. 2804-2815 (2014)

[5] V. Nasirian, S. Moayedi, A. Davoudi, F. L. Lewis, "Distributed Cooperative Control of DC Microgrids", IEEE. Trans Vol. 30, pp. 2288-2303 (2015)

[6] Toru Tanaka, Yoshinori Takahashi, Kenji Natori, and Yukihiko Sato"High-Efficiency Floating Bidirectional Power Flow Controller for Next-Generation DC Power Network," IEEJ J. Industry Applications, vol. 7, no. 1, pp. 29-34, (2018)

[7] Toshiki Nakanishi, and Jun-ichi Itoh,"Control Strategy for Modular Multilevel Converter based on Single-phase Power Factor Correction Converter",IEEJ J. Industry Applications, vol.6, no.1, pp.46-57, (2017)

[8] H. Hu, S. Harb, X. Fang, D. Zhang, Q. Zhang : "A Three-port Flyback for PV Microinverter Applications With Power Pulsation Decoupling Capability", IEEE. Trans, Vol. 27, No. 9, pp. 3953-3964 (2012)

[9] Kodai Abe, Hitoshi Haga, Kiyoshi Ohishi, and Yuki Yokokura,"Current Ripple Suppression Control Based on Prediction of Resonance Cancellation Voltage for Electrolytic-Capacitor-Less Inverter",IEEJ J. Industry Applications, vol.6, no.1, pp.1-11, (2017)

[10] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, P. Wang, "Decoupling of Fluctuating Power in Single-Phase Systems Through a Symmetrical Half-Bridge Circuit", IEEE. Trans, Vol. 30, No. 4, pp.1855-1865 (2015)

[11] H. Hu, S. Harb, N. Kutkut, I. Batarseh, Z. J. Shen : "Power Decoupling Techniques for Micro-inverters in PV Systems — a Review," Energy Conversion Congress and Exposition 2010, pp.3235-3240, pp. 12-16 (2010)

[12] K. H. Chao, P. T. Cheng: "Power Decoupling Methods for single-phase three-poles AC/DC converters", Energy Conversion Congress and Exposition 2009, pp. 3742-3747 (2009)

[13] S.Yamaguchi, T.Shimizu: "Single-phase Power Conditioner with a Buck-boost-type Power Decoupling Circuit", IEEJ Journal of Industry Applications, Vol. 5, No. 3, pp. 191-198 (2016)

[14] A. Omomo, N. Takaoka, H. N. Le, K. Kusaka, J. Itoh, "T-type NPC Inverter with Active Power Decoupling Capability Using Discontinuous Current Mode", IEEE EPE2018, pp. 1-10 (2018)