Voltage Unbalance Compensation Method with Zero Voltage Switching for Series Connected Switching Devices

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Abstract— **This paper proposes a voltage unbalance compensation method of series-connected switching devices for high voltage application such as DC distribution systems. In the series connection, a turn-off voltage unbalance occurs in switching devices due to a parasitic parameter mismatch and a switching timing mismatch among switching devices. In this paper, a capacitor snubber and Zero Voltage Switching (ZVS) operation are utilized to reduce voltage unbalance. In particular, the proposed method reduces the parasitic capacitor (collector-emitter capacitance) mismatch among series-connected devices by a capacitor snubber circuit, whereas the switching losses are effectively reduced by ZVS. As the simulation results, it is confirmed that the collector-emitter voltage unbalance is reduced by 88% by the proposed method in comparison with a snubber-less configuration. Finally, in order to confirm the effectiveness of the proposed method, experiments with a test circuit applied with the proposed method are conducted. According to the experimental results, the voltage unbalance is reduced by 86.0% due to the application of the proposed method.**

***Index Terms*—series connection, high voltage power converter, voltage unbalance, zero voltage switching (ZVS)**

I. INTRODUCTION

Recently, high voltage DC/DC converters have been actively researched for DC distribution systems [1]-[6]. The DC distribution systems have many advantages in comparison with an AC distribution, e.g. low power transmission losses and high compatibility to DC power generation systems such as photovoltaics systems.

In the DC distribution system, isolated bidirectional DC/DC converters are employed in order to connect the DC power generation sources to the DC grid. Hence, these power converters require high voltage rating devices because the DC-bus has a high voltage level more than several kilovolts. Therefore, the switching devices which have high voltage rating are chosen.

On the other hand, wide band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have been developed in order to enhance the performance of the power switching devices [7]. In particular, a high voltage rating switch concept using series-connected SiC-MOSFET has been actively researched for Medium Voltage (MV) or High Voltage (HV) applications [8]-[10]. In this study, a 10 kV-15 kV SiC module which consists of series-connected 1.7 kV SiC-MOSFETs is employed in order to improve the conversion efficiency [11].

Note that a drain-source voltage unbalance has to be considered in the series connection techniques due to the mismatch of parasitic capacitors on each LV-devices [12]-[13]. A RC snubber method is commonly adopted in order to solve this problem. However, the snubber resistor losses worsen conversion efficiency.

In order to avoid the decrease in the conversion efficiency, a voltage unbalance compensation method with a gate timing control method has been proposed [14]-[16]. In this method, the gate signals for series-connected devices are adjusted by digital gate control with a Field Programmable Gate Array (FPGA) and a Digital Signal Processor (DSP). However, it is difficult to identify the parameter mismatch in actual systems because the collector-emitter capacitance and the switching speed depend on the junction temperature condition.

This paper proposes a voltage balance method for the series-connected devices using C snubber and the zero-voltage-switching (ZVS) operation with the Triangular Current Mode (TCM). The snubber capacitance is selected at least five times higher than the parasitic capacitance to reduce the mismatch effect of the parasitic capacitances. Meanwhile, turn-on losses are drastically reduced by the ZVS operation. In addition, the design criteria of the C snubber is introduced in order to compensate the rise timing mismatch of the corrector-emitter voltage on each series connected switching devices. The proposed method has advantages such as simple configuration and low snubber losses in comparison with the conventional voltage balance methods such as the RCD snubber. The originality of this paper is that the voltage unbalance of the series-connected switching devices is compensated by the simple capacitor snubber. In addition, the switching losses are drastically reduced due to the ZVS operation. In this paper, the validity of the proposed method is confirmed by the simulation and fundamental experiments.

This paper is organized as follows; high power and high voltage converter topologies are introduced in section II. Next, the causes of the voltage unbalance of the series-connected devices is explained in section III. In section IV, the proposed voltage balance method for series-connected devices applied C snubber and ZVS operation is presented.

Finally, the effectiveness of the voltage balance method

in the prototype DC/DC converter is confirmed by the simulations and experiments.

II. HIGH POWER AND HIGH VOLTAGE CONVERTER TOPOLOGIES

Fig. 1 shows the circuit configuration of Series Resonance Converter (SRC) for aircraft application [17]. In this system, two HVDC buses are used for power system architecture, and a Solid State Transformer (SST) is utilized for the power link between two HVDC buses.

SRC achieves ZVS and the Zero Current Switching (ZCS) operation utilizing resonance between series capacitor and a leakage inductance to reduce the switching loss. Each DC port is connected to 3.5 kV bus. Therefore, medium-voltage SiC MOSFETs are applied for each switching devices.

Fig. 2 shows the circuit configuration of the multiport isolated DC/DC converter for medium voltage and low voltage DC grids [18]. This converter is utilized for bidirectional interfacing of MVDC and LVDC grid. In this system, SRC is also applied to achieve the galvanic isolation between each DC grid. Note that the SRC is operated by the open loop control, and the switching frequency is set to the resonance frequency for the achievement of the ZVS operation. The power flow during each port is controlled by two DC/DC converter. In this case, the switching devices which have high voltage rating are necessary for port of MVDC grid.

Fig. 3 shows the circuit configuration of the DC/DC converter which consists of the series-connected SiC-MOSFET for high power medium voltage converter such as data center DC distribution [19]. In this circuit as an example, the switching devices with the high voltage rating are required due to high voltage DC input of 20 kV. Generally, IGBT is employed for the switching devices due to its high voltage rating properties. Meanwhile, the DC/DC converter has the requirements such as the reduction of the size and the improvement of the conversion efficiency. In particular, the high-speed switching operation is important to reduce the size of the passive components such as the transformer.

In this system, the series-connected configuration using SiC-MOSFET is utilized in order to satisfy these requirements, and it is the one solution to install the low voltage devices to the high voltage power conversion system such as Fig.1 and Fig.2. However, the voltage unbalance between each series devices is the problem due to mismatch of the parasitic capacitance.

III. VOLTAGE UNBALANCE OF SERIES-CONNECTED DEVICES

Firstly, the drain-source voltage at the turn-off period is expressed as

$$v_{ds} = \frac{1}{C_{ds}} \int i_c(t)\, dt \qquad (1)$$

where v_{ds} is the drain-source voltage, C_{ds} is the parasitic

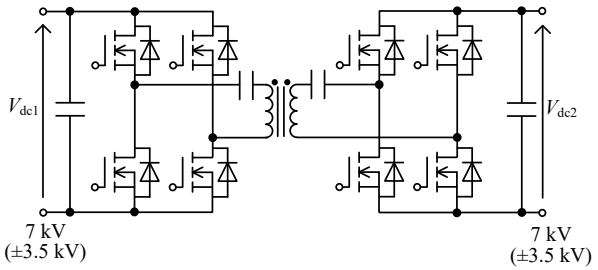


Fig. 1. Circuit configuration of Series Resonant Converter (SRC) for solid state transformer during two HVDC buses [17].

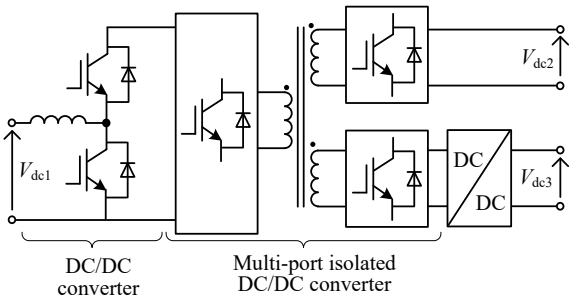


Fig. 2. Circuit configuration of multiport isolated DC/DC converter for medium voltage and low voltage DC grids [18].

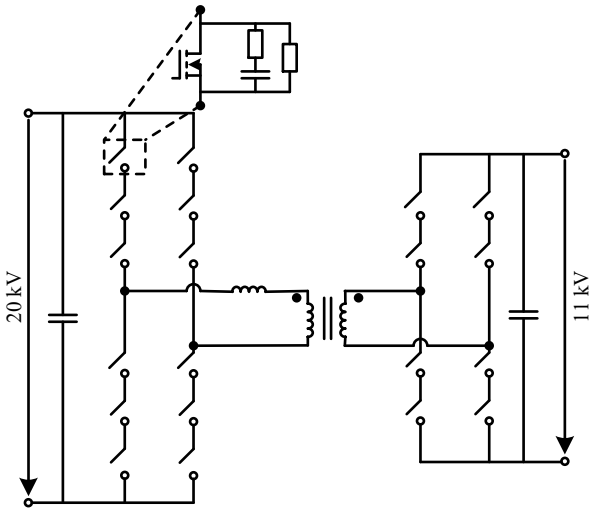


Fig. 3. Circuit configuration of high power converter with series connected technique for high power application [19]. The drain-source voltages of each MOSFET are divided due to the series connection.

capacitance, i_c is the parasitic capacitor current. According to (1), the drain-source voltage depends on the parasitic capacitance. The voltage unbalance occurs due to mismatch of C_{ds} on each series-connected device. In particular, C_{ds} fluctuates dependently on the drain-source voltage condition. Therefore, it is difficult to match the drain-source voltage for each individual device.

The RC snubber is a simple solution to suppress the voltage unbalance. In this method, the snubber capacitor is connected to reduce the mismatch effect of the parasitic capacitances. Note that the snubber capacitance is designed much higher than the parasitic capacitance. In addition, the snubber resistor is applied to suppress the voltage ringing caused by the resonance between the snubber capacitor and the parasitic line inductance. However, the snubber losses are increased due to this snubber resistor.

On the other hand, in the gate timing control method utilizing the digital gate control, the influence of the parameter mismatch which includes the gate-source capacitor and the gate-drain capacitor is analyzed based on mathematical equations. In addition, the gate timing control with the delay gate signal has been considered.

Fig. 4 shows the circuit configuration of the digital gate control [14]. In this method, a gate timing control which uses the FPGA has been proposed. The turn-off voltage unbalance between two series-connected devices is compensated by adjusting the switching timing, and this method has been proven to improve the conversion efficiency in comparison with the RC snubber technique due to the snubber less configuration. However, it is difficult to match the nominal value of the parasitic parameter with the actual value because the parasitic parameter depends on the temperature condition. Especially, the delay gate signal for the voltage balance is given by the parasitic capacitance. As the result, the voltage unbalance remains due to these reasons.

In this paper, the voltage unbalance compensation method with simple solution is introduced in order to solve these problems.

IV. VOLTAGE UNBALANCE COMPENSATION METHOD

A. *Principle of the proposed method*

Fig. 5 shows the DC/DC converter with series-connected switching devices. The proposed method compensates the voltage unbalance by the C snubber and ZVS. Firstly, the parasitic capacitor mismatch is suppressed by introducing the snubber capacitors. The collector-emitter voltage at the turn-off period with the C snubber is expressed as

$$v_{ce} = \frac{1}{C_{ce} + C_{snubber}} \int i_c(t)\,dt \tag{2}$$

where C_{ce} is the parasitic capacitance, $C_{snubber}$ is the snubber capacitance, and i_c is the capacitor current. In this case, each snubber capacitance is designed much higher than the parasitic capacitance.

However, the turn-on switching losses increases when the snubber capacitor is inserted because this capacitor discharges at the turn-on period of the switches. The capacitor current is expressed as

$$i_c = \frac{dv_{ce}}{dt}\left(C_{ce} + C_{snubber}\right) \tag{3}$$

According to (3), i_c increases due to the C snubber. Moreover, the capacitance of the C snubber is much larger than the parasitic capacitance. In this case, the capacitor current flows into the switching device when the switching device is turned on. As a result, the turn-on switching losses increase. Moreover, the current has potential to break the switching device because this discharge current might become higher than the current rating of the switching device. Thus, the connection of the C snubber alone worsens the efficiency and might even break the switching devices.

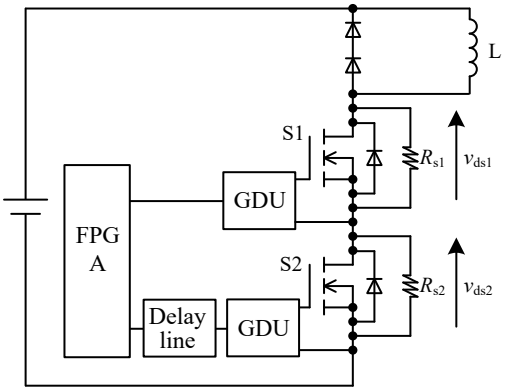


Fig. 4. Circuit configuration of digital gate control [14]. One of the gate driver in switching device has a delay adjustment. The delay adjustment changes the gate timing based on the parasitic parameters.

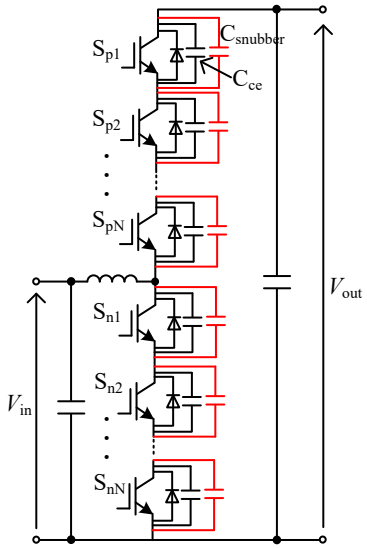


Fig. 5. DC/DC converter with series-connected switching devices. The upper and lower arms are consisted of multiple switching devices which have low voltage rating.

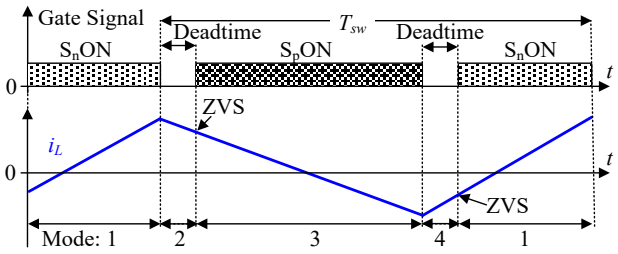


Fig. 6. Switching waveforms of TCM operation. The parasitic capacitor of low side arm is discharged during dead time before turn-on. As a result, ZVS is achieved. In the TCM operation, the current ripple is designed more than the Continuous Current Mode (CCM) to obtain negative current for ZVS.

In order to solve this problem, ZVS is applied to reduce the turn-on switching losses. The charge of the snubber capacitor and the parasitic capacitor is expressed as

$$q = v_{ce}\left(C_{ce} + C_{snubber}\right) \tag{4}$$

where q is the electrical charge. The charge of the snubber capacitor and the parasitic capacitor are delivered back to the DC-link capacitor by the negative current before the turn-on of the switches. As the result, the turn-on losses are drastically reduced because the collector-emitter voltage becomes almost zero thank to ZVS.

Fig.6 shows the switching waveforms of the TCM operation [20]. The TCM operation utilizes the large

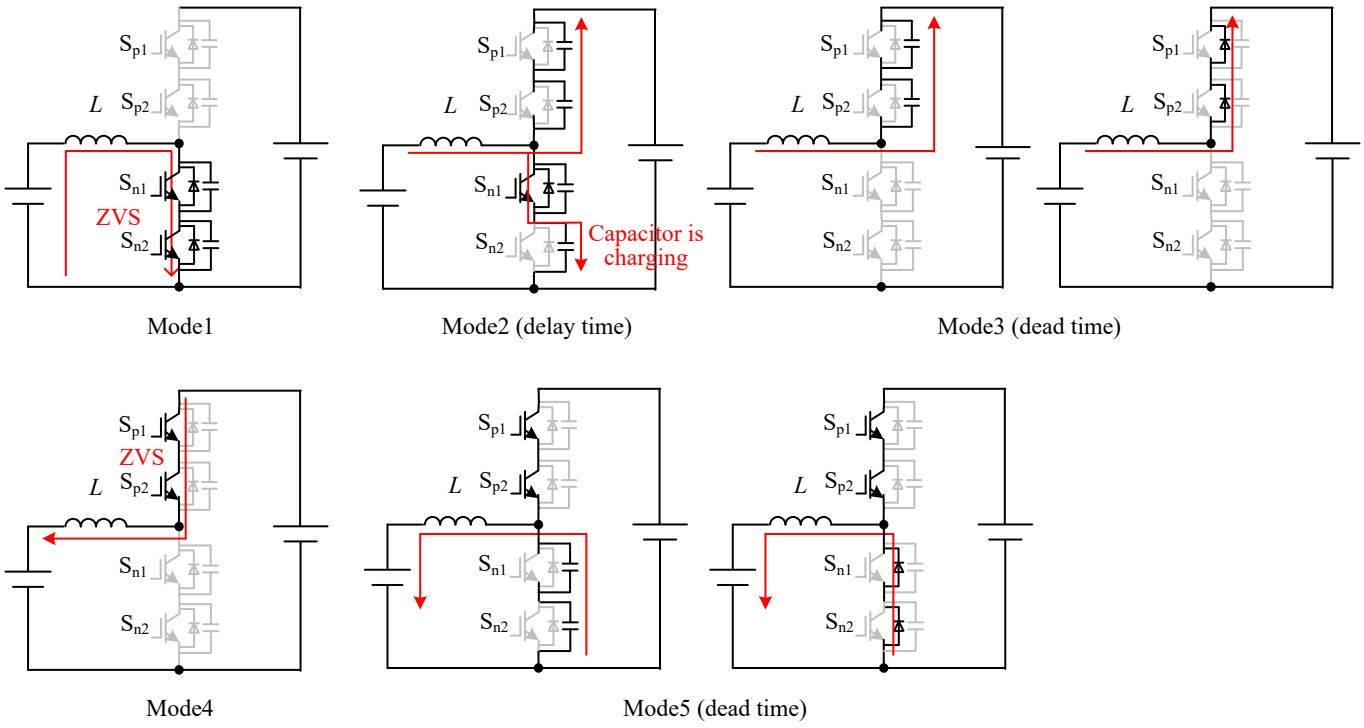


Fig. 7. Operation modes of TCM applies with series connected-switching devices.

current ripple for ZVS; consequently, the parasitic capacitor and the snubber capacitor are discharged during the dead time.

Fig.7 shows the operation mode of the DC/DC converter with the TCM operation. Firstly, the switch S_{n1} and S_{n2} is turned on, and the boost inductor L is charged. In mode 1, S_{n1} and S_{n2} achieves ZVS in turn-on because the discharge of the parasitic capacitor and the snubber capacitor is fully completed during the dead time.

When S_{n2} is turned-off before S_{n1} is turned-off, mode 2 is started. In this mode, the parasitic capacitor and the snubber capacitor of switch S_{p1} and S_{p2} are discharged. Together with S_{p1} and S_{p2} discharging, the S_{n2} capacitor is charged while delay time. It makes voltage unbalance among S_{n1} and S_{n2}.

When S_{n1} is turned-off, mode 3 is started. In this mode, the parasitic capacitor and the snubber capacitor of switch S_{p1} and S_{p2} are continue discharged. After that, the inductor current commutates from the each capacitors to the free-wheeling diode. In mode 4, the S_{p1} and S_{p2} is turned-on at the forward voltage of the free-wheeling diode, which is considered as ZVS. During the mode 4, the inductor current reaches to negative current as shown in Fig.6.

Mode 5 is started when S_{p1} and S_{p2} is turned-off, and the parasitic capacitor and the snubber capacitor are discharged due to the negative current which is obtained from mode 3. As the result, the S_{n1} and S_{n2} achieves turn-on ZVS. According to these operations, the proposed method avoids the occurrence of large turn-on switching losses due to the snubber capacitor employed in each switching devices.

B. Design of snubber capacitor of series-connected switching devices

Fig.8 shows the waveforms of the gate-emitter voltage and the collector-emitter voltage when gate timing mismatch occurs. Note that the black line indicates large parasitic capacitor condition, and v_{signal} is the gate signals from the controller. In actual system, it is difficult to synchronize each gate-emitter voltage although v_{signal} is the same due to the difference of the parasitic capacitance. As the result, the rise timing of the corrector-emitter voltage has delay, leading to the occurrence of the voltage unbalance between each series-connected switching devices.

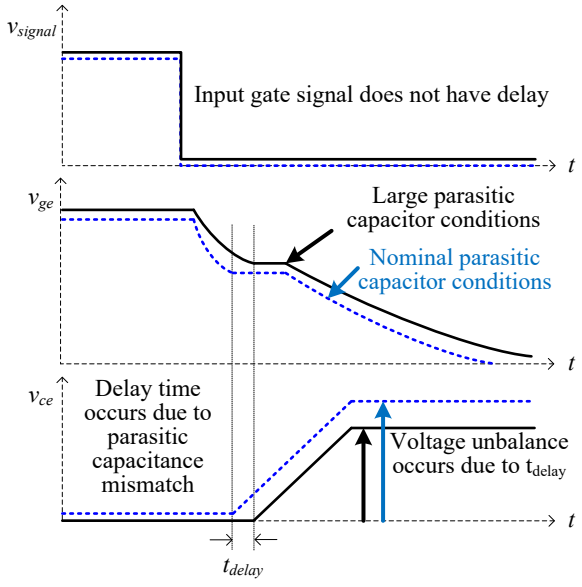


Fig. 8. Waveforms of gate-emitter voltage and corrector-emitter voltage when switching timing mismatch occurs.

In order to avoid this problem, the minimum snubber capacitor has to satisfy

$$C_{snubber} > \frac{i_c * t_{delay}}{\Delta v_{unb}} - C_{ce} \quad (5)$$

where t_{delay} is the period of the delay time among series-connected devices, Δv_{unb} is the voltage unbalance which occurs among series-connected devices. It can be observed from (5) is that C snubber should be infinity to make the

voltage unbalance becomes zero. Thus, the design of the snubber capacitance is according to the required minimum voltage unbalance. Moreover, the C snubber also reduces the influence of the delay time among series-connected devices. Note that, the delay time among series-connected devices should be evaluated to design the C snubber reducing the influence of delay time.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation results of DC/DC converter applied with proposed method

Table.1 shows the parameters for simulations. In order to confirm the validity of the TCM operation in the DC/DC converter, two series-connected devices is used in each arms.

Fig. 9 shows the simulation results of the upper arm in the DC/DC converter with series-connected switching devices. Note that Fig.9 (a) is depicts the waveform when the C snubber is not applied. According to Fig.9 (a), the voltage unbalance of 20.0% occurs due to the parasitic parameter mismatch between C_{CE1} and C_{CE2}. On the other hand, as shown in Fig.9 (b), the voltage unbalance between V_{ce1} and V_{ce2} is suppressed significantly by the C snubber. The upper arm switching devices is confirmed to achieve ZVS without the TCM operation.

Fig. 10 shows the simulation results of the lower arm in the DC/DC converter with the series-connected switching devices. Note that Fig. 10 (a) is depicts the waveforms when the C snubber is not applied, whereas Fig.10 (b) shows the waveforms when the C snubber is applied. The voltage unbalance reduction thanks to the C snubber same as Fig. 9 is confirmed. According to Fig. 10 (a) and (b), the lower arm switching devices also achieves ZVS operation due to the TCM operation.

Fig. 11 shows the simulation results of the lower arm in the DC/DC converter with the delay time. Note that Fig. 11 (a)'s snubber capacitance is 4 nF. It is lower than the designed value of the C snubber. According to Fig. 11 (a), the delay time between S3 and S4 is 5 ns. The turned-off period is different between S3 and S4 caused by the delay time. Consequently, the voltage unbalance occurs between series-connected devices caused by the delay time. On the other hand, in Fig. 11 (b) the snubber capacitance of 8.65 nF is employed. According to the Fig. 11 (b), the slope of collector-emitter voltage is less steep compared with that in Fig. 11 (a). The high snubber capacitance connected to the switching devices between collector and emitter reduces the influence of the delay time among the series-connected devices.

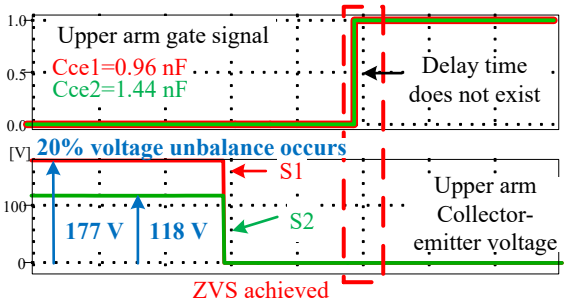
B. Experimental results for effectiveness confirmation of proposed method

Fig. 12 shows the test circuit which employs the proposed voltage balance method. Note that this experiment is conducted for the fundamental evaluation of the proposed method. In addition, IGBTs are installed in this experiment because the voltage unbalance compensation principle is similar between IGBT and SiC-MOSFET.

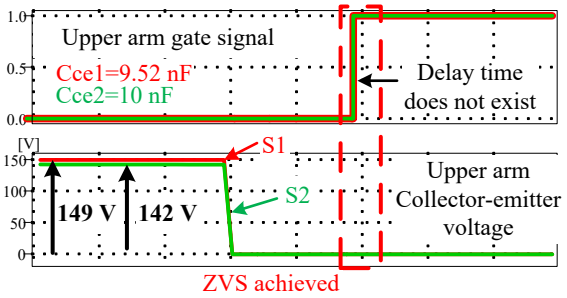
Fig. 13 shows the experimental results of the test circuit. Note that Fig. 13 (a) is not applied the proposed voltage balance method. According to Fig. 13 (a), the voltage unbalance of 29.2% occurs due to the parasitic parameter mismatch. On the other hand, as shown in Fig. 13 (b), the

Table 1 Simulation parameters.

Quantity	Symbol	Value
Input voltage	V_{in}	200 V
Output voltage	V_{out}	300 V
Switching frequency	f_{sw}	20 kHz
boost inductance	L	290 μH
Collector-emitter parasitic capacitance (V_{ce} = 30 V)	C_{ce}	1.2 nF
Mismatch of the Parasitic capacitance	-	20%
Snubber capacitance	$C_{snubber}$	8.65 nF

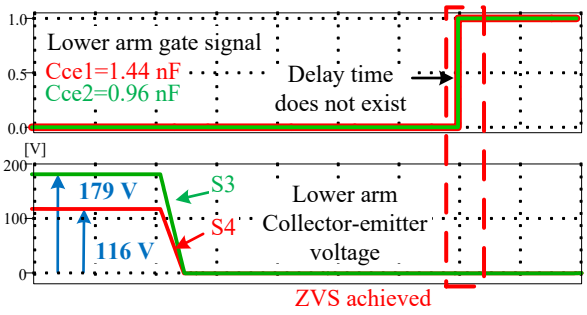


(a) Without C snubber circuit.

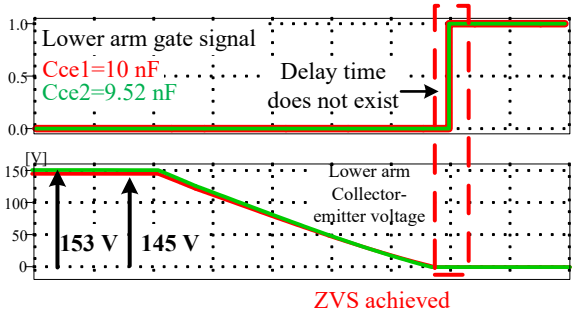


(b) With C snubber circuit

Fig. 9. Simulation results of upper arm in the DC/DC converter applied series connected switching devices when the parasitic capacitance is mismatched.



(a) Without C snubber circuit



(b) With C snubber circuit

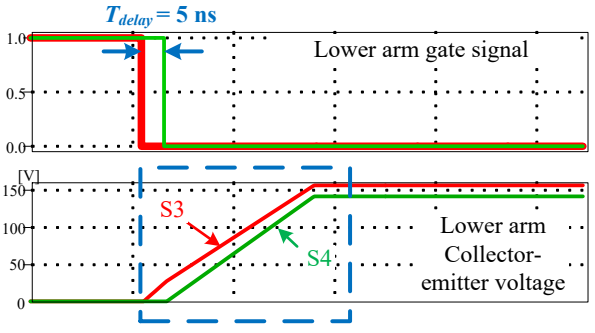
Fig. 10. Simulation results of lower arm in the DC/DC converter applied series connected switching devices when the parasitic capacitance is mismatched.

voltage unbalance between V_{ce1} and V_{ce2} is 4.2%. Thus, the proposed method is confirmed validity by test circuit.

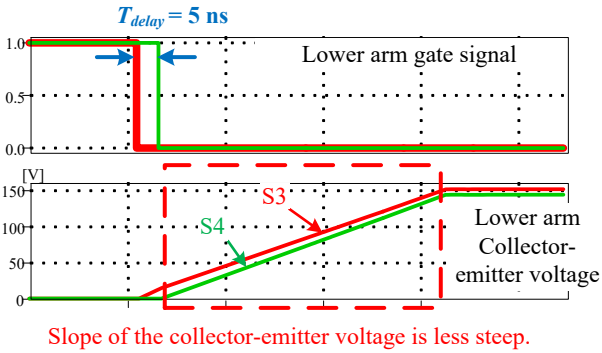
VI. CONCLUSION

In this paper, the voltage balancing method with the C snubber and the ZVS achievement was proposed. The voltage unbalance of the series-connected switching devices was compensated by the simple snubber capacitor circuit. In particular, the switching losses were drastically reduced due to the ZVS operation. The validity of the proposed method was tested by a simulation model. The simulation model was the DC/DC converter with the series-connected switching devices. The circuit is applied with the TCM operation to achieve the ZVS operation in the lower arm switching devices in the DC/DC converter. According to the simulation results, the DC/DC converter simulation model achieved the ZVS operation at the both arms. The application of the C snubber circuit reduced the voltage unbalance caused by the parasitic capacitance of the switching devices. Moreover, the C snubber also reduced the influence of the delay time among the series-connected switching devices. Finally, in order to confirm the effectiveness of the proposed method, the boost converter applied with the proposed method is experimented. According to the experimental result, the voltage unbalance is reduced due to the application of the proposed method.

In the future work, the DC/DC converter and the TCM operation will be conducted in the experiment.



(a) C snubber capacitance of 4 nF



(b) C snubber capacitance of 8.65 nF

Fig. 11. Simulation results of DC / DC converter with and C snubber capacitor when the gate signal has delay time.

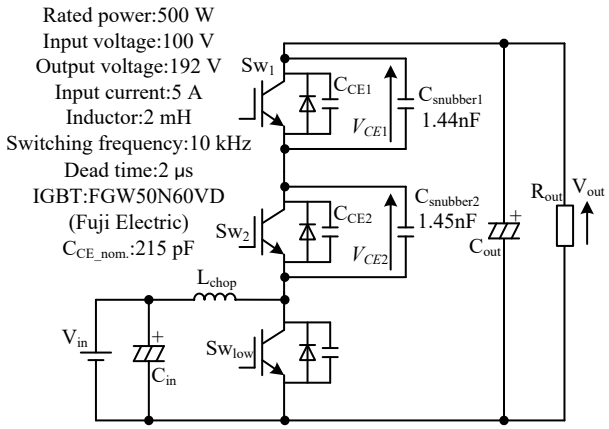


Fig. 12. Test circuit employed with the proposed voltage balance method.

REFERENCES

[1] N. Flourentzou, Agelidis. V, and Demetriades. G, "VSC-Based HVDC Power Transmission Systems: An Overview" IEEE Transactions on Power Electronics, Vol.24, (3), pp.592-602 (2009)

[2] R. T. Naayagi, and S. K. Panda "Fault-tolerant converter for future offshore wind farm HVDC networks" 2017 IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia)

[3] Y. Wang, K. Wang, C. Li, Z. Zheng, and Y. Li, "System-Level Efficiency Evaluation of Isolated DC/DC Converters in Power Electronics Transformers for Medium-Voltage DC Systems" IEEE Access (2019)

[4] Yusuke Hayashi, and Tamotsu Ninomiya, "Highly Scalable Sensorless Multicellular AC-DC Transformer (ADX) for the DC Distribution System in Data Centers" IEEJ J. Industry Applications, vol. 7, no. 6, pp. 479-487, 2018.

[5] Yusuke Hayashi, Yoshikatsu Matsugaki, and Tamotsu Ninomiya, "Capacitively Isolated Multicell Dc-Dc Transformer for Future Dc Distribution System" IEEJ J. Industry Applications, vol. 6, no. 4, pp. 268-277, 2017.

[6] Yue Yu, Keisuke Masumoto, Keiji Wada, and Yuichi Kado, "A DC Power Distribution System in a Data Center using a Triple Active Bridge DC-DC Converter" IEEJ J.Industry Applications, vol. 7,no .3, pp. 202-209, 2018.

[7] S. Dimitrijev, and P. Jamet, "Advances in SiC Power MOSFET technology", Microelectronics Reliability, Vol.43, pp.225-233 (2013)

[8] K. Vechalapu, A. Negi, and S. Bhattacharya "Performance evaluation of series connected 15 kV SiC IGBT devices for MV power conversion systems" 2016 IEEE Energy Conversion Congress and Exposition (ECCE)

[9] S. Ji, T. Lu, Z. Zhao, H. Yu, and F. Wang "Active voltage balancing control for 10kV three-level converter using series-connected HV-IGBTs" 2016 IEEE Applied Power Electronics Conference and Exposition (APEC)

[10] K. Vechalapu, S. Hazra, U. Raheja, A Negi, and S. Bhattacharya "High-speed medium voltage (MV) drive applications enabled by series connection of 1.7 kV SiC MOSFET devices" 2017 IEEE Energy Conversion Congress and Exposition (ECCE)

[11] K. Vechalapu, and S. Bhattacharya "Performance comparison of 10 kV-15 kV high voltage SiC modules and high voltage switch using series connected 1.7 kV LV SiC MOSFET devices" IEEE ECCE 2016 (2016)

[12] Y. Han, W. Chen, X. Chen, X. Ma, Y. Sha, X. Yang, and X. Li "A 4000 V input auxiliary power supply with series connected SiC MOSFETs for MMC-based HVDC system", Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016 IEEE 8th International, pp.279-284 (2016)

[13] L. Wang, D. zhang, and Y. Wang "High performance solid-state switches using series-connected SiC-MOSFETs for high voltage applications", IPEMC-ECCE Asia, 2016 IEEE 8th International, pp.1674-1679 (2016)

[14] K. Shingu, and K. Wada, "Digital control based voltage balancing for series connected SiC MOSFETs under switching operations", in Proc. IEEE Energy Conversion Congress and Exposition, 2017, pp. 5495-5500 (2017)

[15] K.Shingu, and K. Wada, "Voltage Balancing Control for Series Connected MOSFETs Based on Time Delay

Adjustment Under Start-Up and Steady-State Operations " 2018 IEEE Energy Conversion Congress and Exposition (ECCE)

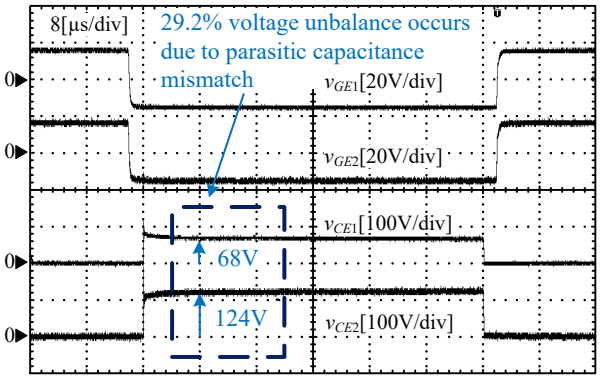
[16] P. Wang, F. Gao, Y. jing, Q. Hao, K. Li, and H. Zhao, "An Integrated Gate Driver with Active Delay Control Method for Series Connected SiC MOSFETs" 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics(COMPEL)

[17] Piotr Czyz, Thomas Guillod, Florian Krismer, and Johann W. Kolar "Exploration of the Design and Performance Space of a High Frequency 166 kW / 10 kV SiC Solid-State Air-Core Transformer" The 2018 International Power Electronics Conference

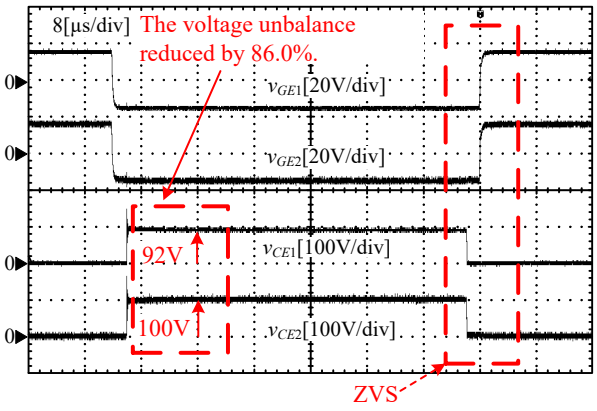
[18] Yan-Kim Tran, and Drazen Dujic, "A multiport medium voltage isolated DC-DC converter" IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society

[19] S. charya, R Chattopadhyay, A. Anurag, S. Rengarajan, Y. Prabowo, and S. Bhattachary, "High Power Medium Voltage 10 kV SiC MOSFET Based Bidirectional Isolated Modular DC-DC Converter", IPEC-ECCE Asia (2018)

[20] Hoai Nam Le, Koji Orikawa, Jun-ichi Itoh "Zero-Voltage Switching for Bidirectional Buck/Boost Converter using Hybrid Discontinuous Current Mode" 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, 2016, pp. 1-8.



(a) Without proposed method



(b) With proposed method

Fig. 13. Experimental results of test circuit for effectiveness confirmation of proposed method.