FRT Operation for Single-Phase Grid-Tied Inverter with Active Power Decoupling Capability

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***Abstract*-- This paper proposes a Fault Ride-Through (FRT) operation for a single-phase grid-tied inverter with an active power decoupling capability. The power decoupling circuit achieves the double-line-frequency power pulsation compensation with a small capacitance; consequently, a transient response with a sudden load change becomes worsen because a large energy buffer, i.e. bulky electrolytic capacitors, does not apply. In particular, high overshoot voltages occur in a DC-link voltage when the grid voltage sag of the single-phase grid occurs, resulting in the interrupt of the FRT operation due to the over voltage protection. In order to solve this problem, the buffer capacitance is designed in the consideration of the overshoot amount of the DC-link voltage. The theoretical value of the overshoot amount is verified with a 1-kW prototype. As an experimental result, The error between the experimental and the calculation value is within 10%. Furthermore, the proposed control achieved both the FRT operation and the active power decoupling capability.**

***Index Terms*—DC-AC Inverters, FRT Operation, Active Power Decoupling,**

I. INTRODUCTION

In recent years, photovoltaics (PV) systems have been actively employed to solve environmental problems such as global warming [1]-[3]. In the PV systems, each PV module is connected to a single-phase grid by a DC to single-phase AC converter which consists of a boost converter and the voltage source inverter (VSI). Furthermore, maximum power point tracking (MPPT) is applied to optimize the power generation efficiency. However, an instantaneous power pulsation due to the single-phase grid fluctuates the PV generated power, which results in low power generation efficiency. Therefore, power decoupling capability is necessary in the DC to single-phase AC converter to guarantee instantaneous power pulsation.

A passive power decoupling method with large electrolytic capacitors is a typical solution. However, a life time of the electrolytic capacitors depends on the environmental temperature according to Arrhenius equation. As a result, system reliability is limited due to the electrolytic capacitors. On the other hand, active power decoupling methods such as DC active filters have been researched to solve the life-time problem [4]-[13]. In these methods, the single-phase power pulsation is compensated by a small capacitance, leading to the application of film or ceramic capacitors instead of the bulky electrolytic capacitors. As the result, the converter reliability is no longer restricted by the life time of the electrolytic capacitors.

Meanwhile, with the expansion of the PV systems, local grid voltage sag might occur when several PVs are disconnected from the grid, which might lead to a widespread loss of generation. In order to prevent this problem, a Fault Ride-Through (FRT) capability is required to continue the power converter operation during the grid voltage sag [13]-[24]. However, in the power converter employing the active power decoupling capability, high overshoot and undershoot voltages occur in a DC-link voltage during the grid voltage sag due to the lack of a large energy buffer, i.e. a large capacitance. Overshoot might trigger over voltage protection, and undershoot distorts the input / output current during the DC-link voltage falls below the grid voltage. Therefore overshoot and undershoot voltages might interrupt the FRT operation. Reference [13] proposes an FRT operation with an active power decoupling scheme. However, the amount of the DC-link voltage overshoot has not been considered during the voltage sag. In addition, in the other papers, the DC-link voltage overshoot in worst condition at voltage sag is not sufficiently studied with the power pulsation and the small capacitance of the DC-link.

In this paper, a control method of the FRT operation with the small energy buffer is proposed. First, the principles of following contents are shown in section II; (1) mechanism of the power pulsation compensation, (2) reduction of the capacitance for the buffer capacitance with the active power decoupling method, (3) the design method of the steady state buffer capacitance. Second, the DC-link voltage overshoot amount at the voltage sag is obtained by converting the transfer function of the control block. Moreover, the overshoot amount is shown by using an approximate equation. The DC-link capacitance is designed under the condition that the DC-link capacitance is limited by considering the DC-link voltage overshoot at the voltage sag. Finally, the FRT operation of the grid-tied inverters with the small capacitance is confirmed by experiments. The experiments are conducted with the grid connection of 100 V or 200 V. The experimental results

show that the DC link voltage value follows the command value even during the voltage sag. Furthermore, the output power recovers after the grid-voltage recovery as before the voltage sag. Therefore, the grid-tied inverter with the small buffer capacitance is possible to achieve the FRT operation in the worst condition of the voltage sag. By using the theoretical value with the approximate equation, the error with experimental value is less than 10%.

II. Circuit configuration and active power decoupling method

A. Circuit method

Fig. 1 (a) shows the circuit configuration which consists of the active power decoupling circuit based on the boost converter and the VSI. The active power decoupling circuit achieves the power decoupling operation by the small capacitance C_{buf}. Therefore, the single-phase power pulsation is compensated by a small capacitance, leading to the application of film or ceramic capacitors instead of the bulky electrolytic capacitors. In addition, this circuit is also utilized for a boost-up operation of a PV input voltage. Consequently, the proposed circuit does not require additional components such as an inductor for the power decoupling capability.

B. Operation principle

Fig. 1 (b) shows the relationship between the input power, the instantaneous output power, and the compensation power of the energy buffer in the active power decoupling circuit. Firstly, the instantaneous output power P_{out} when the output voltage and current are sinusoidal waveforms is expressed as

$$P_{out} = \frac{V_{out} I_{out}}{2}(1 - \cos 2\omega t) \tag{1}$$

where V_{out} is the peak grid voltage, I_{out} is the peak output current, and ω is the angular frequency of the grid. According to (1), the single-phase instantaneous power pulsation occurs at twice the frequency of the grid frequency. Moreover, the input power P_{in} is expressed as

$$P_{in} = \frac{1}{2} V_{out} I_{out} = V_{in} I_{in} \tag{2}$$

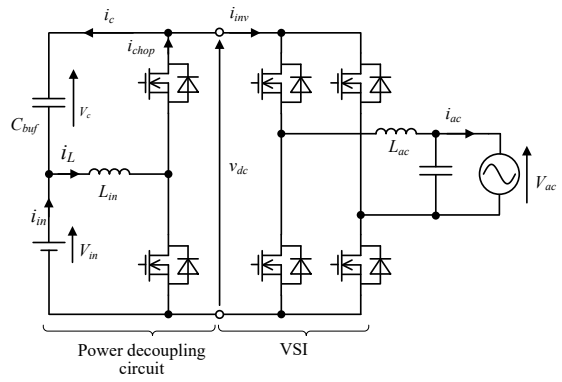
where V_{in} is the DC input voltage, and I_{in} is the DC input current. In order to keep the input power constant, i.e. the instantaneous power P_{in}, the frequency component of the second term in (1) is actively compensated by the buffer capacitor. Therefore, the instantaneous power P_{buf} of the buffer capacitor is controlled by

$$P_{buf} = -\frac{1}{2} V_{out} I_{out} \cos(2\omega t) \tag{3}.$$

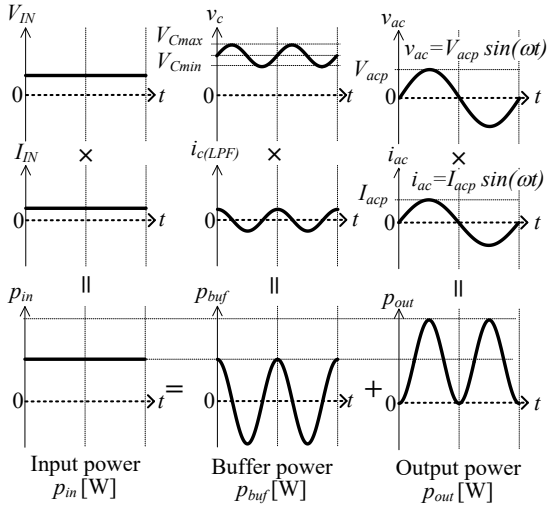
The active power decoupling circuit charges and discharges the differential power between the input and output power. In addition, the charging or discharging energy of the buffer capacitor E is expressed as

$$E = \frac{1}{2} C_{buf} \Delta V^2 \tag{4}$$

where C_{buf} is the buffer capacitance, and ΔV is the buffer capacitor voltage peak to peak value. According to (4), the compensation energy in DC-link capacitor is achieved by



(a) Grid-tied inverer with power decoupling circuit



(b) Principle of power decoupling

Fig. 1. Grid-tied inverter with active power decoupling circuit and principle of power decoupling. The circuit consists of typical boost converter and small buffer capacitance C_{buf}. This circuit does not need additional components for the power decoupling. According to Fig.1 (b), the differential power between the input and output power is compensated by small capacitance C_{buf}.

increasing the buffer capacitance C_{buf} as in the passive power decoupling method. On the other hand, the active power decoupling circuit actively charges and discharges the buffer capacitor to control the buffer energy, which implies ΔV is increased instead of increasing C_{buf}. Note that, the compensation power for the power pulsation W_c is expressed as follows

$$W_C = \frac{1}{2} V_{out} I_{out} \int_{-\frac{\pi}{4\omega}}^{\frac{\pi}{4\omega}} \cos(2\omega t)\, dt = \frac{V_{out} I_{out}}{2\omega} = \frac{p_{out}}{\omega} \tag{5}.$$

In addition, the capacitor power is obtained from the capacitance and the buffer capacitor voltage and expressed as

$$W_C = \frac{1}{2} C_{buf} V_{C\max}{}^2 - \frac{1}{2} C_{buf} V_{C\min}{}^2 \tag{6}$$

where V_{Cmax} and V_{Cmin} are the maximum and minimum values of the allowable voltage fluctuation, respectively. The required capacitance is calculated from (5) and (6), and expressed as

$$C_{buf} = \frac{2W_C}{V_{C\max}{}^2 - V_{C\min}{}^2} \quad (7).$$

According to (7), the capacitance of the buffer capacitor is possible to decrease as the fluctuation of the DC-link voltage increases. However, the design of C_{buf} in (7) is a design value for a steady-state operation. Therefore, the load fluctuation and the voltage sag operation are not considered in (7). The design method considering the transient phenomenon is described in the next chapter.

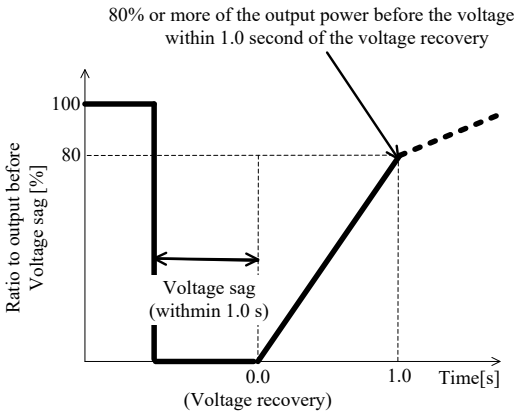
III. Control Method and Challenges of FRT Operation

A. FRT requirement in grid interconnection

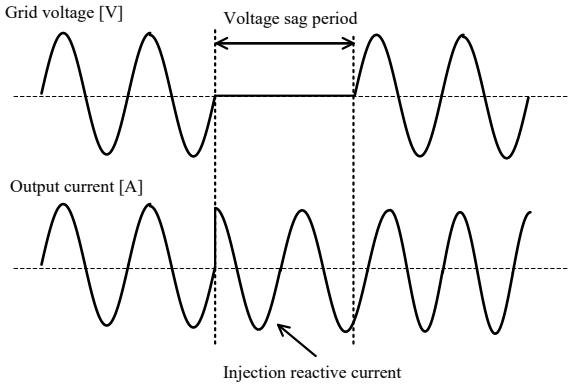
A power converter in a photovoltaic system might halt operation when voltage sag occurs or at the voltage recovery. Therefore, FRT operation controls the voltage and frequency fluctuation during the grid voltage recovery and supports the recovery of the output power.

Fig. 2 (a) shows the operation of FRT at the momentary voltage drop. In Japan, the FRT operation after the voltage recovery is required that the output power is recovered to 80% of the output power before the occurrence of the voltage sag. Furthermore, the output power recovery must be within one second after the voltage recovery. Table I shows the FRT requirements of several country including Japan. The FRT requirements are different in each country.

There are countries in Europe having the FRT requirements that is required to inject the reactive current during the voltage sag. Fig. 2 (b) shows an FRT operation in which a reactive current is injected to the grid side during voltage sag. The reactive current is injected to assist the grid voltage recovery. After the grid voltage recovery, the inverter output power is recovered by gradually switching from the reactive current to the active current.



(a) FRT requirements in Japan



(b) Operation of the voltage sag period

Fig. 2. FRT operation for grid-tied inverter.

B. Challenges of FRT operation with active power decoupling capability

In general, the DC-link voltage control is employed in the VSI control, whereas the input current control is applied in the boost converter to achieve MPPT. Consequently, the DC-link voltage control bandwidth is designed to low to avoid the interference of the power pulsation frequency; hence, the high overshoot and undershoot voltage in DC link when the sudden load change might occur due to the DC-link capacitance minimization thank to the active power decoupling capability.

Fig. 3 shows the simulation results of the FRT operation with the active power decoupling capability in the ideal condition. Note that the active current becomes zero, whereas the reactive current is provided from the VSI

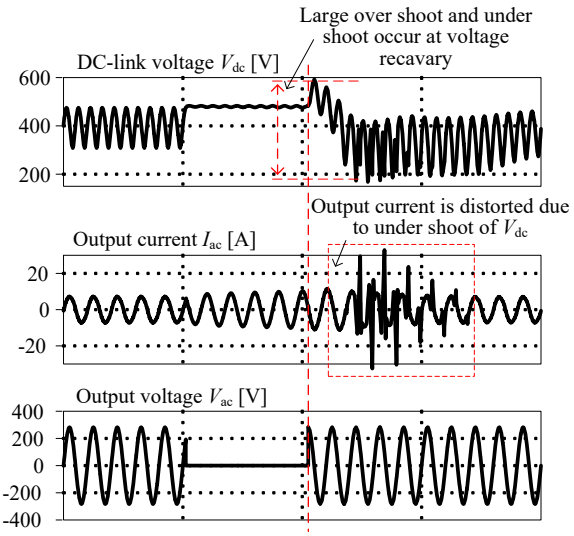


Fig. 3. FRT operation with small DC-link capacitance when DC-voltage control is applied to VSI control. High overshoot and undershoot occur at the grid voltage recovery. As the result, the output current distorts due to undershoot of V_{dc}.

Table I. FRT requirements.

country	Voltage drops down	Voltage sag time	Voltage or output power recovery time
Japan	0 %	1000 ms	80% more than the output power within 1.0 s
Germany	0 %	150 ms	90% more than the grid-voltage within 1.5 s
British	0 %	140 ms	90% more than the output Power within 1.0 s
America	20 %	625 ms	90% more than the grid voltage within 3.0 s

or PV during the grid voltage sag. As shown in Fig. 3, the grid-tied inverter operates stably before the grid voltage sag. However, the output current distorts when the DC link voltage undershoots less than the instantaneous grid voltage after the grid voltage recovery. Therefore, the DC-link voltage minimum value is requried to keep higher than the grid-voltage-peak value at the grid voltage drop and recovery. In the active power decoupling method, the DC-link capacitance is reduced by largely varying the DC-link voltage; this leads to a large overshoot and undershoot occurring at the voltage drop and recovery. Therefore, design of the buffer capacitance is necessary to consider not only the steady state operation but also the voltage sag operation.

C. Control method

Fig. 4 shows the proposed control block diagram of the proposed circuit. In this paper, the DC-link voltage control is performed on the VSI side or the power decoupling side respectively. In the former, the DC-link voltage control is employed in the VSI circuit together with the output current i_{out} control. In the later, the DC-link voltage control is employed in the power decoupling circuit together with the input current i_{in} control. Note that the power decoupling control is achieved by feeding forward the capacitor current reference at the output of the DC-link voltage control. The charge and discharge current for the buffer capacitor is expressed as

$$i_c = \frac{P_{out}}{v_c}\cos(2\omega t) \tag{8}$$

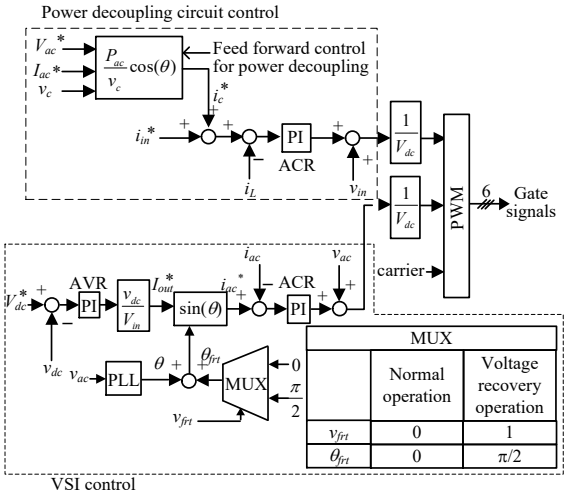
where i_c is the feed forward current to achieve the power decoupling. The VSI control is composed of the phase synchronization with the phase locked loop (PLL) control, and the output current i_{ac} control. The phase of the output current advances 90 degrees during the grid voltage sag. The difference between the DC-link voltage control employed in the VSI side and that employed in the power decoupling side is that the power supply source for the DC-link is from the grid voltage or the solar cell voltage. The DC-link voltage control employed in the VSI side cannot maintain the DC-link voltage during the voltage sag because there is no power supply source for the DC-link capacitor. Therefore, in order to control the DC-link voltage during the voltage sag, the DC-link voltage control is employed in the power decoupling side to supply the power from the solar cell to the DC-link capacitor.

D. Detection method of voltage sag

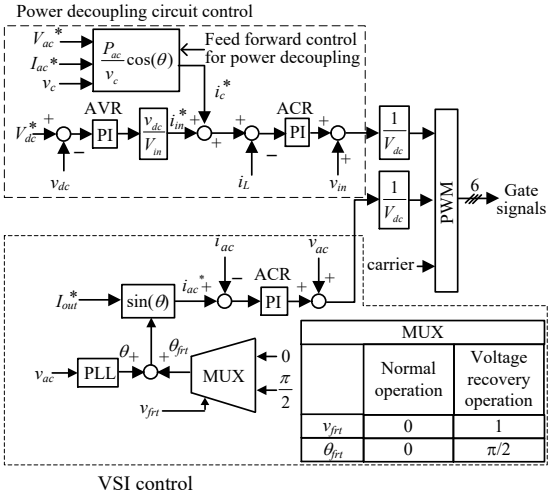
Fig.5 shows the voltage-sag detection method is achieved by detecting the grid voltage and using the High-pass filter (HPF) on the control side. The grid voltage v_{ac} is defined as $v_{ac}\sin\theta$. Moreover, Differential of $v_{ac}\sin\theta$ which is $v_{ac}\cos\theta$ is derived by the grid voltage and HPF. The magnitude of the grid voltage v_{ac} can be expressed as

$$\sqrt{v_{ac}^2\sin\theta + v_{ac}^2\cos\theta} = v_{ac} \tag{9}.$$

HPF differentiates the grid voltage. According equation (9), the magnitude of the grid voltage is constant regardless of the phase of the grid voltage. The grid voltage drops to 0 V due to the voltage sag, resulting the value of equation (9) becoming zero. The detection of the voltage sag is realized by comparing the grid voltage with the threshold value. However, the use of HPF causes a detection delay time. In order to reduce the delay time, it is necessary to raise the cutoff frequency of the HPF. However, the detection error of the instantaneous drop occurs due to the high cutoff frequency. The cutoff frequency of HPF is designed to be ten times compared to the grid frequency.



(a) AVR with grid-tied inverter



(b) AVR with power decoupling circuit

Fig. 4. Control block diagram of proposed circuit. The feedforward control and the DC-link voltage control are applied to the power decoupling circuit control to achieve both FRT operation and the power decoupling operation.

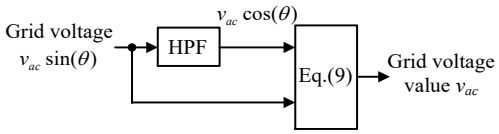


Fig. 5. Voltage-sag detection method.

IV. CONSIDERATION OF DC-LINK VOLTAGE OVERSHOOT AT VOLTAGE SAG

In a power decoupling circuit, the amount of the DC-link voltage overshoot at the voltage sag depends on the load fluctuation. The DC-link voltage overshoot is caused by fluctuations in the buffer capacitor current i_c and the inverter input current i_{inv} due to the load fluctuation. Therefore, the overshoot of the DC-link voltage is determined by the disturbance response such as the buffer capacitor current and the inverter current.

Fig. 5 (a) shows the control block diagram of the power decoupling side. In this control block, the Auto current regulator (ACR) response is much higher than the auto voltage regulator (AVR) response. Thus, the ACR gain is set to 1.0. K_{pv} and T_v of the proportional-integral (PI) controller for AVR are expressed by the following equations.

$$K_{pv} = 2\xi\omega_{nv}C \tag{10}$$

$$T_V = \frac{2\xi}{\omega_{nv}} \tag{11}$$

where ζ is the damping coefficient, and ω_{nv} is the angular frequency of the voltage controller.

Fig. 5 (b) shows the disturbance-transfer-function model from the inverter current to DC-link voltage in Fig. 5 (a). The disturbance transfer function of the inverter input current i_{inv} is expressed as

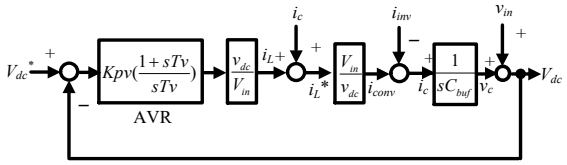
$$G_{load\_i_{inv}}(s) = \frac{-\frac{1}{C}s}{s^2 + 2\xi\omega_{nv}s + \omega_{nv}^2} \tag{12},$$

where s is the Laplace operator. Similarly, the disturbance transfer function due to the buffer capacitor current i_c expressed by (13)

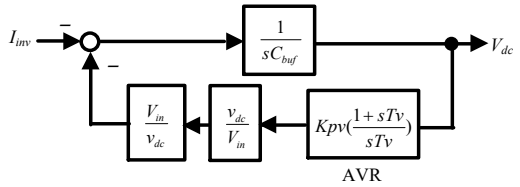
$$G_{load\_i_c}(s) = \frac{-\frac{1}{C}\frac{V_{in}}{v_{dc}}s}{s^2 + 2\xi\omega_{nv}s + \omega_{nv}^2} \tag{13}.$$

Fig. 6 (a) shows the controller on the power decoupling side including the inverter-output-current controller. The disturbances in the power decoupling controller occur due to the output current i_{ac} fluctuation at the voltage sag.

Fig. 6 (b) shows the disturbance-transfer-function model from the inverter current to DC-link voltage in Fig. 6 (a). Generally, an overshoot amount due to the disturbance is obtained by the transfer function from a step response or a ramp response of disturbance with Laplace transform and inverse Laplace transform. The transfer functions of ACR and AVR are second-order systems. Therefore, the disturbance transfer function of AVR including ACR is a fourth-order system. The transfer function of the fourth order system is converted to the time domain by inverse Laplace transform. However, formalizing the amount of overshoot requires complicated calculations in the forth-order transfer function. Therefore, the overshoot of the DC-link voltage is derived by an approximate equation. The elements required to derive the overshoot of the DC-link voltage are the variation of the output power P_{out}, the buffer capacitance C_{buf}, the average

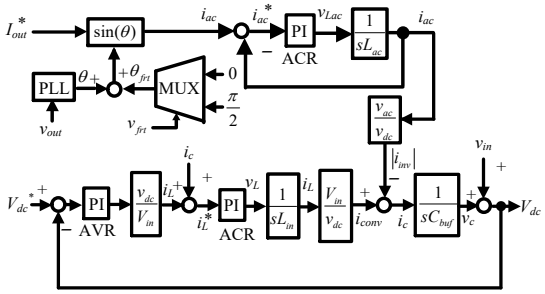


(a) Control block diagram of power decoupling side

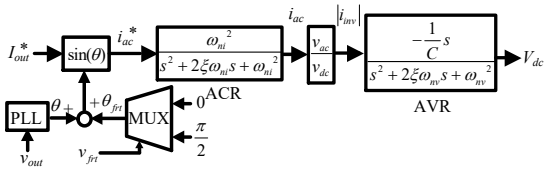


(b) Inverter current disturbance response of power decoupling controller

Fig. 5. Derivation of disturbance response.



(a) Control block diagram of power decoupling side including inverter-output current



(c) Output current disturbance response of power decoupling controller

Fig. 6. Derivation of disturbance response with inverter-output-current controller.

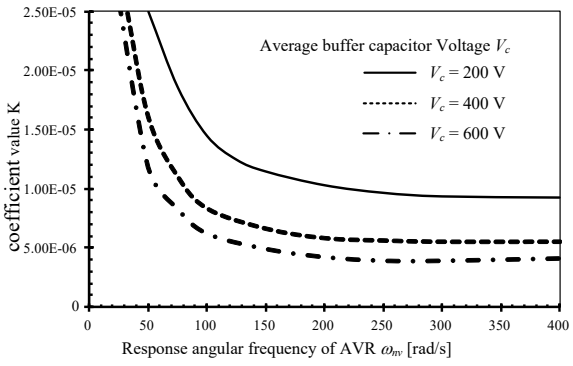


Fig. 7. Coefficient K versus AVR response angular frequency ω_{nv} and buffer capacitor average voltage V_c.

voltage V_c, and the AVR response angular frequency ω_{nv}. The DC-link voltage is proportional to the output power and inversely proportional to the buffer capacitance. The approximate equation is expressed as

$$\Delta V_{dc} = -K \frac{\Delta P_{out}}{C_{buf}} \quad (14).$$

According to (14), the buffer capacitance considering the overshoot of the DC-link voltage is expressed as

$$C_{buf} = -K \frac{\Delta P_{out}}{\Delta V_{dc}} \quad (15).$$

The coefficient K depends on the AVR response angular frequency ω_{nv} and the average voltage of the buffer capacitor average voltage V_c.

Fig. 7 shows the coefficient K with the buffer capacitor average voltage V_c and the AVR response angular frequency ω_{nv}. Fig. 7 is considering the ACR response angular frequency is much larger than the AVR response angular frequency. The coefficient K becomes small when the AVR response angular frequency ω_{nv} is high. However, the coefficient K is almost constant in the high response angular frequency range of AVR. Moreover, the rising limit of the AVR response angular frequency depends on the ACR response angular frequency. The buffer capacitor average voltage V_c becomes high when the coefficient K becomes small. The reason is that more energy is required to raise the buffer capacitor voltage according to (4) and (6). However, raising the average voltage of the buffer capacitor also increases the required withstand voltage of the switching devices. Therefore, the buffer capacitance is designed by the required withstand voltage of the switching devices.

V. Experimental Result

A comparison of the case for DC-link voltage control is performed in VSI side and the power decoupling side. Table II shows the experimental conditions.

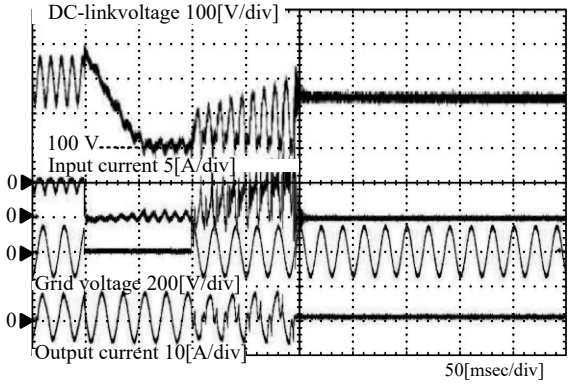
Fig. 9 shows the FRT operation during the grid voltage sag. Note that in order to consider the worst case of the maximum DC-link voltage overshoot, the voltage sag occurs when the DC-link voltage reaches the maximum voltage ripple during the steady-state operation.

Fig. 9 (a) shows the FRT operation when the DC-link voltage control is employed in the VSI control. During the grid voltage sag, the DC-link voltage control employing in the VSI control cannot regulate the DC-link voltage. This is because there is conversion loss existing in the power converter, whereas the input power is set to zero during the voltage sag. As a result, the DC-link voltage drops below the maximum value of the grid voltage to the input voltage (100 V). The grid voltage recovers when the DC-link voltage maximum value is lower than the grid voltage value. Therefore, the input and the output current are distorted. Eventually, the protection circuit operates, and the operation of the grid-tied inverter is halted.

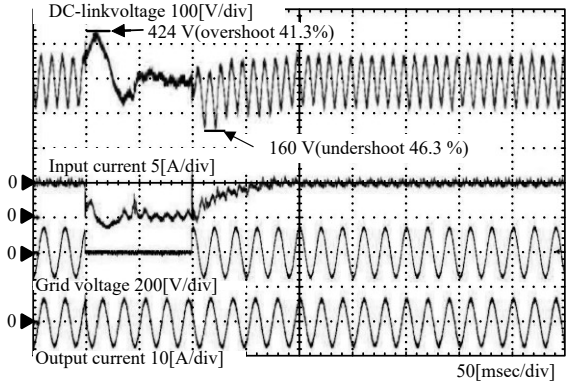
Fig. 9 (b) shows the FRT operation when the DC-link voltage control is employed in the power decoupling

Table II. Experimental conditions with 100-V grid-connection.

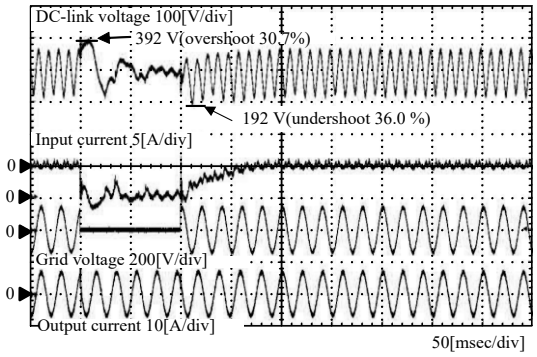
Quantity	Symbol	Value
Input voltage	V_{in}	100 V
Output voltage	V_{out}	100 V
Rated power	P	500 W
Dead time	T_{dt}	3.0 μs
boost inductor	L	3 μH
buffer capacitor	C_{buf}	55 μF
DC-link voltage	v_{dc}	300 V
Interconnected inductor	L_{ac}	6 μH
Switching frequency	f_{sw}	20 kHz
Voltage sag time	T_{vs}	100 ms



(a) DC-link voltage control employing in the VSI control



(b) DC-link voltage control employing in power decoupling circuit (ω_{nv} = 100 rad /s)



(c) DC-link voltage control employing in power decoupling circuit (ω_{nv} = 200 rad /s)

Fig. 9. FRT operation during grid voltage sag at 100 V grid-connection.

circuit. Since the energy required to maintain the voltage is supplied from the input side even during a voltage sag, it is observed that DC-link voltage value follows the command value even during the voltage sag. As a result, the output current distortion does not occur even after the grid voltage recovery. Furthermore, the DC-link voltage overshoot and undershoot are suppressed to 41.3%(124 V) and 46.7%(140 V) for the DC-link average voltage (300 V). The DC-link voltage minimum value is always higher than the grid voltage maximum value. Thus, the FRT operation is achieved without any distortion of the input and the output current. By using the overshoot amount which used the approximation formula in Chapter 4, the theoretical calculation is derived by (14) as $K = 1.5*10^{-5}$. As the result, the amount of the DC-link voltage overshoot is 136 V. The error between the experimental and the calcuration value is 8.8%.

Fig. 9 (c) shows the AVR response angular frequency changed to 200 rad / s from the condition of Fig. 9 (b). The DC-link voltage overshoot and undershoot are suppressed to 30.7% (92 V) and 36.0% (108 V) for the DC-link average voltage (300 V). The overshoot amount at (14) is calculated as $K = 1.05*10^{-5}$. Thus, the amount of the DC-link voltage overshoot is 96 V. The error between the experimental and the calcuration value is 4.2%. Furthermore, raising the AVR response angular frequency reduces not only the overshoot of DC-link voltage but also the undershoot of DC-link voltage.

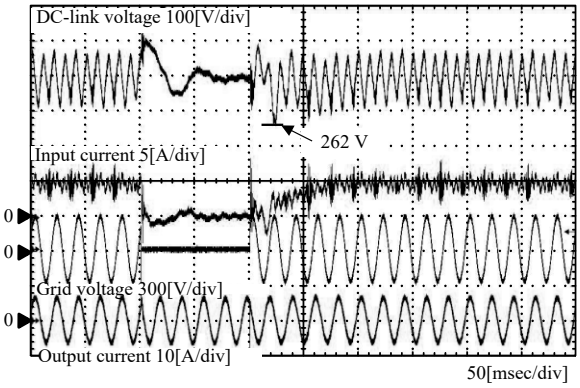
Fig. 10 shows the experimental results of the FRT operation with the designed buffer capacitance considering the overshoot obtained in Chapter 4. Since the maximum rated voltage of IGBT is 600 V which is used in the experiment, the DC-link voltage maximum value including overshoot is designed to be 500 V. Table III shows the conditions of this experiment.

Fig. 10 (a) shows the waveform from start of the voltage sag to the output power recovery. In the experimental waveform, the grid-tied inverter is possible to continue the operation from the start of the voltage sag to the recover of the output power. However, the DC-link voltage maximum value (262 V) becomes lower than the grid voltage maximum value (282 V) due to the DC-link voltage undershoot at the voltage recovery. Although, the input and output current distortion do not occur. Therefore, the buffer capacitance design is also necessary to consider the DC-link voltage undershoot at the grid voltage reovery.

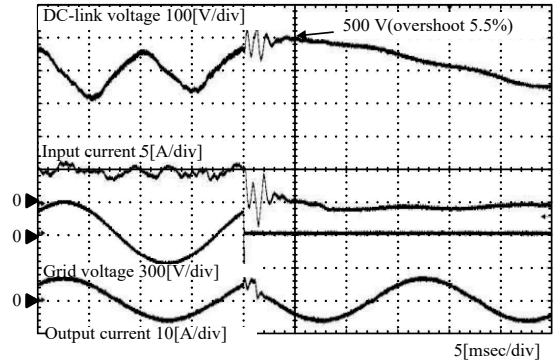
Fig.10 (b) shows the magnified waveform at the occurence of a voltage sag. At the start of the voltage sag, the output current is confirmed to switch from the active current to the reactive current. The overshoot amount of DC-link voltage is 20.0% (100 V) of the DC-link average voltage (400 V). Thus, the DC-link voltage is suppressed to around 500 V. Note that the overshoot amount with (14) is calculated as $K = 1.05*10^{-5}$. As the result, the amount of the DC-link voltage overshoot is 105 V. The error between the experimental and the calcuration value is 4.8%. However, the DC-link voltage is fluctuated due to the resonance of the input current at the start of the voltage sag.

Table III. Experiment parameters with 200-V grid-connection.

Quantity	Symbol	Value
Input voltage	V_{in}	200 V
Output voltage	V_{out}	200 V
Rated power	P	1.0 kW
Response frequency of AVR	ω_{nv}	200 rad/s
Dead time	T_{dt}	3.0 μs
boost inductor	L	6 μH
buffer capacitor	C_{buf}	100 μF
DC-link voltage	v_{dc}	400 V
Interconnected inductor	L_{ac}	12 μH
Switching frequency	f_{sw}	20 kHz
Voltage sag time	T_{vs}	100 ms



(a) Operation waveform with minimum buffer capacitor design



(b) Magnifiged waveform at the start of voltage sag

Fig. 10. Operating waveform by minimum buffer capacitor design at 200 V grid-connection.

Table IV. Comparison of theoretical and experimental value for DC-link voltage overshoot.

Verification conditions						Theoretical Value [V]	Measured value [V]	Error Rate [%]
waveform	P_{out} [W]	C_{buf} [μF]	ω_{nv} [rad/s]	V_c [V]	K [10^{-5}]			
Fig.9 (b)	500	55	100	200	1.5	136	124	8.8
Fig.9 (c)	500	55	200	200	1.05	92	96	4.2
Fig.10	1000	100	200	200	1.05	105	100	4.8

The resonance frequency of the input current fluctuation is 1 kHz, which is caused by the input LC filter resonance.

Table IV shows the comparison between the theoretical and the experimental value for the overshoot amount of the DC-link voltage. From the Table IV, the error between the theoretical and the experimental value is large when the

AVR response angular frequency is low. The cause of the large error is that the coefficient K is used as the approximate equation for the overshoot amount calculation. Other reasens of the error are that the ACR response angular frequency is not included in the the approximate equation and the delay time of the voltage sag detection by HPF is not considered.

VI. Conclusion

In this paper, the FRT operation of the grid-tied inverters with the small capacitance was proposed. The analysis of the minimization limitation for the DC-link capacitance considering the overshoot voltage during the grid voltage sag was introduced. Moreover, it was confirmed that the DC-link voltage control employed in the power decoupling circuit achieved both the FRT operation and the active power decoupling capability. Moreover, the overshoot amount in the experimental result was agreed with the theoretical value using the approximate equation with an error within 10%. The undershoot voltage caused the distortion in the input current and the output current. This problem may stop the circuit operation. In the future work, the calculation of the amount of DC-link voltage undershoot at grid voltage recovery will be considered.

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