Voltage THD Reduction with Discontinuous Current Mode Control for Islanded-mode Operation in Single-phase Grid-tied Inverter

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Keywords

«Renewable energy systems», «Power conditioning», «Non-linear control», «High power density systems», «Silicon Carbide (SiC)», «Single phase system», «Uninterruptible Power Supply (UPS)»

Abstract

This paper proposes a filter capacitor design for a single-phase grid-tied inverter operating under islanded-mode with discontinuous current mode current control to reduce an inverter-side inductance and a filter capacitance without worsening output voltage distortion. The design considers the worst case of load, which is the non-linear load. A voltage source is applied to the circuit model of the load to obtain the harmonics of the current. By using these harmonics and the disturbance transfer function, the output voltage amplitude of the each harmonic components are obtained to calculate the output voltage total harmonic distortion (THD). Then, the filter capacitor satisfying the output voltage THD is determined by the theoretical output voltage THD calculation formula. The simulated output voltage THD agrees with the calculation value with the error of below 10%. As experimental results with 1.5-kVA prototype, the output voltage THD with the CCM/DCM control method and the current feedforward is reduced by 88.8% compared to that of the continuous current mode control method even with the minimized inductor impedance of 0.19% and minimized capacitor admittance of 6.7%.

Introduction

In recent year, photovoltaic (PV) systems have attracted many attentions due to an increasing demand of renewable resources [1]-[5].

In general, an islanded-mode operation is required for the grid-tied inverters to supply the power to the load during a black out [2], [4], [10]-[12]. In the islanded-mode operation, the grid-tied inverter needs to regulate the load voltage regardless of the load characteristic, i.e. the achievement of the sinusoidal voltage regulation even with the nonlinear or low-power-factor load. The non-linear effect due to the dead-time is small when the inductance of the inverter-side inductor is large. Therefore, the regulation of the output voltage total harmonic distortion (THD) can be satisfied even with a small capacitance of the filter capacitor. However, the disturbance characteristics of the current control induced by the dead-time decays in the reduction of the inverter-side inductance for the achievement of high power density. Consequently, the inductance reduction leads to the increase in the grid current THD when the inverter is operated in continuous current mode (CCM) [12]. In the islanded-mode operation, this current distortion acts as a disturbance of a voltage control, and the small capacitance of the filter capacitor cannot compensate for such disturbance. As typical solution, it is necessary to satisfy the regulation with output voltage THD by increasing the filter capacitance. Consequently, it is difficult to miniaturize both the inverter-side inductor and the filter capacitor.

Meanwhile, many dead-time error compensation methods have been proposed for the purpose of improving the disturbance characteristics of the current control system [5]-[9]. However, the conventional dead-time error compensations either cannot compensate completely the nonlinearity

induced by the dead-time, or become dependent on the inductance. In order to solve these problems, a current control method for both CCM and discontinuous current mode (DCM) is proposed for the single-phase grid-tied inverter [9]. In this method, the duty ratio at the previous computation period is utilized to compensate the DCM nonlinearity induced by the dead-time. In the CCM/DCM feedback current control method, the low output current THD can be achieved in any load condition even with a small inductance. However, the island mode operation for the single grid-tied inverter operating in both CCM and DCM, and the design of the filter capacitor with small LC filters have not been considered.

This paper proposes a filter capacitor design for the single-phase grid-tied inverter operating under islanded-mode with a CCM/DCM current control to reduce the inverter-side inductance and the filter capacitance without worsening the output voltage distortion. The islanded-mode operation with the CCM/DCM feedback current control are compared to that with the CCM feedback current control under conditions of the same voltage controller and same current controller. The new contribution of this paper is the filter capacitor design satisfying the output voltage distortion constrains even with the small inverter-side inductance and filter capacitance. The filter capacitor design based on the disturbance characteristics of the control system can satisfy the desired output voltage THD with the smallest reducible filter capacitance. In particular, by using the output voltage control method with CCM/DCM control, the reduction of the filter capacitor voltage THD is confirmed with a 1.5-kVA 100-kHz prototype.

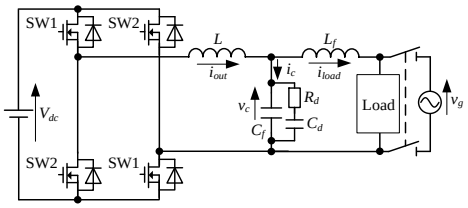
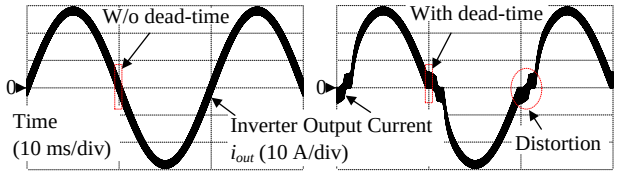
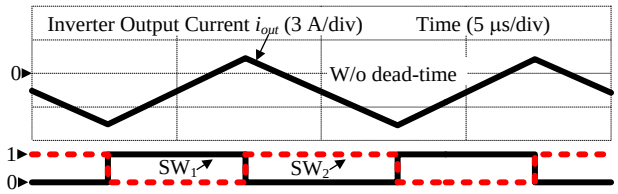


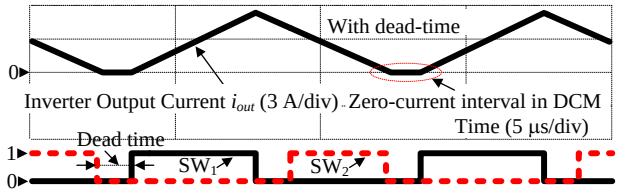
Fig. 1. Single-phase grid-connected inverter with LCL filter.



(a) Inverter output current w/o dead-time and with dead-time



(b) Zoomed-in current and switching signals w/o dead-time



(c) Zoomed-in current and switching signals with dead-time

Fig. 2. Zero-crossing current distortion.

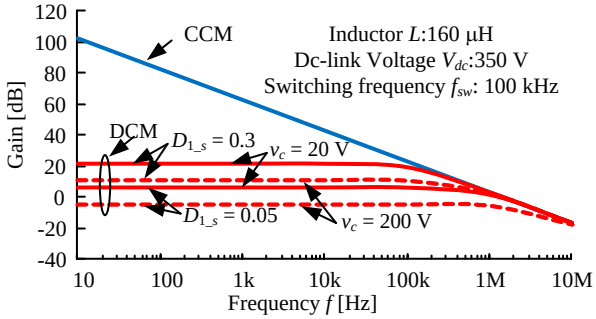


Fig. 3. Duty to current gain in CCM and DCM.

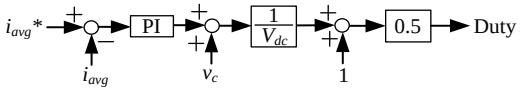
Continuous and Discontinuous Current Mode Control

Fig. 1 indicates the circuit configuration of a single-phase grid-tied inverter with a LCL filter. In this paper, a single-phase H-bridge inverter is applied due to its simplicity. The LCL filter with shunt RC connecting the inverter to the grid smooths the output current and reduces the current resonance [3].

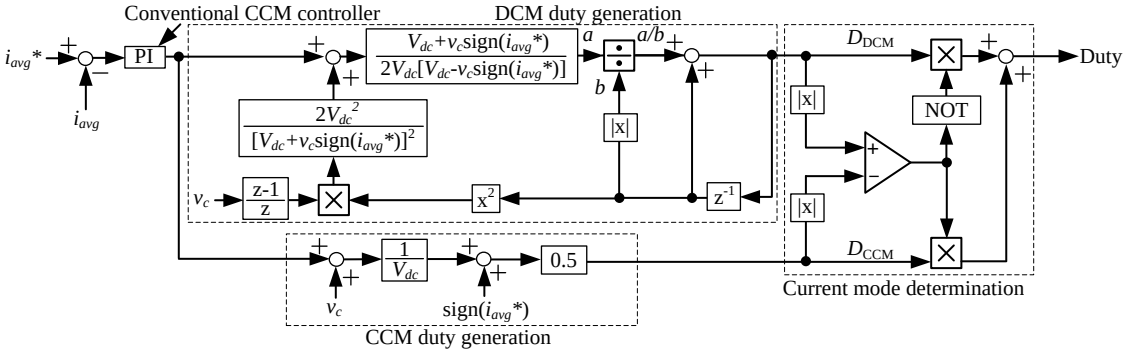
Fig. 2 shows the zero-crossing current distortion during the grid-tied operation. As shown in Fig. 2(a) and Fig. 2(b), when the dead-time is not applied, the inverter output current flows continuously over entire the switching period; hence, a sinusoidal current waveform is obtained. However, the zero-current clamping occurs during the dead-time interval due to the influence of the period when all switches are turned off as shown in Fig. 2(a) and 2(c). The circuit mode changes from CCM to DCM due to the zero-current clamping.

Fig. 3 depicts the duty to current gain in CCM and DCM. The duty to current gain of DCM has a strong nonlinearity compared the duty to current gain of CCM. This worsens the current response in DCM if the same controller in CCM is employed in DCM.

Fig. 4(a) and Fig. 4(b) show the CCM feedback current control system and the



(a) CCM feedback current control.



(b) CCM/DCM feedback current control.

Fig. 4. CCM feedback current control and CCM/DCM feedback current control.

CCM/DCM feedback current control system, respectively [9]. The same PI controller which is designed in CCM is applied in the feedback current control for both the CCM operation and the CCM/DCM operation, because the DCM nonlinear factors are completely compensated in the CCM/DCM control method. Furthermore, the important characteristic of the CCM/DCM control method is that the DCM duty generation is independent from the inductance.

Islanded-mode Operation and Filter Capacitor Design

Fig. 5 describes the filter capacitor design algorithm base on the output voltage THD. The filter capacitor design starts with the initialization of the following parameters: the current control cutoff frequency f_{c_i}, the current control damping factor ζ_i, the voltage control cutoff frequency f_{c_v}, the voltage control damping factor ζ_v, the output voltage v_c, the cutoff frequency of disturbance observer f_{dob}, the output frequency f_g, the filter capacitance C_f, the damping capacitance C_d, the damping resistor R_d. First, the desired output voltage THD is selected based on the regulation of IEC 62040-3. In step 1, the harmonic components of the load current when connecting an ideal voltage source is obtained from simulator such as *PLECS* (*Plexim Inc.*). Next, in step 2, the transfer function of the voltage control loop is derived to calculate the compensation gain K_t. Finally, in step 3, the filter capacitor C_f satisfying the output voltage THD is determined by the theoretical output voltage THD calculation formula.

Step 1: Harmonic analysis of load current

Fig. 6 shows the non-linear load configuration connecting with an ideal voltage source. In this paper, the non-linear load with crest factor of 2.3 is considered as the worst case of the load. The non-linear load contains a diode-bridge rectifier connecting a capacitor and a load resistor in parallel at the output, i.e. the rectifier load. The disturbance current harmonic component at the maximum load is required to design the filter capacitor that satisfies the output voltage THD at the worst condition of load. The disturbance current harmonic component of non-linear load is obtained by connecting the ideal voltage source as shown in Fig. 6. The disturbance current of the non-linear load with the harmonic analysis up to 40^{th}-order are obtained to calculate the output voltage THD.

Fig. 7 shows the harmonic analysis of the non-linear load current with the output frequency of 50 Hz as the fundamental component. The harmonic components of the non-linear load current are dominated by the odd-order harmonic components. Therefore, the calculation of the output voltage THD uses only the load current value of the fundamental wave components is A_1, and the load current harmonic components of A_{2n+1}, where n is a natural number from 1 to 20.

Step 2: Derivation of transfer function and calculation of compensation gain K_t

Fig. 8 shows the block diagram of the voltage feedback control for islanded-mode operation. Note that subscript M indicates a nominal model value. The filter capacitor voltage control and the current control are designed based on the 2^{nd}-order transfer function. The bandwidth of the current control is

limited by the sampling rate of the hardware, which is considered to be low in this paper, leading to the low bandwidth of the filter capacitor voltage control. Therefore, the compensation gain K_t is introduced to adjust the amplitude of the voltage reference. The output of the PI controller in the filter capacitor voltage control is the filter capacitor current command i_c*. Hence, the voltage PI controller requires the feed-forward of the load current i_{load} to eliminate the disturbance from the load current. As another approach, it is possible to apply a disturbance observer (DOB) that estimates and compensates the disturbance from the load current i_{load} in the voltage control system. As shown in Fig. 8, the response transfer function of current control G(s) is expressed by

$$G(s)=\frac{\frac{K_{pi}}{L}s+\frac{K_{pi}}{T_{ii}L}}{s^2+\frac{K_{pi}}{L}s+\frac{K_{pi}}{T_{ii}L}}=\frac{4\pi\zeta_i f_{c\_i}s+\left(2\pi f_{c\_i}\right)^2}{s^2+4\pi\zeta_i f_{c\_i}s+\left(2\pi f_{c\_i}\right)^2} \quad (1),$$

where L is the inverter-side inductance, K_{pi} and T_{ii} are gains calculated from L, f_{c_i} and ζ_i. By the employment of the CCM/DCM control method, the DCM nonlinearity is compensated, and the response transfer function of the current control is the 2nd-order system. Meanwhile, in the case of the CCM control method, the response transfer function of the current control changes due to the DCM nonlinearity induced by the dead-time.

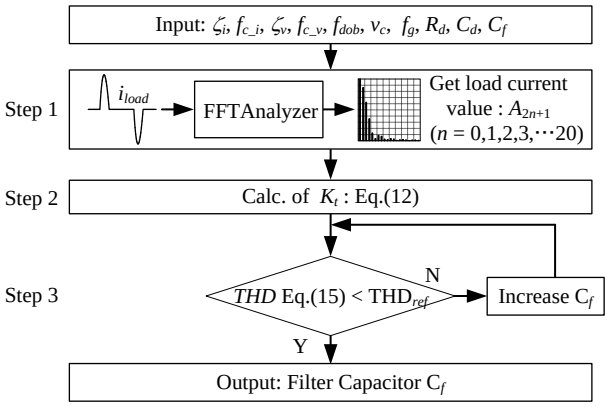
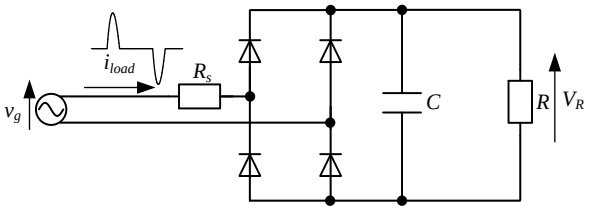


Fig. 5. Filter capacitor design algorithm.



Parameters: R_s=3.3 Ω, C=2040 μF, R=63 Ω , (Crest factor is 2.3.)

Fig. 6. Non-linear load configuration connected to ideal voltage source.

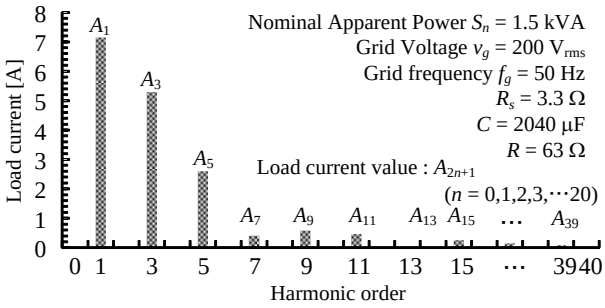


Fig. 7. Harmonic component of non-linear load current.

The plant model for the voltage control and the nominal plant model for the voltage control are expressed by

$$P_C(s)=P_{CM}(s)=\frac{R_dC_ds+1}{R_dC_dC_fs^2+\left(C_d+C_f\right)s} \quad (2)$$

The voltage controller G_{pi}(s) and the reference filter F(s) are expressed by, respectively

$$G_{pi}(s)=K_{pv}\left(1+\frac{1}{T_{iv}s}\right)=4\pi\zeta_v f_{c\_v}\left(C_f+C_d\right)\left(1+\frac{2\pi f_{c\_v}}{2\zeta_v s}\right) \quad (3),$$

$$F(s)=\frac{K_t}{T_{iv}s+1}=\frac{K_t}{\frac{2\zeta_v}{2\pi f_{c\_v}}s+1} \quad (4),$$

where K_{pv} and T_{iv} are gains calculated from C_f, C_d, f_{c_v} and ζ_v. Note that the cutoff frequency of the voltage controller and the cutoff frequency of the current controller are designed to be separated by 5 times or more. The feedback transfer function of DOB is expressed by

$$G_{DOB}(s)=\frac{2\pi f_{dob}}{s+2\pi f_{dob}} \quad (5),$$

where f_{dob} is the cutoff frequency of DOB. The disturbance estimation value i_{dis} is expressed by

$$\hat{i}_{dis}=G_{DOB}(s)\left[i_{out}-P_{CM}{}^{-1}(s)v_c\right] \quad (6)$$

Fig. 9 shows the transfer functions of the disturbance and the response. The response transfer function G_{ref}(s) of the voltage control is the transfer function from the output voltage command to the output

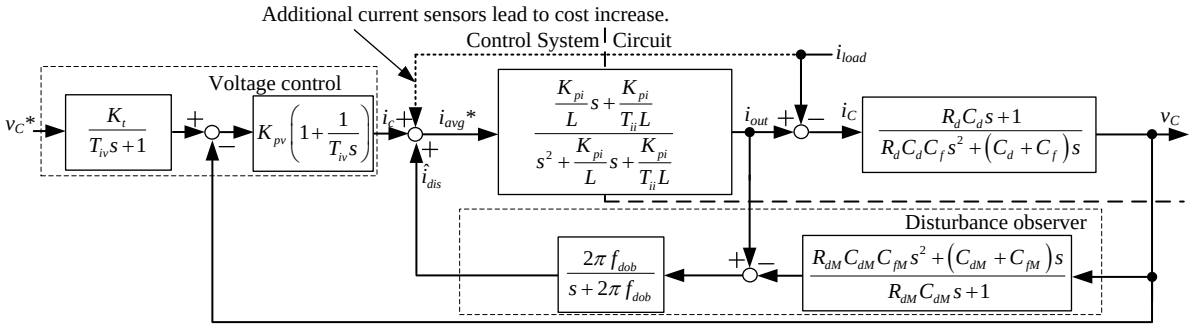


Fig. 8. Control block diagram for islanded-mode operation.

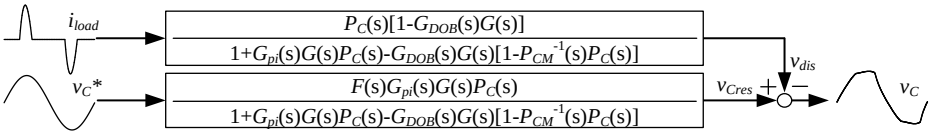


Fig. 9. Transfer functions of disturbance and response.

voltage. The disturbance transfer function $G_{dis}(s)$ of the voltage control is the transfer function from the load current to the output voltage. The response transfer function $G_{ref}(s)$ of the voltage control and the disturbance transfer function $G_{dis}(s)$ of the voltage control are expressed by, respectively

$$G_{ref}(s)=\frac{F(s)G_{pi}(s)G(s)P_C(s)}{1+G_{pi}(s)G(s)P_C(s)-G_{DOB}(s)G(s)\left[1-P_{CM}^{-1}(s)P_C(s)\right]} \quad (7),$$

$$G_{dis}(s)=\frac{P_C(s)\left[1-G_{DOB}(s)G(s)\right]}{1+G_{pi}(s)G(s)P_C(s)-G_{DOB}(s)G(s)\left[1-P_{CM}^{-1}(s)P_C(s)\right]} \quad (8)$$

The transfer functions of the disturbance and the response include the voltage controller, the response transfer function of the current control, the plant model for the voltage control and the transfer function of DOB. Therefore, the transfer function of disturbance and response are mutually dependent on each other. In the proposed filter capacitor design method, the disturbance transfer function satisfying the output voltage THD is designed by selecting the filter capacitance design, whereas the low-bandwidth response transfer function is compensated using the compensation gain K_t. As shown in Fig. 9 and (7)-(8), the output voltage is expressed by

$$v_C=G_{ref}(s)v_C^{*}-G_{dis}(s)i_{load} \quad (9)$$

If the transfer functions and input parameters on the right equation are known, the output voltage can be estimated. The output voltage command is expressed by

$$v_C^{*}=V_C\sin\left(2\pi f_g t\right) \quad (10),$$

where V_c is the output maximum voltage. In the islanded-mode operation, the fixed output voltage and fixed output frequency are used as command values. In addition, according to (7), the voltage control system is a two degree of freedom system. Thus, the gain of the output frequency of (7) can be set at 0dB by the compensation gain K_t of (4). The calculation for the gain compensation at the output frequency of (7) is expressed by

$$\left|G_{ref}(j2\pi f_g)\right|=1 \quad (11)$$

Then, the compensation gain K_t satisfying (11) is expressed by

$$K_t=\frac{T_{iv}}{K_{pv}}\sqrt{\left[\frac{K_{pv}}{T_{iv}}-\left(C_f+C_d\right)\left(2\pi f_g\right)^2\right]^2+\left[K_{pv}\left(2\pi f_g\right)\right]^2}=\sqrt{\left[1-\left(\frac{f_g}{f_{c\_v}}\right)^2\right]^2+\left[2\zeta_v\frac{f_g}{f_{c\_v}}\right]^2} \quad (12)$$

The current control interference is ignored as being sufficiently separated from the voltage control in term of the control bandwidth.

Step 3: Determination of filter capacitor satisfying output voltage THD

By using the result of the harmonic components analysis of the load current in Fig. 7 and the disturbance transfer function of (8), the output voltage amplitude of the fundamental component V_1 and the output voltage amplitude of the odd-order harmonic components V_{2n+1} are expressed by, respectively

$$\begin{cases} V_1 = V_C \left| G_{ref}(j2\pi f_g) \right| + A_1 \left| G_{dis}(j2\pi f_g) \right| = V_C + A_1 \left| G_{dis}(j2\pi f_g) \right| \\ V_{2n+1} = A_{2n+1} \left| G_{dis}(j2\pi(2n+1) f_g) \right| \end{cases} \tag{13}$$

Next, THD of the output voltage is calculated as

$$THD = \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + \cdots + V_{2n+1}^{\,2}}}{V_1} \tag{14}$$

Substituting (13) into (14), the theoretical output voltage THD is expressed by

$$THD_{v_c}(C_f) = \frac{\sqrt{\sum_{n=1}^{20} V_{2n+1}^{\,2}}}{V_1} = \frac{\sqrt{\sum_{n=1}^{20} \left[A_{2n+1} \left| G_{dis}(j2\pi(2n+1) f) \right| \right]^2}}{V_c + A_1 \left| G_{dis}(j2\pi f) \right|} \tag{15}$$

Thus, the output voltage THDv_c is a function of the filter capacitor C_f.

Fig. 10 depicts the comparison between simulated and calculated results of voltage THD while varying the filter capacitance. The simulated results of the CCM control method without dead-time, the CCM control method with dead-time and the CCM/DCM control method with dead-time are compared. The disturbance of the voltage control is compensated by the current feedforward in Fig. 10(a) and Fig. 10(b), whereas the disturbance of the voltage control is compensated by DOB in Fig. 10(c). Note that the base impedance Z_b and the base admittance Y_b is expressed by

$$Z_b = \frac{v_c^{\,2}}{P_n} = \frac{1}{Y_b} \tag{16}$$

whrer P_n is the rated active power at connected to linear load power factor of 1.0. The percentage impedance %Z and the percentage admittance %Y is expressed by

$$\%Z = \frac{2\pi f_g L}{Z_b} \tag{17}$$

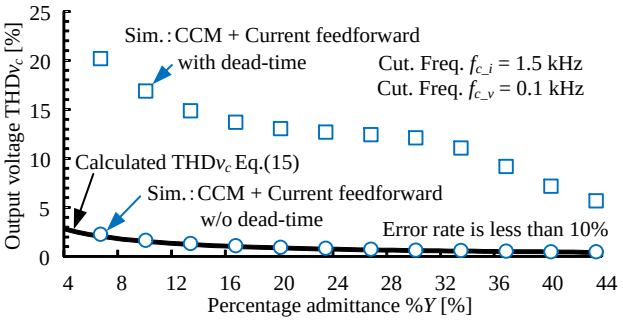
$$\%Y = \frac{2\pi f_g C}{Y_b} \tag{18}$$

where C is the filter capacitance.

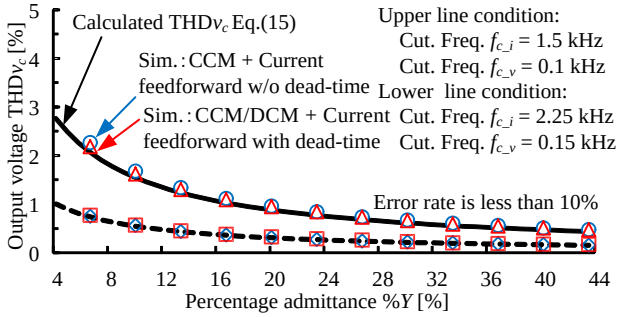
As shown in Fig. 10(a), the voltage THD of the CCM control method without dead-time agrees to the calculated value with the error of less than 10%. Thus, the validity of (15) can be confirmed. Meanwhile, in the CCM control method with dead-time, the simulated value does not match the calculated value. This is because the nonlinearity of the DCM cannot be compensated.

As shown in Fig. 10(b), the voltage THD of the CCM control method without dead-time and the voltage THD of the CCM/DCM control method with dead-time agree to the calculated value with the error of less than 10% even when the cutoff frequencies are different. This is because the CCM/DCM control method compensates the DCM nonlinearity, hence, the current control response is as same as that in CCM.

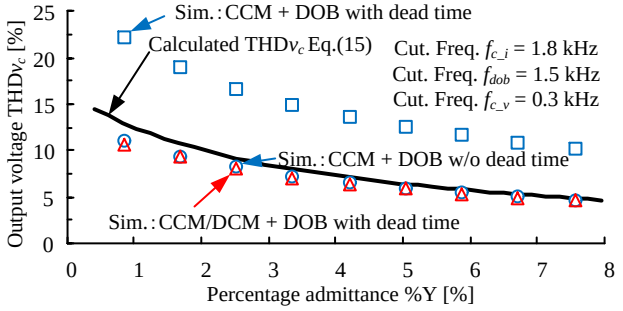
As shown in Fig. 10(c), the voltage THD of the CCM control method without dead-time matches that of the CCM/DCM control method with dead-time. However,



(a) CCM control method w/o or with dead-time, and voltage control disturbance compensation method with current feedforward



(b) CCM control method w/o dead-time value, CCM/DCM control method with dead-time, and voltage control disturbance compensation method with current feedforward



(c) CCM control method w/o or with dead-time, CCM/DCM control method with dead-time, and voltage control disturbance compensation method with DOB

Fig. 10. Comparison between simulated and calculated results of voltage THD.

the voltage THD of the CCM/DCM control method with dead-time does not match the calculated value. This is because the output voltage THD is so high that it causes an error with the assumption of the use of the ideal voltage source as shown in Fig. 6. Thus, it is necessary to increase the cutoff frequency of DOB, the cutoff frequency of voltage controller and the cutoff frequency of current controller. By employing the CCM/DCM control method and using the proposed filter capacitor design method of Fig. 5, it is possible to design a minimized filter capacitance that satisfies the desired output voltage THD.

Experimental Results

Table I shows the system parameters for the experiments. The impedance %Z of the inverter-side inductor is minimized to 0.19%. In the islanded-mode, the inverter regulates the output voltage, whose frequency is 50 Hz, and amplitude is 200 V_{rms}.

Fig. 11 shows the prototypes of inverter-side inductor. The inductor volume is reduced by 53% thank to the reduction of the inverter-side inductor impedance %Z from 0.68% to 0.19%.

Inverter Operation with Linear Load

Fig. 12 shows the output voltage, the load current and the inverter output current when the CCM control method with DOB at %Z=0.68%, %Y=6.7%, and linear load power factor of 1.0. The zero-crossing distortion is observed with the CCM control method even with the relatively large inductor impedance of 0.68%.

Fig. 13 shows experimental waveforms of the CCM control method and the CCM/DCM control method with DOB at the linear loads under the power factors of 1.0 and 0.85, respectively.

As shown in Fig. 13(a) and 13(c), the zero-crossing distortion is observed with the CCM control method. Furthermore, the output voltage THD is over 5.6% under the power factor of 1.0 and 0.85, respectively. On the other hand, as shown in Fig. 13(b) and 13(d), the CCM/DCM operation can be observed clearly from the inverter output current. In the CCM/DCM control method, the DCM nonlinear factors are effectively compensated, resulting in the reduction of the output voltage THD.

Fig. 14 depicts the comparison of output voltage THD characteristics between the CCM control and the CCM/DCM control under constant effective power condition. As shown in Fig. 14, the output voltage THD of the CCM control method is higher than 3.0% over output power range from 0.2 to 1.0p.u.. According to standard such as IEC 62040-3, the output voltage THD with the linear load must be lower than 3%; hence, the islanded-mode operation with the

TABLE I System Parameters.

Circuit Parameter		
V_{DC}	DC link Voltage	350 V
v_c	Output Voltage	200 Vrms
S_n	Nominal Apparent Power	1.5 kVA
Switching Device		SCT3030AL
f_g	Grid Frequency	50 Hz
Z_b	Base Impedance	26.7 Ω
Y_b	Base Admittance	0.0375 S
L_1	Inductor (%Z = 0.19%)	160 μH
L_2	Inductor (%Z = 0.68%)	580 μH
L_f	Filter Inductor	20 μH
C_{f_1}	Filter Capacitor (%Y = 1.7%)	2 μF
C_{f_2}	Filter Capacitor (%Y = 3.4%)	4 μF
C_{f_3}	Filter Capacitor (%Y = 6.7%)	8 μF
C_{f_4}	Filter Capacitor (%Y = 20%)	24 μF
C_{f_5}	Filter Capacitor (%Y = 41%)	49 μF
C_d	RC Damping Capacitor	4 μF
R_d	RC Damping Resistor	4.7 Ω
f_{sw}	Switching Frequency	100 kHz
T_{dead}	Dead-Time	500 ns
Non-linear load crest factor		2.3
Controller Parameter		
f_{samp}	Sampling Frequency	25 kHz
f_{c_i}	Cutoff Freq. of Current	1.8 kHz
ζ_i	Damping Factor of Current	1.2
f_{dob}	Cutoff Freq. of DOB	1.5 kHz
f_{c_v}	Cutoff Freq. of Voltage	0.3 kHz
ζ_v	Damping Factor of Voltage	1.0

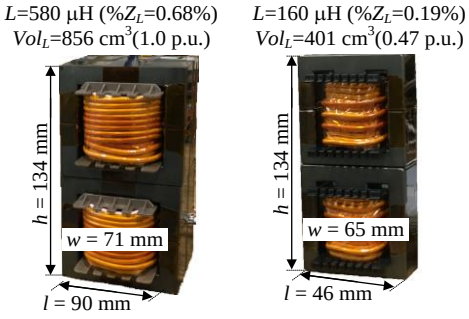


Fig. 11. Prototypes of inverter-side inductor.

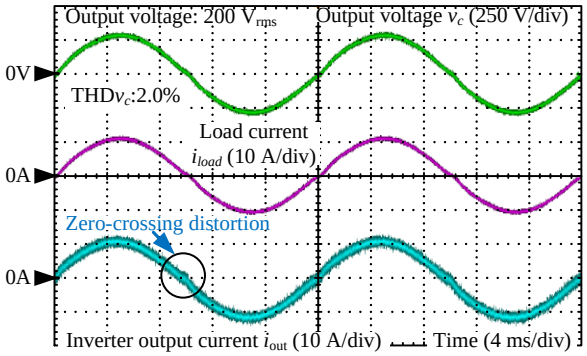
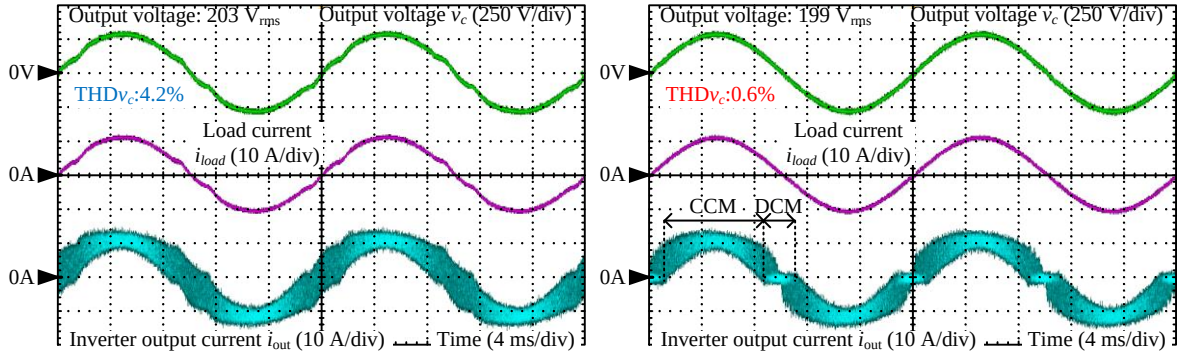
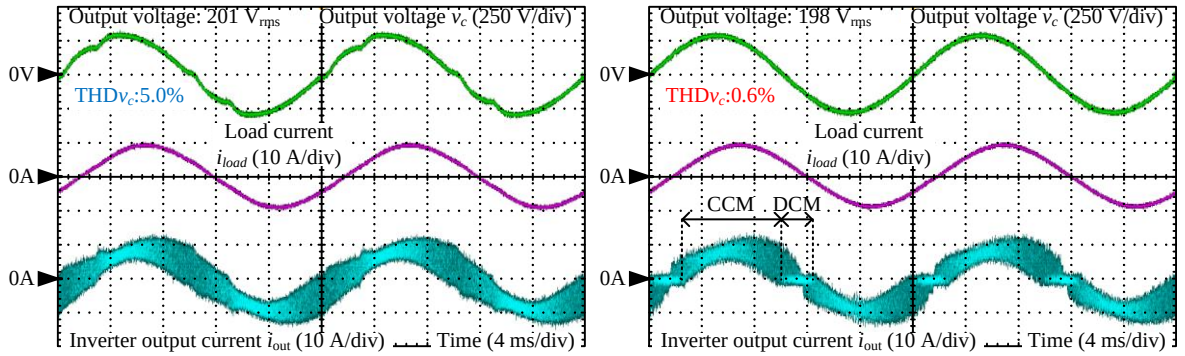


Fig. 12. Inverter operation waveforms with CCM control method and DOB at %Z=0.68%, %Y = 6.7, and linear load power factor of 1.0.



(a) CCM control method with DOB at power factor of 1.0

(b) CCM/DCM control method with DOB at power factor of 1.0



(c) CCM control method with DOB at power factor of 0.85

(d) CCM/DCM control method with DOB at power factor of 0.85

Fig. 13. Inverter operation waveforms with CCM control method and CCM/DCM control method at %Z = 0.19, %Y = 6.7 and different linear load power factor.

CCM control method, of which the output voltage THD at the linear load is 4.2%, does not satisfy the harmonic constrains. On the other hand, the output voltage THD of the CCM/DCM control method is maintained below 3.0% over the output power range from 0.2 to 1.0p.u.. In particular, at the rated power, the output voltage THD with the CCM/DCM control method is reduced by 84.6% from 4.2% to 0.6% compared to the CCM control method.

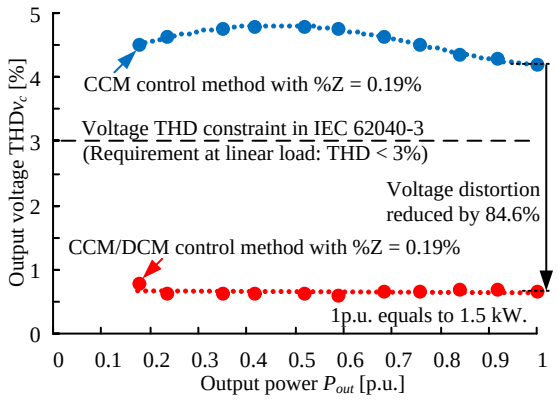
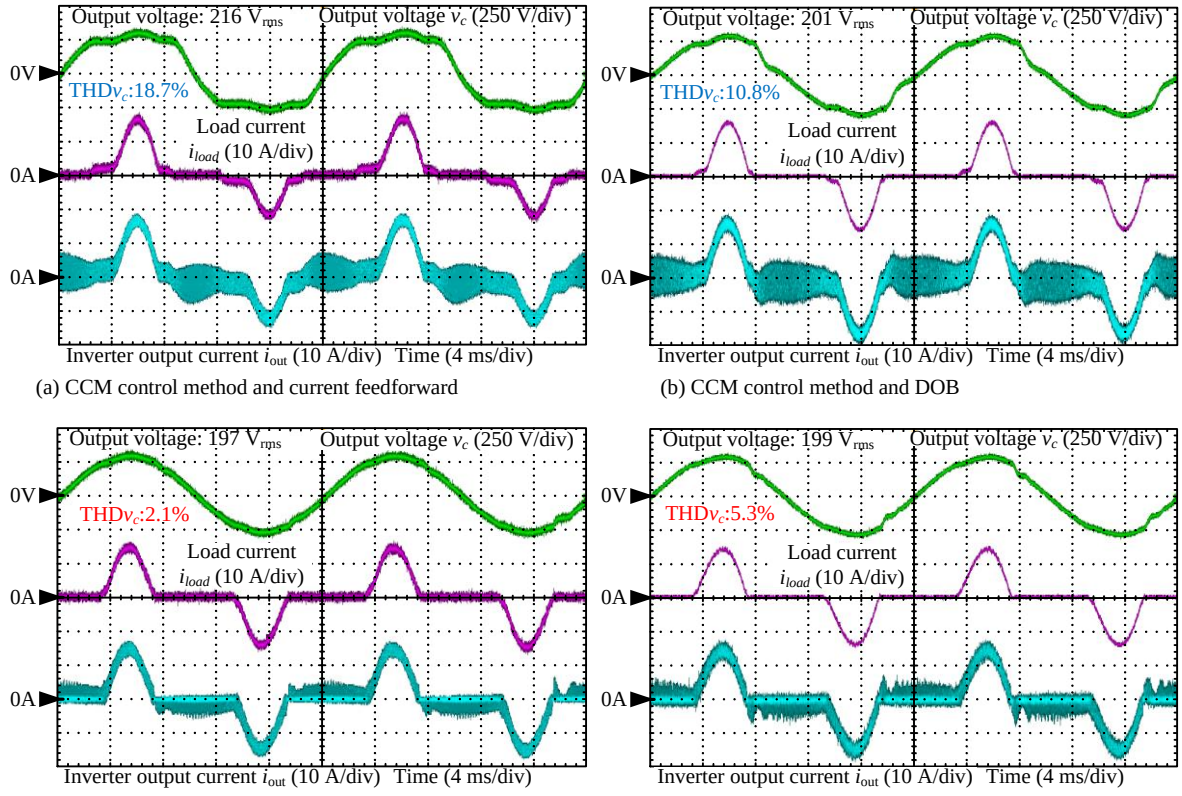


Fig. 14. Comparison of output voltage THD.

Inverter Operation with Non-linear Load

Fig. 15 shows the experimental waveforms of the CCM control method and the CCM/DCM control method with current feedforward and DOB at the non-linear load. Note that additional current sensors lead to cost increase if the current feedforward is applied. Fig. 15(a) and 15(b) depict the CCM control method with current feedforward and DOB, respectively. Meanwhile, Fig. 15(c) and 15(d) depicts the CCM/DCM control method with current feedforward and DOB, respectively. The zero-crossing distortion is observed with the CCM control method as shown in Fig. 15(a) and 15(b), whereas the smooth current control is confirmed with the CCM/DCM control method in Fig. 15(c) and 15(d). The CCM/DCM control method can be observed clearly from the inverter output current. It is possible to compensate the DCM nonlinear factors with the CCM/DCM control method even with non-sinusoidal current such as the non-linear load current.

As shown in 15(d), the voltage THD is lower with the current feedforward than that with DOB compared to Fig. 15(c). This is because with the low cutoff frequency of DOB, the phase delay of the estimated disturbance current and the circuit parameter errors occur, leading to the insufficient disturbance compensation. Note that the control system becomes sensitive to noise when the high cutoff frequency of DOB is applied. As shown Fig. 15(a), the output voltage distortion is observed with the CCM control method even with the current feedforward. It is difficult to improve the output voltage



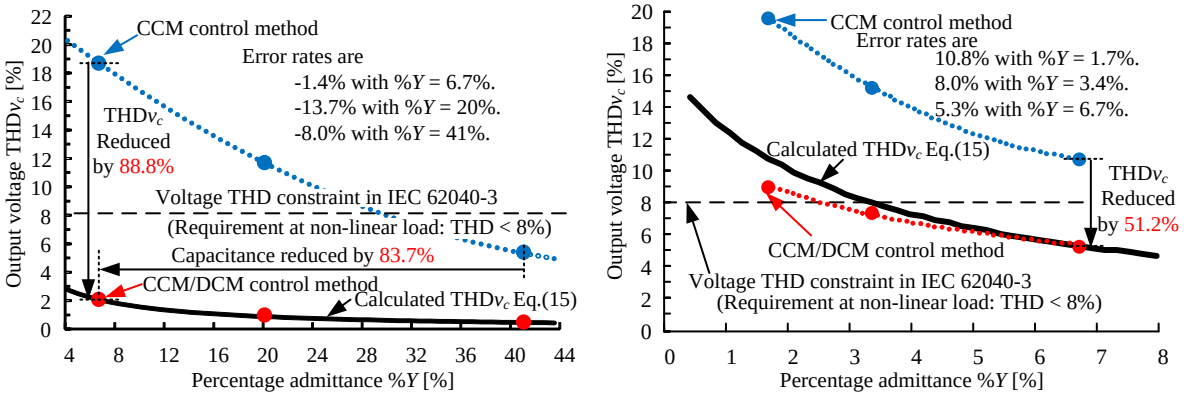
(a) CCM control method and current feedforward

(b) CCM control method and DOB

(c) CCM/DCM control method and current feedforward

(d) CCM/DCM control method and DOB

Fig. 15. Inverter operation waveforms with CCM control method and CCM/DCM control method at %Z=0.19%, %Y=6.7% and non-linear load with crest factor of 2.3.



(a) Output voltage THD with current feedforward

(b) Output voltage THD with DOB

Fig. 16. Comparison of output voltage THD.

THD due to the DCM nonlinearity even if the disturbance current is compensated by the current feedforward.

Fig. 16 depicts the output voltage THD versus the filter capacitance between the CCM control and the CCM/DCM control and the calculated output voltage THD with current feedforward and DOB under the non-linear load condition. As shown in Fig 16(a), the output voltage THD with the CCM/DCM control method is reduced by 88.8% from 18.7% to 2.1% compared to the CCM control method. The percentage admittance %Y with the CCM/DCM control method is reduced by 83.7% from 41% to 6.7% compared to the CCM control method. Moreover, the output voltage THD of CCM/DCM control method with current feedforward agrees to the calculated voltage THD in (15) with a maximum error of -13.7% at the percentage admittance %Y of 20%. As shown in Fig 16(b), the output voltage THD with the CCM/DCM control method is reduced by 51.2% from 10.8% to 5.3% compared to the CCM control method. However, the output voltage THD of CCM/DCM control method does not match the calculated voltage THD in (15). This is because the output voltage THD is so high that it causes an error with the assumption of the use of the ideal voltage source as shown in Fig. 6. Thus, it is necessary to increase the

cutoff frequency of DOB, the cutoff frequency of voltage controller and the cutoff frequency of current controller.

Conclusion

This paper proposed the filter capacitor design for the single-phase grid-tied inverter operating under islanded-mode with discontinuous current mode current control to reduce the inverter-side inductance and the filter capacitance without worsening output voltage distortion. The design considered the worst case of load, which is the non-linear load. The voltage source was applied to the circuit model of the load to obtain the harmonics of the current. Then, these harmonics were inputted to the equation calculated from the transfer function of the control system to calculate the required capacitor. The simulated output voltage THD agreed to the calculation value with the error of below 10%. As experimental results, the CCM/DCM control method achieved the low voltage distortion even with the minimized inverter-side inductance, whose impedance %Z was 0.19%. At the non-linear load, the output voltage THD with the CCM/DCM control method and the current feedforward is reduced by 88.8% compared to that of the CCM control method even with the minimized inductor impedance of 0.19% and minimized capacitor admittance of 6.7%. The output voltage THD of CCM/DCM control method with the current feedforward agreed to the calculated voltage THD in (15) with a maximum error of -13.7% at the percentage admittance %Y of 20%.

References

[1] B. Liu, T. Yoshino and A. Kawamura, "Seamless Control of Grid-Connected Inverter during Single Phase Disconnection after Single Phase Fault in a Weak Grid", in *IEEJ Journal of Industry Applications*, vol. 7, no. 6, pp. 506-516, 2018.

[2] R.-J. Wai, C.-Y. Lin, Yu-C. Huang and Y.-R. Chang, "Design of High-Performance Stand-Alone and Grid-Connected Inverter for Distributed Generation Applications", in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1542-1555, April. 2013.

[3] W. Wu, Y. He, T. Tang and F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter", in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4339-4350, Oct. 2013.

[4] Md. N. Arafat, S. Palle, Y. Sozer and I. Husain, "Transition Control Strategy Between Standalone and Grid-Connected Operations of Voltage-Source Inverters", in *IEEE Transactions on Industry Applications*, vol. 48, no. 5, pp. 1516-1525, Sept. 2012.

[5] S. Nagai, H. N. Le, T. Nagano, K. Orikawa and J. Itoh, "Minimization of Interconnected Inductor for Single-Phase Inverter with High-Performance Disturbance Observer", in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 22-26, May. 2016.

[6] M. A. Herran, J. R. Fischer, S. A. Gonzalez, M. G. Judewicz and D. O. Carrica, "Adaptive Dead-Time Compensation for Grid-Connected PWM Inverters of Single-Stage PV Systems", in *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2816-2825, Nov. 2013.

[7] K. D. Gusseme, D. M. Van de Sype, Alex P. M. Van de Bossche and J. A. Melkebeek, "Digitally controlled Boost Power-Factor-Correction Converters Operation in Both Continuous and Discontinuous Conduction Mode", in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 88-97, Feb. 2005.

[8] T. Mannen and H. Fujita, "Dead-Time Compensation Method Based on Current Ripple Estimation", in *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 4016-4024, July 2015.

[9] H. N. Le and J. Itoh, "Inductance-Independent Nonlinearity Compensation for Single-Phase Grid-Tied Inverter Operating in Both Continuous and Discontinuous Current Mode", in *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4904-4919, May. 2019.

[10] C. Wang and M. H. Nehrir "Power Management of a Stand-Alone Wind/Photovoltaic/Fuel Cell Energy System", in *IEEE Transactions on Energy Conversion*, vol. 23, no. 3, pp. 957-967, Sept. 2008.

[11] H. Tao, J. L. Duarte and M. A. M. Hendrix, "Line-Interactive UPS Using a Fuel Cell as the Primary Source", in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 3012-3021, Aug. 2008.

[12] S. Nagai and J. Itoh, "Open-loop-based Island-mode Voltage Control Method for Single-phase Grid-tied Inverter with Minimized LC Filter", in *IEEJ Journal of Industry Applications*, vol. 8, no. 1, pp. 108-115, 2019.