

# Thermal Stress Reduction for DC-link Capacitors of Three-phase VSI with Multiple PWM Switching Patterns

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**Abstract**—This paper demonstrates the thermal stress reduction for the DC-link capacitors with multiple PWM strategies. An optimized positioning of the gate pulse reduces the DC-link capacitor current. The capacitor current reduction space vector PWM (SVPWM) strategies reduces the film capacitor core temperature by a maximum of 9.0°C compared to those obtained with the conventional strategies, whereas the maximum allowable temperature of the film capacitor is 105°C. The carrier-based PWM approaches also reduce the thermal stress; however, the reduction amount is not as large as the SVPWM approach. In addition to the trade-off between the implementation requirement and the reduction effect on the capacitor current, the analytical and experimental results confirm that there is a trade-off between the improved capacitor current harmonics and the worsened load current harmonics.

**Keywords**— Two-level voltage source inverter, DC-link capacitor, Thermal stress, PWM

## I. INTRODUCTION

Three-phase AC motors are widely used in both industrial and household applications [1]–[5]. The employment of film capacitors in the DC-link part of the three-phase VSI have been actively researched to absorb the current ripple due to the inverter fast switching. The maximum allowable temperature of polypropylene, which is a dielectric material of the film capacitor, is 105°C [6]; thus, the suppression of its temperature rise is important. It is possible to suppress the temperature rise of the capacitors by reducing the harmonic components of DC-link current  $i_{DC.in}$ , defined in Fig. 1.

So far, several modulation strategies of PWM inverter have been proposed for the reduction of the current stress on the DC-link capacitors [7]–[12]. In several approaches based on space vector PWM (SVPWM), the capacitor current is minimized by selecting the optimized combination of the voltage space vectors [7]–[10]. On the other hand, with approaches based on triangular carrier-based PWM, three-phase modulating signals which are shifted in every half control period also achieve the switching patterns for the capacitor current reduction [11]–[12]. Nevertheless, only the reduction effect of these PWM strategies on the capacitor current have been demonstrated in the past works, whereas the thermal stress for the DC-link capacitors with these strategies have not been evaluated yet.

This paper provides experimental evaluations and the comparison of the thermal stress for the DC-link capacitors with regard to the several PWM strategies by using the

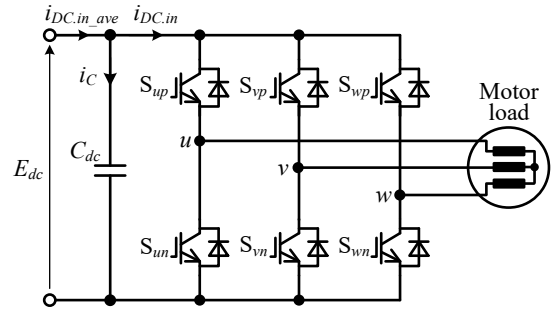


Fig. 1. Three-phase two-level VSI employed in motor drive system.

thermostatic bath, leading to fair comparisons. In addition, multilateral evaluations demonstrate that there is trade-off between the capacitor current and the output current harmonics, which can be the choice index of the capacitor current reduction PWM strategies.

This paper is organized as follows: first, the reduction methods of the DC-link capacitor current with the multiple PWM strategies are presented. Second, the effects on the DC-link capacitor current, the output phase current, and the inverter efficiency are compared by analysis and experiment. Finally, the capacitor temperature rise test is presented to confirm the effectiveness of these capacitor current reduction PWM strategies.

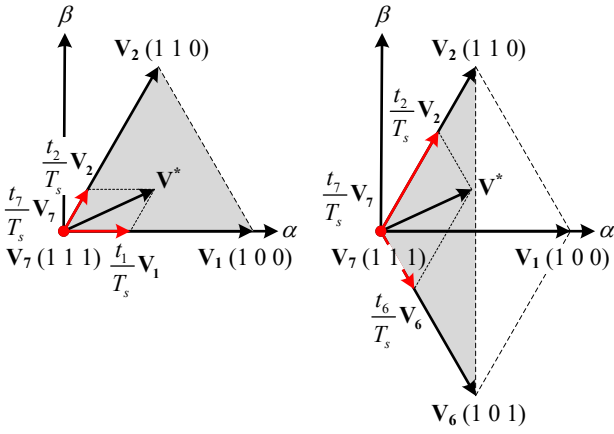
## II. PWM STRATEGIES FOR DC-LINK CAPACITOR CURRENT REDUCTION

### A. SVPWM Approaches [7]–[10]

Fig. 2 shows the conventional and the capacitor current reduction SVPWM strategies at the modulation index ( $m$ ) of 0.7, phase angle ( $\theta$ ) of 25 degrees, and the load power factor ( $\cos \phi$ ) of 0.866. Instantaneous value of the inverter input current is the superposition summation of the switched current pulses from each phase leg [13] and calculated as

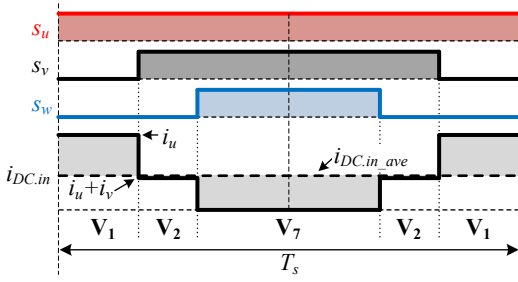
$$i_{DC.in} = \sum_{x=u,v,w} (s_x \times i_x). \quad (1)$$

The capacitor current is calculated as difference between  $i_{DC.in}$  and its average value  $i_{DC.in,ave}$  as following equation, and corresponds to the shaded areas in  $i_{DC.in}$  waveform [14].

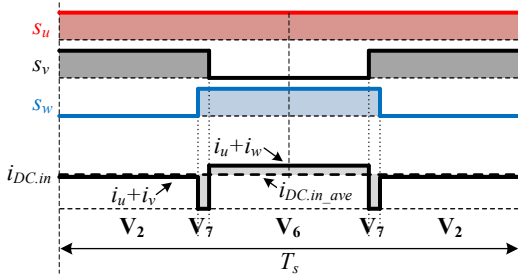


(a) Conv. SVPWM.

(b)  $i_C$  reduction SVPWM.



(c) Zoomed-in waveform of  $i_{DC,in}$  with conv. SVPWM.



(d) Zoomed-in waveform of  $i_{DC,in}$  with  $i_C$  reduction SVPWM.

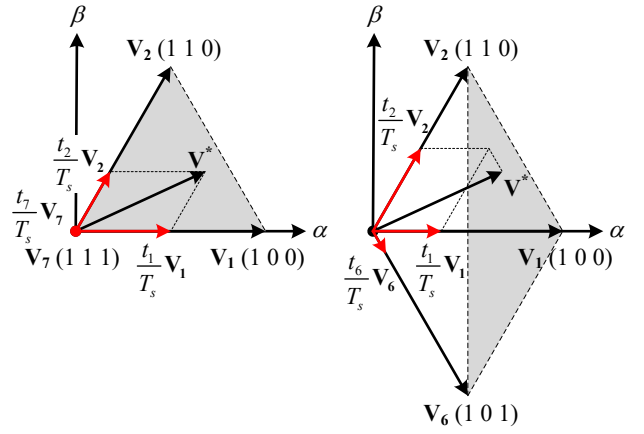
Fig. 2. Conventional and capacitor current reduction SVPWM strategies at  $m = 0.7$ ,  $\theta = 25^\circ$ ,  $\cos \varphi = 0.866$ . In low modulation index region, the two non-adjacent active vectors and one zero vector are used to reduce the capacitor current.

$$i_{C,RMS}(T_s) = \sqrt{i_{DC,in,RMS}^2(T_s) - i_{DC,in\_ave}^2} \quad (2)$$

$$\text{and} \begin{cases} i_{DC,in,RMS}(T_s) = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{DC,in}^2 dt} \\ i_{DC,in\_ave} = \frac{3}{4} m \cdot I_m \cos \varphi \end{cases}$$

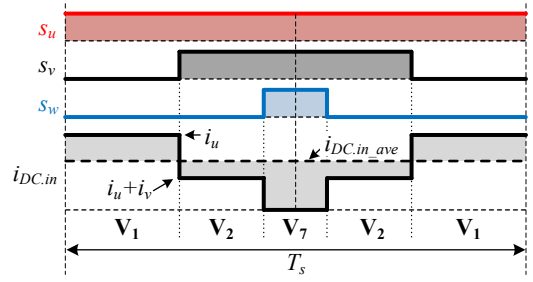
where  $T_s$  is the control period,  $I_m$  is the maximum value of the load current, and  $\varphi$  is the load power factor lagging angle. Under these conditions, the combination of one active vector ( $V_6$ ), one non-adjacent active vector ( $V_2$ ), and one zero vector ( $V_7$ ) suppresses the capacitor current to the minimum [9]–[10]. This is because this vector combination results in the omission of  $V_1$  which cause the largest error between the instantaneous value ( $= i_u$ ) and average value of DC-link current.

Fig. 3 shows another example of the conventional and the capacitor current reduction SVPWM strategies at  $m = 1.0$ , i.e. high modulation index. If the tip of the voltage reference vector  $V^*$  does not belong to the triangle formed by the tips of

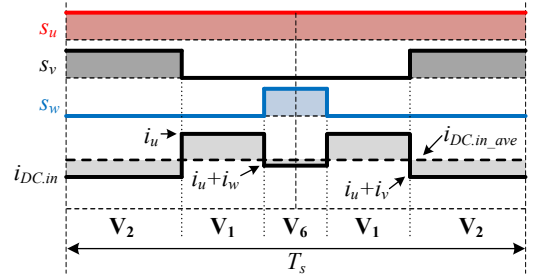


(a) Conv. SVPWM.

(b)  $i_C$  reduction SVPWM.



(c) Zoomed-in waveform of  $i_{DC,in}$  with conv. SVPWM.



(d) Zoomed-in waveform of  $i_{DC,in}$  with  $i_C$  reduction SVPWM.

Fig. 3. Conventional and capacitor current reduction SVPWM strategies at  $m = 1.0$ ,  $\theta = 25^\circ$ ,  $\cos \varphi = 0.866$ . In high modulation index region, the three consecutive active vectors are used to reduce the capacitor current.

three voltage space vectors ( $V_6$ ,  $V_2$ , and  $V_7$ ) shown in Fig. 2(b), the voltage reference vector cannot be generated by synthesizing these voltage space vectors. Under these conditions, the combination of three consecutive active vectors ( $V_6$ ,  $V_1$ , and  $V_2$ ) suppresses the capacitor current to the minimum [7]–[10]. In addition, the available areas with the three consecutive voltage space vectors are the same as those with conventional SVPWM. Therefore, the capacitor current reduction SVPWM strategy allows the same output voltage limitations as conventional SVPWM to be obtained. However, those gate pulse layout for the capacitor current reduction shown in Fig. 2(d) and Fig. 3(d) is not realized by using only one triangular-carrier. Therefore, the capacitor current reduction SVPWM leads to the requirement of high cost hardware such as field-programmable gate array (FPGA).

### B. Carrier-based Continuous PWM Approach [11]

Fig. 4 shows the modulating signals of continuous PWM (CPWM) and output phase current at  $m = 0.7$  and  $\cos \varphi = 0.866$ . The carrier-based PWM approaches generate the gate pulses by comparing the calculated modulating signals and the high-frequency carrier only with the general-purpose micro-

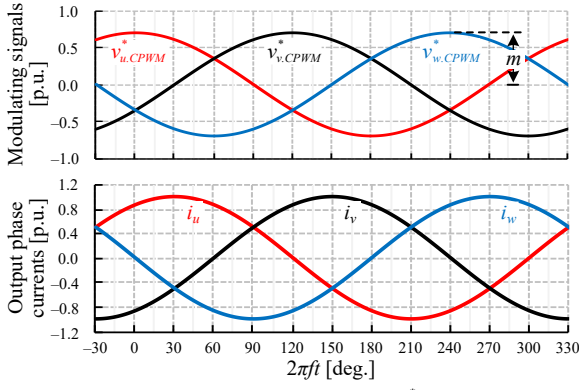


Fig. 4. Continuous modulating signals  $v_{x,CPWM}^*$  and output phase currents  $i_x$  at  $m = 0.7$  and  $\cos \varphi = 0.866$ .

computer, whereas the SVPWM approach requires FPGA. Generally, the modulating signals are set as the three-phase sinusoidal continuous waveforms as

$$\begin{cases} v_{u,CPWM}^* = m \cdot \cos(2\pi ft) \\ v_{v,CPWM}^* = m \cdot \cos(2\pi ft - 2\pi/3) \\ v_{w,CPWM}^* = m \cdot \cos(2\pi ft + 2\pi/3) \end{cases} \quad (3)$$

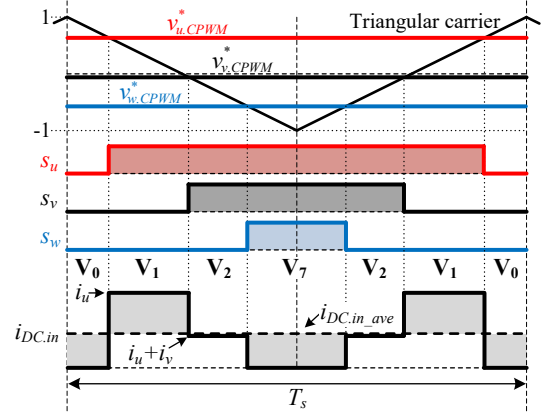
where  $m$  is the modulation index and  $f$  is the fundamental frequency.

The concept of the capacitor current reduction carrier-based PWM is realized under the premise that the modulating signals can be updated twice during one carrier cycle, which is the constraint of the micro-computer. By shifting the modulating signals in every half control period while maintaining its average value during a control period, only the gate pulse timings is adjusted while maintaining these widths. The positively-shifted modulating signal  $v_{xp}^*$  and the negatively-shifted modulating signal  $v_{xn}^*$  are calculated as

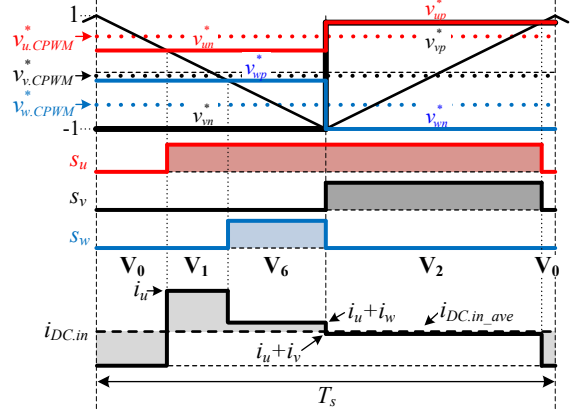
$$\begin{cases} v_{xp}^* = (2 - A_x) \cdot v_{x,CPWM}^* + A_x - 1 & (\text{if } v_{x,CPWM}^* \geq 0) \\ v_{xn}^* = A_x \cdot (v_{x,CPWM}^* - 1) + 1 & (\text{if } v_{x,CPWM}^* < 0) \end{cases} \quad (4)$$

where  $A_x$  is the shifting coefficient between the original and shifted modulating signal. The value of  $A_x$  is defined from 1.0 to 2.0.  $A_x$  of 1.0 means that the modulating signal shift is not performed.  $A_x$  of 2.0 indicates that the modulating signal is shifted maximally in linear-modulation region.

Fig. 5 shows the zoomed-in waveforms of the modulating signals, the three-phase switching functions, and the inverter input current with the conventional and capacitor current reduction continuous PWM (CPWM) strategies. For the capacitor current reduction, firstly,  $u$ -phase modulating signal should become larger than the other two phase modulating signals, and the gate pulse  $s_u$  should cover  $s_v$  and  $s_w$  in the time domain to avoid the  $i_{DC,in}$  polarity flip compared to the  $i_{DC,in,ave}$  polarity. Secondly, the overlap of the other two gate pulses  $s_v$  and  $s_w$  should be shortened to further reduce  $i_{DC,in}$  fluctuation around  $i_{DC,in,ave}$ . With those modified gate pulse timings, the applying durations of  $V_1$  and  $V_7$ , which cause the large



(a) Conventional CPWM.



(b) Capacitor current reduction CPWM.

Fig. 5. Zoomed-in waveforms of CPWM modulating signals, switching functions, and inverter input current at  $m = 0.7$ ,  $\theta = 25^\circ$ ,  $\cos \varphi = 0.866$ . The divergence degree coefficients between the original voltage references and shifted references are set as  $A_u = 1.68$ ,  $A_v = 2.00$ , and  $A_w = 2.00$ .

difference between  $i_{DC,in}$  ( $= i_u$  with  $V_1$ , or 0 with  $V_7$ ) and  $i_{DC,in,ave}$ , are shortened and eliminated compared to the conventional CPWM. Furthermore, the applying durations of  $V_2$  and  $V_6$ , which result in the small  $i_{DC,in}$  harmonics, are extended and generated with those gate pulses. In order to achieve both the criterion for avoiding the  $i_{DC,in}$  polarity flip compared to the  $i_{DC,in,ave}$  polarity and the criterion for reducing the  $i_{DC,in}$  fluctuation,

- 1)  $v_u^*$ , whose output phase current is positive, is shifted to the positive side simultaneously with the larger phase voltage reference between the other two phases, i.e.  $v_v^*$ .
- 2)  $v_v^*$  and  $v_w^*$  are shifted alternately and maximally to the positive side as long as they do not exceed  $v_{up}^*$  and  $v_{un}^*$ .

### C. Carrier-based Discontinuous PWM Approach [12]

Fig. 6 shows the modulating signals of discontinuous PWM (DPWM) and its injected zero sequence signal at  $m = 0.7$ . The discontinuous modulating signals lead to the advantages of the switching loss reduction due to the reduced switching transitions compared to those with CPWM. In addition, DPWM strategy extends the linear modulation range compared to CPWM. The discontinuous modulating signals are obtained by injecting the zero sequence signal  $v_{offset}^*$  into  $v_{x,CPWM}^*$  [15] as

$$\begin{aligned}
v_{x,DPWM}^* &= v_{x,CPWM}^* + v_{offset}^* \quad (x = u, v, w), \\
v_{offset}^* &= \begin{cases} 1 - |v_{max}| & (\text{if } |v_{max}| \geq |v_{min}|) \\ -1 + |v_{min}| & (\text{if } |v_{min}| < |v_{max}|) \end{cases}, \\
\begin{cases} v_{max} = \max[v_{u,CPWM}^*, v_{v,CPWM}^*, v_{w,CPWM}^*] \\ v_{min} = \min[v_{u,CPWM}^*, v_{v,CPWM}^*, v_{w,CPWM}^*] \end{cases}
\end{aligned} \quad (5)$$

Fig. 7 shows the zoomed-in waveforms of the modulating signals, the three-phase switching functions, and the inverter input current with the conventional and capacitor current reduction DPWM strategies. In a similar way to the CPWM approach, shifted discontinuous modulating signals, calculated as following, are used to reduce the capacitor current in the DPWM approach.

$$\begin{aligned}
\begin{cases} v_{xp}^* = 1 \\ v_{xn}^* = 2 \cdot v_{x,DPWM}^* - 1 \end{cases} & \quad (\text{if } v_{x,DPWM}^* \geq 0) \\
\begin{cases} v_{xp}^* = 2 \cdot v_{x,DPWM}^* - 1 \\ v_{xn}^* = -1 \end{cases} & \quad (\text{if } v_{x,DPWM}^* < 0).
\end{aligned} \quad (6)$$

For the capacitor current reduction, overlap period between two unclamped phases' switching functions,  $s_v$  and  $s_w$  in Fig. 7, should be shortened. Therefore, there two phase modulating signals  $v_{v,DPWM}^*$  and  $v_{w,DPWM}^*$  are shifted alternately to the positive side. As a result, the applying durations of  $V_1$  and  $V_7$ , which cause the large difference between  $i_{DC,in}$  and  $i_{DC,in,ave}$ , are shortened and eliminated. Instead of the omission of these worse switching periods for the capacitor current, the applying durations of  $V_2$  and  $V_6$ , which result in the small  $i_{DC,in}$  harmonics, are extended and generated just like CPWM approach shown in Fig. 5.

These carrier-based CPWM and DPWM approaches require only general-purpose micro-computer and FPGA is not necessary. However, the reduction effects on the capacitor current are inferior to the SVPWM approaches because the degree of freedom for the gate pulse timing is limited in the carrier-based PWM approaches. Therefore, the optimized gate pulse layout for the capacitor current reduction cannot be achieved in the carrier-based PWM approaches.

### III. ANALYTICAL RESULTS

#### A. DC-link Capacitor RMS Current

As explained in above section, the DC-link capacitor RMS current is dependent on  $m$ ,  $\varphi$ , and the switching patterns. The DC side of the three-phase VSI operates at six fold fundamental frequency; hence, the normalized DC-link capacitor RMS current is calculated based on (2) by considering only a sixth of the fundamental period as

$$I_{C,RMS(p.u.)} = \frac{1}{I_m} \sqrt{\frac{3}{\pi} \int_0^{\pi/3} \left( \sum \left[ \frac{t_k}{T_s} (i_{DC,in,k} - i_{DC,in,ave})^2 \right] \right) d\theta} \quad (7)$$

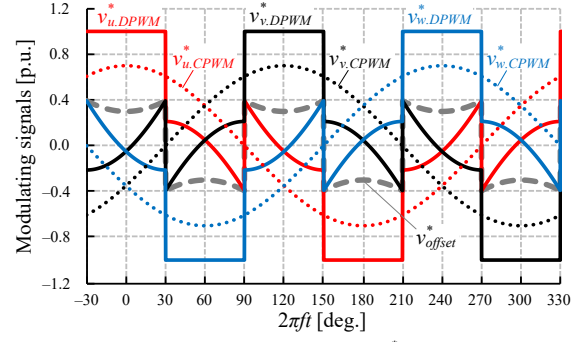
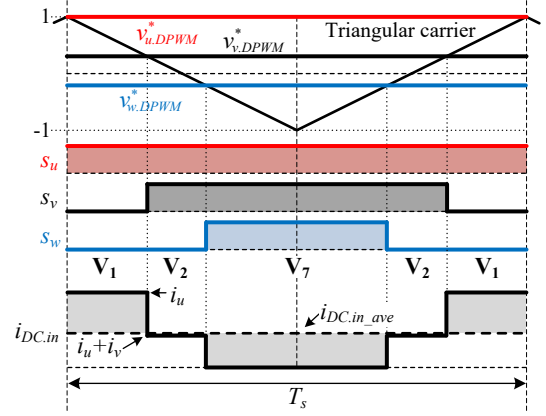
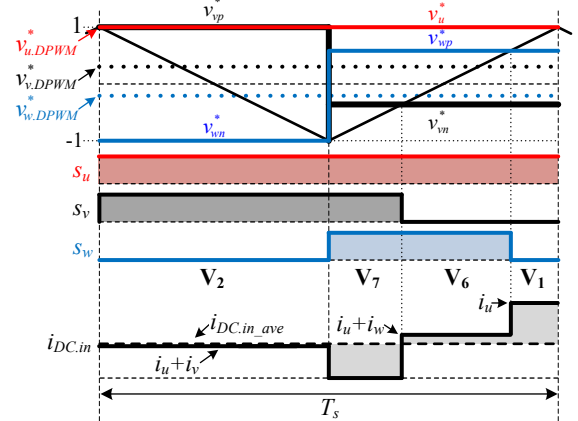


Fig. 6. Modulating signals of DPWM  $v_{x,DPWM}^*$  and its injected zero sequence  $v_{offset}^*$  signal at  $m = 0.7$ .



(a) Conventional DPWM.



(b) Capacitor current reduction DPWM.

Fig. 7. Zoomed-in waveforms of DPWM modulating signals, switching functions, and inverter input current at  $m = 0.7$ ,  $\theta = 25$  deg.,  $\cos \varphi = 0.866$ .

where  $t_k$  is the on-duty of VSI voltage space vector  $V_k$  ( $k = 0 \sim 7$ ) within  $T_s$ , and  $i_{DC,in,k}$  is the instantaneous DC-link current value with the voltage space vector  $V_k$ .

Fig. 8 shows the comparisons of the DC-link capacitor RMS current under the high load power factor conditions. Both figures confirm that there are no  $I_{C,RMS(p.u.)}$  differences between the conventional SVPWM, CPWM, and DPWM due to those same applying durations of the active vectors and the zero vectors. Fig. 8(a) confirms that the capacitor current reduction SVPWM leads to the best reduction effect in the modulation index region from 0.6 to 0.8 under the unity load power factor condition, which is a typical operating condition of the grid-tied VSI. Within the carrier-based PWM approaches, the capacitor current reduction DPWM leads to the better reduction effect compared to the CPWM approach.

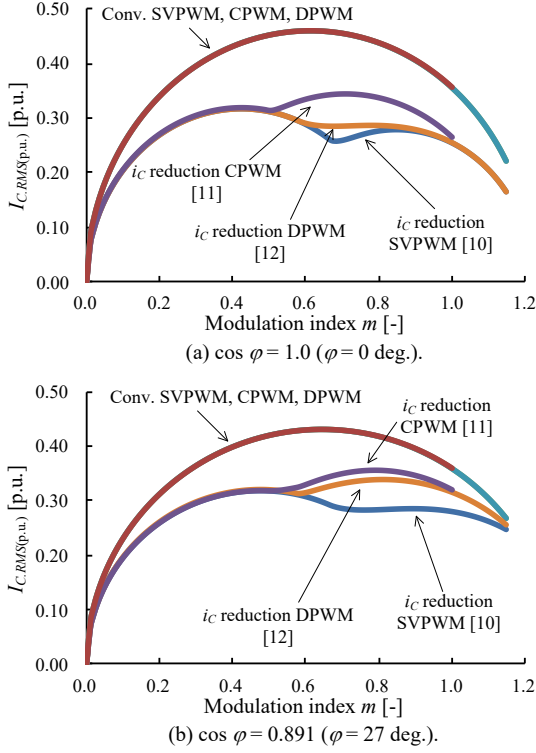


Fig. 8.  $I_{C,RMS(p.u.)}$  comparisons between conventional and capacitor current reduction PWM strategies against different modulation index at high load power factor conditions.

This is because the fact that certain one phase discontinuous modulating signal is always clamped, making it possible to set the switching pattern which leads to the smaller  $i_{DC,in}$  ripple longer than CPWM approach. Fig. 8(b) demonstrates the after-mentioned experimental condition of  $\cos \varphi = 0.891$  with an induction motor load. This trend in the reduction effect between the three capacitor current reduction PWM approaches is clearly shown also in this condition.

### B. Load Current Quality

In order to evaluate the load current quality, the concept of harmonic flux presented in [16] is used. Assuming that the motor switching frequency model is an inductance  $L$ , a harmonic flux load current vector  $\mathbf{I}_h$  has a proportional relationship between the harmonic flux vector  $\lambda_h$  (time integral of the instantaneous error voltage vector) as

$$\lambda_h = L \mathbf{I}_h = \int_{NT_s}^{(N+1)T_s} (\mathbf{V}_k - \mathbf{V}^*) dt. \quad (8)$$

Fig. 9 shows the harmonic flux vector trajectories at  $m = 0.7$ ,  $\theta = 25$  degrees. The distance between the trajectories and the origin ( $o$ ), which is the initial value of  $\lambda_h$  at the beginning of the carrier cycle, corresponds to the magnitude of the harmonic flux [16]. The calculation of (8) and Fig. 9 evaluate the ripple current on a per-carrier cycle base. Since the harmonic flux vector characteristic has six-fold space symmetry, the per-fundamental cycle (per 60 degrees in space) harmonic flux RMS value, which characterizes the load current quality and the harmonic losses in the test motor, is calculated as follows.

$$\lambda_{RMS} = \sqrt{\frac{3}{\pi} \int_0^{\pi/3} \int_{NT_s}^{(N+1)T_s} \|\lambda_h\|^2 dt d\theta}. \quad (9)$$

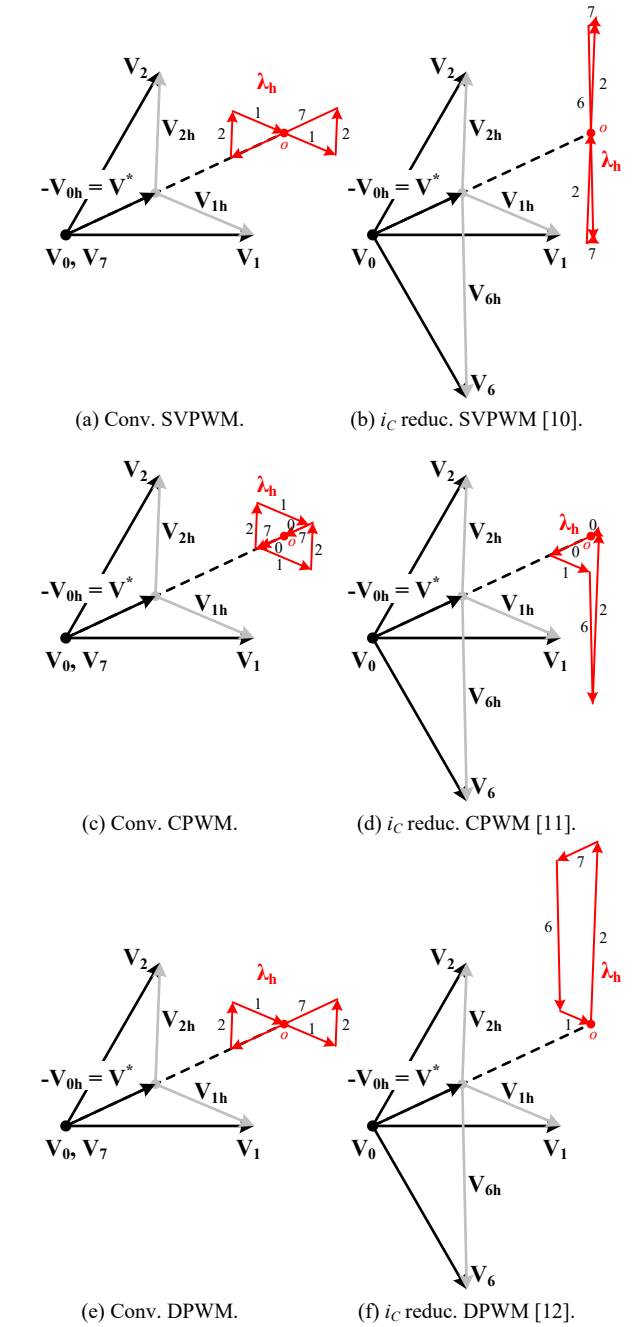


Fig. 9. Harmonic flux vector  $\lambda_h$  trajectories at  $m = 0.7$  and  $\theta = 25$  degrees. The distance between the trajectories and the origin ( $o$ ), which is the initial value of  $\lambda_h$  at the beginning of the carrier cycle, corresponds to the magnitude of the harmonic flux.

Fig. 10 shows the comparison of the harmonic flux RMS values. Figs. 9–10 confirm that the capacitor current reduction PWM strategies worsen the harmonic flux compared to those obtained with each conventional PWM strategies. The reason is because the capacitor current reduction PWM strategies result in the application of the voltage space vector which is not the closest to  $\mathbf{V}^*$ , i.e.  $\mathbf{V}_6$  in Fig. 9. Within the capacitor current reduction PWM strategies, the SVPWM approach leads to the worst harmonic flux RMS value, and the carrier-based CPWM approach leads to the minimal deterioration.



This trend in the worsened harmonic flux RMS value with the capacitor current reduction PWM strategies is in a trade-off relationship with the trend in the improved DC-link capacitor RMS current which is shown in Fig. 8.

#### IV. EXPERIMENTAL RESULTS

Fig. 11 shows the experimental setup. The DC-link capacitor and the inverter, operated at the switching frequency of 10 kHz, are placed inside thermostatic bath, whereas the temperature test starts from 25°C.

Fig. 12 shows the film capacitor under test as the DC-link capacitor. The thermocouple is built in the central part of the film capacitor. An equivalent series resistance (ESR) is measured using HIOKI 3532-50 LCR tester. At very low frequencies, ESR is high due to prevalent leakage. At low frequencies, ESR is dominated by the dielectric losses which decrease in inverse proportion to the frequency. At medium to high frequencies, the losses in the conductors are dominant and ESR becomes relatively constant. At high frequencies, ESR increases again due to the skin effect [17].

Fig. 13 shows the inverter operating test results with each modulation method. All capacitor current reduction PWM strategies reduce the switching frequency harmonics of the capacitor current compared to conventional strategies. Furthermore, the capacitor loss, which is calculated as follows, is also reduced.

$$P_{Cap} = \sum_{n=1} \left( R_{ESR,n} \cdot i_{Cap,n}^2 \right). \quad (10)$$

The maximum  $P_{Cap}$  reduction of 54.2% is obtained by the SVPWM approach as observed in Figs. 13(a)–(b). The reduction effects on  $P_{Cap}$  with the capacitor current reduction PWM strategies are correspond with the analytical results of  $I_{C,RMS(p.u.)}$  shown in Fig. 8(b).

Fig. 14 shows the measured capacitor core temperature. The temperature tests are conducted until the bath internal temperature reached 60°C, the rated temperature of the coated vinyl of wire, under the same experimental conditions as in Fig. 13. The largest reduction of  $P_{Cap}$  with the SVPWM approach, which can be observed from Figs. 13(a)–(b), enables the greatest suppression of the capacitor core temperature rise. The application of the capacitor current reduction SVPWM reduces the equilibrium capacitor core temperature, which is estimated by the least-square method, by 11°C at most compared to the conventional strategy.

Table 1 lists the inverter efficiency with each PWM strategies under same experimental conditions as in Fig. 13. The CPWM strategies lead to the worst efficiency due to the requirement of more number of switching transitions. In addition, the SVPWM and DPWM strategies result in almost same efficiency because the number of switching transitions is same.

Fig. 15 shows the harmonic spectrum of  $i_u$  under the same experimental conditions as in Fig. 13. All capacitor current reduction PWM strategies worsen the phase current THD compared to the conventional PWM strategies because of the instantaneous error between the voltage reference vector and the output voltage vector. This trend is similar to the analytical results of  $\lambda_{RMS}$  shown in Fig. 10. In particular, the capacitor

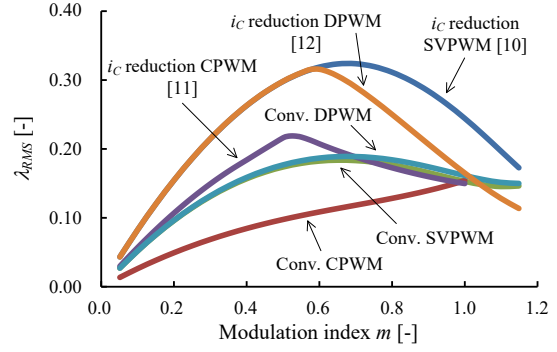


Fig. 10. Comparison of harmonic flux RMS values  $\lambda_{RMS}$ .

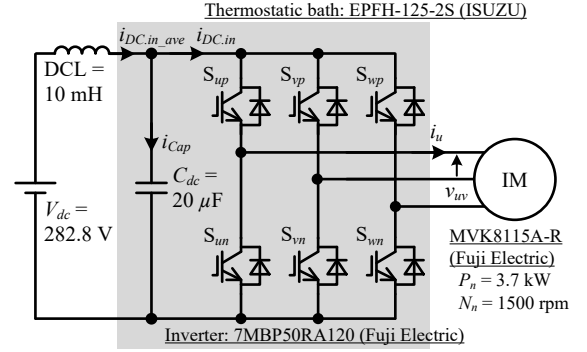
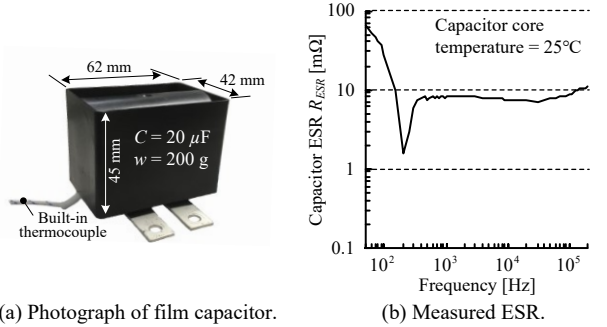


Fig. 11. Experimental setup.



(a) Photograph of film capacitor.  
Fig. 12. Film capacitor under test.

current reduction SVPWM leads the largest time integral of the instantaneous voltage error and the worst current THD.

#### V. CONCLUSION

This paper demonstrated the thermal stress reduction for the DC-link capacitors with multiple PWM strategies. The SVPWM approaches realized the optimal gate pulses for the capacitor current reduction with FPGA, and reduced the capacitor core temperature by 9.0°C at most compared to the conventional strategies. On the other hand, the optimal gate pulses generation led to the large instantaneous inverter voltage error; thus, the capacitor current and the output current harmonics have the trade-off relationship. The carrier-based PWM approaches, which do not require FPGA, realized the intermediate performances on the capacitor current and the output current harmonics between the conventional PWM strategies and the capacitor current reduction SVPWM.

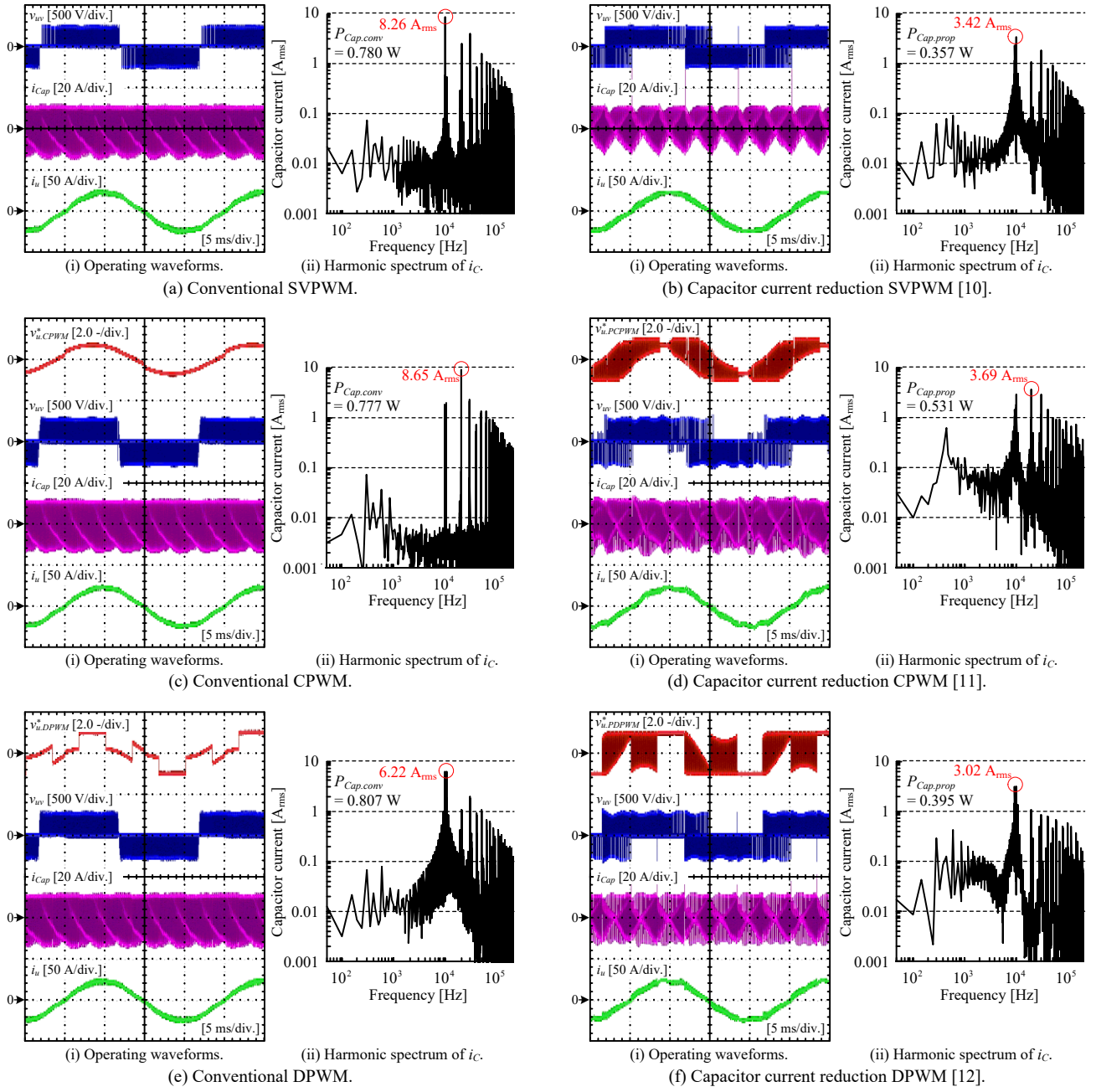


Fig. 13. Experimental results at  $m = 0.643$ ,  $\cos \varphi = 0.891$ , and  $P_{inv} = 2.7$  kW.

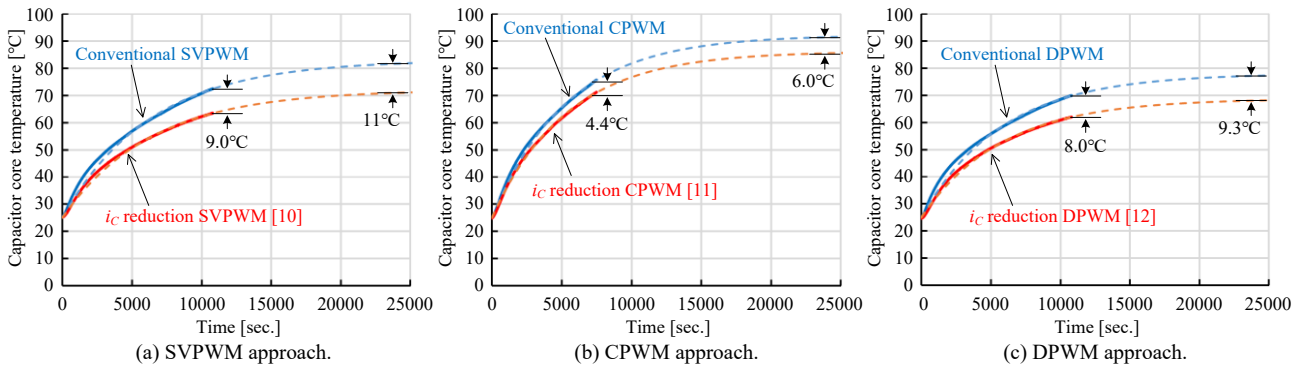


Fig. 14. Measured capacitor core temperature and its approximated curves. The experimental conditions are at  $m = 0.643$ ,  $\cos \varphi = 0.891$ , and  $P_{inv} = 2.7$  kW, under same conditions in Fig. 13.

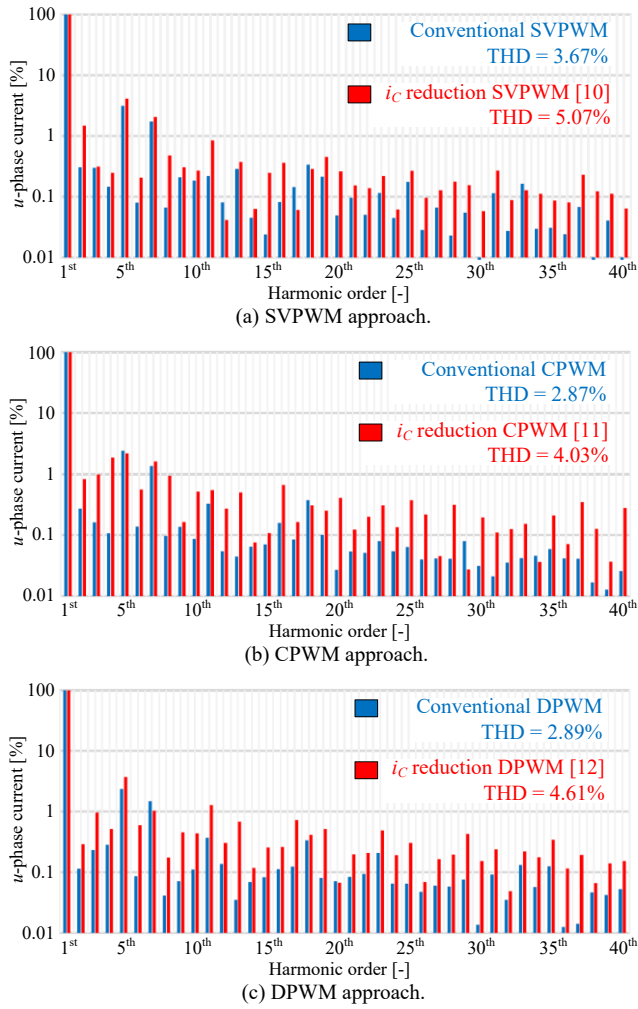


Fig. 15.  $i_u$  harmonic spectrum and its THD at  $m = 0.643$ ,  $\cos \phi = 0.891$ , under same conditions in Fig. 13.

TABLE I. MEASURED INVERTER EFFICIENCIES

	Conv.	$i_c$ reduction	Conv.	$i_c$ reduction	Conv.	$i_c$ reduction
	SVPWM	SVPWM [10]	CPWM	CPWM [11]	DPWM	DPWM [12]
Efficiency [%]	96.11	96.39	95.27	95.17	96.30	96.22

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