Multi-port Converter with Square-wave-voltage Multilevel Converter and Active Power Filter Connected in Series

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***Abstract*—This paper proposes a multi-port converter, which has multiple power sources with a buck converter or inverter connected in series, with an active power filter for a reduction of power conversion loss and circuit volume of an energy storage system. The proposed circuit consists of a multilevel converter, a series-active power filter, and an unfolder. In the proposed circuit, the number of inductors is reduced from four to two compared to the conventional circuit. Moreover, the proposed circuit reduces harmonic components of output voltage with a multilevel topology in order to reduce the volume of a filter inductor. In addition, a voltage control system is proposed for the converter to regulate the capacitor voltage of the active power filter. It is demonstrated that a 1-kW prototype circuit with Si-MOSFETs achieves a maximum efficiency of 99.3%. Furthermore, the capacitor voltage is regulated to constant even when the load power is stepped from no-load to full load.**

Keywords— Multi-port converter, Multilevel DC-AC converter, Series-active power filter, Constant capacitor voltage control

I. INTRODUCTION

In recent years, fuel cell (FC) systems are widely studied due to its high energy efficiency. However, the response of the output power of FC is typically slow against load fluctuation. In order to overcome the load fluctuation, auxiliary energy storage systems using batteries or double-layer capacitors are typically required [1]. In general, a power conversion system is employed in a grid-tied inverter with boost-up converters and a DC-AC converter to connect FC and the battery to the single-phase grid system [2]. However, this power conversion system faces several problems which are the increase in the power conversion loss and the circuit volume due to the boost and filter inductors. In particular, a reduction of the boost and filter inductors is required.

Multi-port converters have been proposed to reduce the conversion loss and the circuit volume [3–5]. In Ref. [4], two DC input ports are connected in series in order to achieve a DC-DC conversion with one inductor. However, the multiport converters still require a DC-AC converter with the AC grid connection. Thus, the interconnecting inductor in the DC-AC converter is still needed. Meanwhile, in Ref. [5], the converter consists of two DC input ports and an AC output port. However, the DC-link voltage must be higher than the maximum voltage of the output AC voltage, leading to the requirement of the high voltage rating devices. Consequently, the high switching frequency to reduce the circuit volume is limited due to the decrease in efficiency.

Besides, multilevel DC-AC converters have been proposed to reduce the harmonic components [6–12]. For instance of the multilevel topologies, such as a neutral point clamped converter [9] and flying-capacitor converter [10] are studied. However, the multilevel topologies increase switching loss because each device is operated with PWM. In [11–12], the multilevel voltage waveform is obtained by the cascade connection of the full-bridge cells. In the cascade-connected full-bridge cell topology, the full-bridge cells have to have an isolated power supply at DC side. Thus, circuit volume is increased by isolate power supplies, e.g., isolation transformer with the converter. However, the number of output voltage levels is limited due to the number of full-bride cells. Consequently, cascade-connected full-bridge cell topology has a relationship between circuit volume and number of output voltage levels. Moreover, the topology increases switching loss since each cell is operated with PWM.

This paper proposes a multi-port DC-AC converter which reduces both the circuit volume and the power conversion loss. The original idea of this paper is that each converter of the input port is connected in series. In addition, the active filter is connected in series with FC and the battery converters with square-wave-operation in order to form a multilevel topology. So, the circuit volume of the power converter is reduced. Moreover, the harmonic components of the output voltage is reduced by the multilevel topology. In the proposed circuit, capacitors are used at a DC-link of the active power filter in order to increase the number of voltage level without isolation power supplies. In addition, the power density of the proposed circuit is compared with the conventional topology through a Pareto front optimization. Finally, the operation of the proposed circuit is demonstrated in the experiment. The prototype circuit achieves a maximum efficiency of 99.3% at

90% of rated power. Besides, the operation of the proposed circuit is verified under the fluctuation of the capacitor initial voltage and the DC-link voltage.

II. Circuit Topology and Capacitor Voltage Control Method

A. Circuit Configuration and Operation Principle

Figure 1 shows the conventional circuit, which consists of a DC-AC converter and two boost-up converters, one of which is connected to FC, whereas the other is connected to auxiliary energy storage systems. Consequently, the conventional circuit requires at least three main inductors L_1, L_2, and L_3. These inductors can be minimized by the design of high switching frequency. Nevertheless, the increase in the switching frequency of the high voltage rating switches in the conventional circuit leads to a decrease in efficiency.

Figure 2 shows the proposed circuit. The proposed circuit consists of a square-wave-voltage multilevel converter, an active power filter, and an unfolder. Furthermore, the square-wave-voltage multilevel converter consists of the two cells (cell A and B), and the active filter consists of the two cells (cell C and D).

Figure 3 shows the operating principle of the proposed circuit. Fig. 3 (a) shows the input voltage of the unfolder and the output voltage of the cell A and cell B, whereas Fig. 3 (b) shows the operation waveforms of the active power filter output voltage. In Fig. 3 (a), the square-wave-voltage multi-level converter outputs four level voltages, which are synchronized with full-wave rectification of the grid voltage. In Fig. 3 (b), the series active filter compensates the harmonic components of the four-level voltages, which are output by the cell A and the cell B. Consequently, the square-wave-voltage multilevel converter and the active filter output full-wave rectified waveform. Next, the unfolder converts the full-wave-rectification voltage waveform into the sinusoidal voltage waveform, i.e., the switching frequency of twice the grid frequency. Therefore, the converter loss is significantly reduced by the proposed circuit due to the low switching frequency of the unfolder and the employment of the low voltage rating devices. In addition, the inductor volume is also reduced because the voltage applied to the inductor is only the difference between the grid voltage and multilevel square wave voltage.

B. Voltage Conditions of Fuel Cell and Battery

Figure 4 (a) shows the circuit configuration of the DC-AC converter by cell connection topology and single-phase inverter. Note that the general single-phase PWM inverter without active power filter shown in Fig. 4 (a) is assumed in this consideration. The cell A and the cell B are required to supply the maximum instantaneous power when the system has no active power filter. So, the voltage condition of the cell A and the cell B DC link voltage are expressed as

$$V_{out\_peak} \le E_A + E_B \quad (1),$$

where V_{out_peak} is the maximum voltage of the output voltage, E_A is cell A DC-link voltage, E_B is cell B DC-link voltage. According to (1), the total voltage of cell A and B should be higher than the maximum voltage of the grid voltage.

Figure 4 (b) shows the circuit configuration of the DC-AC converter by cell connection topology and single-phase

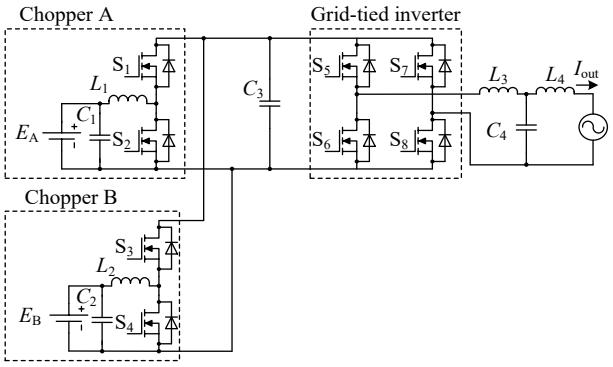


Fig. 1. Conventional circuit.

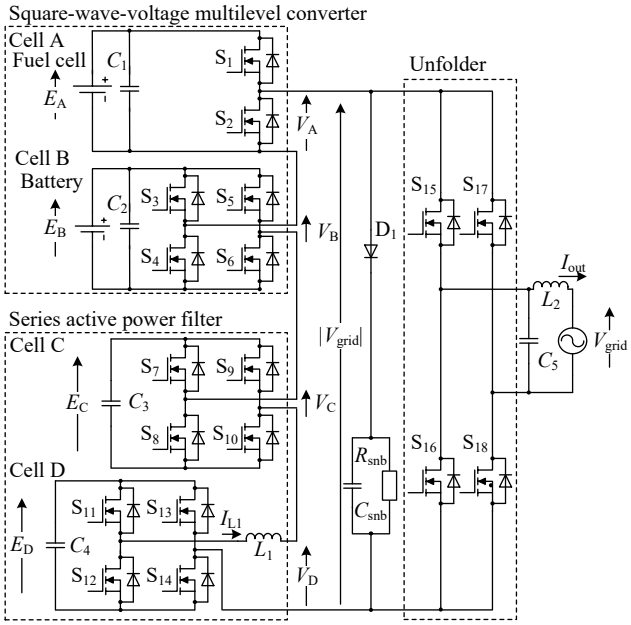
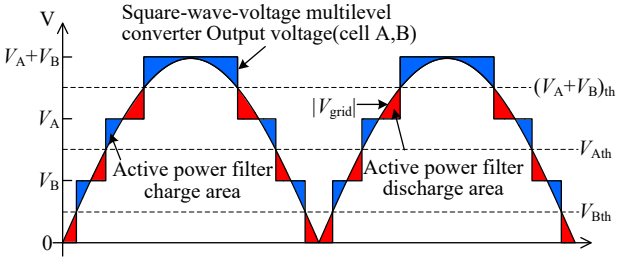
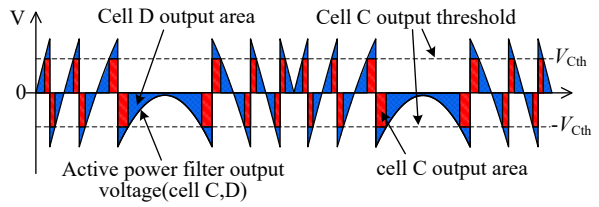


Fig. 2. Proposed circuit.



(a) $|V_{grid}|$ and Cell A, B output voltage



(b) Cell C and active filter output voltage

Fig. 3. Conceptual diagram of the proposed circuit operation.

inverter with the active power filter. The voltage condition of the cell A, cell B, and active power filter are expressed as

$$V_{out\_peak} \le E_A + E_B + E_C \quad (2),$$

where E_C is the DC-link voltage of the active power filter. Note that (2) is instaneous condition. Thus, inverter with active power filter is not output V_{out_peak} in continuity. The input power must be equal to the output power of the active power filter in order to keep the capacitor voltages. In addition, the DC-link voltage of the cell A should be twice the cell B voltage. The output voltage is three levels when the voltage of the cell A is equal to that of the cell B. On the other hand, the voltage of the active power filter is high when the voltage of the cell A is higher than twice the voltage of the cell B. In the active filter, the capacitor voltage of the active filter should be high enough in order to compensate for harmonic components by the cell A and cell B. So, the voltage condition of the cell C and cell D capacitor voltage is shown as

$$(E_A - E_B) \le E_C \quad (3),$$

where E_C is the capacitor voltage of the active power filter. Furthermore, the constant capacitor voltage control is required to achieve stable operation, which is carried out by the capacitor voltage balance control and the average control.

C. Control System of the Proposed Circuit

Figure 5 shows the block diagram of the inductor current control of the cell D. There are two main control objectives in the proposed circuit: the sinusoidal grid current and the constant capacitor voltages. The current output of the cell A–D should be full-wave rectified waveform. Then, the unfolder converts the full-wave rectified current output by the cell A–D. The capacitor voltage regulation is explained as follows.

Figure 6 shows the capacitor voltage control of the proposed circuit. Fig. 6(a) shows the total voltage control of the cell C and cell D, whereas Fig. 6(b) shows that the capacitor voltage balance control of the cell C and cell D. In the total voltage control, the total capacitor voltage of E_C and E_D is regulated. In particular, the outputs of the total voltage control system, i.e., the V_{Bth}, V_{Ath}, and $V_{(A+B)th}$, are controlled to match the area colored by red and the area colored by blue in Fig. 3(a). In the capacitor voltage balance control, the cell C outputs V_{Cth} to match the red area in Fig. 3(b). On the other hand, the cell D outputs V_{Dth} to match the blue area in Fig. 3(b). The total voltage control system regulates the sum of the capacitor voltages in the cell C and cell D, whereas the balance voltage control ensures the same capacitor voltage in the cell C and cell D. As a result, the capacitor voltages in the cell C and cell D becomes constant.

III. Power Density Comparison between Conventional and Proposed Circuit

A. Losses of power devieces and inductor

This chapter discusses the efficiency and the power density. The proposed topology shown in Fig. 2 is compared to the conventional topology shown in Fig. 1.

Table I shows the parameters of the loss and circuit volume analysis. In this consideration, the power losses by the power semiconductors and the copper loss of the inductor are calculated. It assumes that the iron loss of the inductor can be neglected because the inductor is designed to let its current ripple low. The conduction loss of the power semiconductor

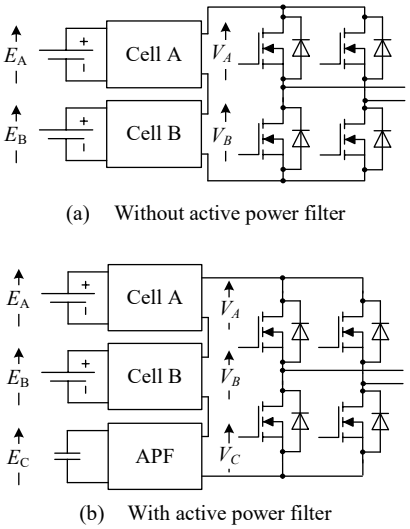


Fig. 4. Circuit configuration of the two power supply inverter.

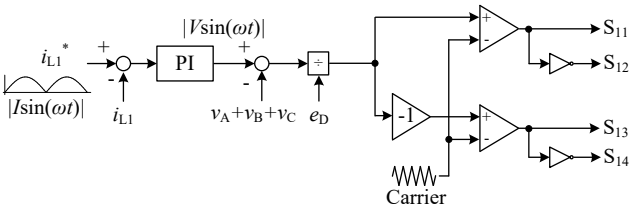
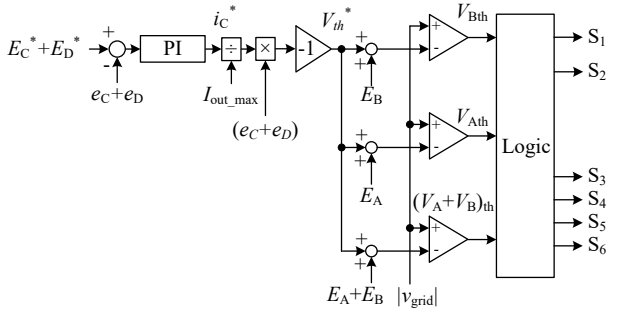
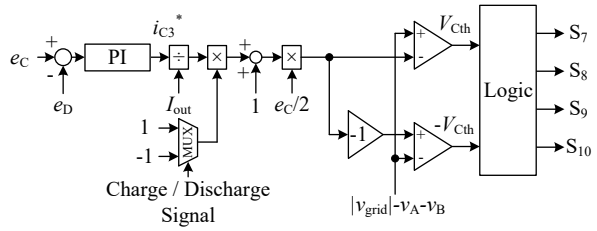


Fig. 5. Block diagram of the output current control.



(a) Total voltage control of capacitor voltages



(b) Balance control of capacitor voltages

Fig. 6. Capacitor voltage control system.

is calculated by the on-resistance of the devices and the RMS value of the device current. So, conduction loss of device P_{con} is shown as

$$P_{con} = R_{on} I_{rms}^2 \quad (4),$$

TABLE I. PARAMETERS OF THE LOSS AND CIRCUIT VOLUME.

Rated power		1 kW	Fuel cell voltage	190 V
Output voltage		200 V	Fuel cell output power	730 kW
Output current		5 A	Battery voltage	95 V
Output frequency		50 Hz	Battery output power	270 W
Switching device	Proposed circuit	Cell A	600 V MOSFET, R_{DS}=15 mΩ IPW65R019C7(Infineon)	
		Cell B	200 V MOSFET, R_{DS}=9.9 mΩ IPP110N20N3(Infineon)	
		Cell C Cell D	60 V MOSFET, R_{DS}=2.1 mΩ IPI120N06S4-H1(Infineon)	
		Unfolder	600 V MOSFET, R_{DS}=15 mΩ IPW65R019C7(Infineon)	
	Conventional circuit		600 V MOSFET, R_{DS}=15 mΩ IPW65R019C7(Infineon)	
	Switching loss IPB200N15N3G (Infineon)	Turn ON	0.97 μJ (at 34 V, 20 A)	
		Turn OFF	5.63 μJ (at 34 V, 20 A)	
Heatshink			CSPI 3.0	
Capacitor	Proposed circuit	Cell A	KXG series (Nippon chemi-con) 350 V, 150 μF, 4 parallel	
		Cell B	KXG series (Nippon chemi-con) 160 V,330 μF, 3 parallel	
		Cell C, Cell D	GXF series (Nippon chemi-con) 50 V, 300 μF	
	Conventional circuit	Chopper A	GXF series (Nippon chemi-con) 400 V, 68 μF ~ 12 μF	
		Chopper B	KXG series (Nippon chemi-con) 160 V, 68 μF ~ 51 μF	
		DC-link	RWF series (Nippon chemi-con) 400 V, 1000 μF	
Inductor	Ripple current		10 %	
	Window utilization factor		0.3	
	Flux density		0.3 T	
	Current density		3 A/mm^2	

where R_{on} is the on-resistance of the device, I_{rms} is the RMS value of the device current. In the proposed circuit, I_{rms} is full-wave rectified waveform because the inductor current is controlled by the inductor current controller of Fig. 5. In the conventional circuit, I_{rms} is the average current of the inductor and the sinusoidal waveform current of the DC-AC converter outputs. The switching loss is measured by switching test of the Si-MOSFET IPB200N15N3G (Infineon). Note that switching loss of each device is assumed that switching loss of each device is in proportion to an applied voltage and device current. The switching loss P_{switch} is shown as

$$P_{switch} = \left(\frac{I_{ave}}{I_{mon}} \frac{V_{dc}}{V_{mon}} e_{on} + \frac{I_{ave}}{I_{moff}} \frac{V_{dc}}{V_{moff}} e_{off} \right) f_{sw} \quad (5),$$

where e_{on} is turn-on loss, e_{off} is turn-off loss, I_{ave} is the average current, V_{dc} is applied voltage of device, V_{mon}, V_{moff}, I_{mon}, and I_{moff} are switching test voltage and current described in a datasheet, f_{sw} is the switching frequency. In the proposed circuit, the switching loss of the cell A, B, and C is neglected because the switching is several times during one grid cycle. The power loss of the inductor under the same core is calculated from winding length. In addition, AC resistance by skin effect is calculated. The cupper loss of inductor is shown as

$$P_L = I_{rms}^2 R_{wdc} + I_{ripple}^2 R_{wac} \quad (6),$$

where R_{wdc} is DC resistance of winding, R_{wac} is AC resistance considering a skin effect, I_{ripple} is current ripple.

B. Circuit volume

The considered volume of the circuit comes from the heatsink, the inductor, and the capacitor. The volume of the heatsink is calculated based on the Cooling System Performance Index (CSPI) [13–14]. CSPI is a value showing the thermal resistance per unit volume, which is expressed by

$$CSPI = \frac{1}{R_{th(s-a)} Vol_H} \quad (7),$$

where $R_{th(s-a)}$ is the thermal resistance of the heatsink, and Vol_H is the volume of the heatsink. The volume of the heatsink is determined by CSPI and the required thermal resistance of the heatsink from the junction temperature of the switching devices. Besides, thermal resistance $R_{th(s-a)}$ is shown as

$$R_{th(s-a)} = \frac{T_j - T_a}{P_{con} + P_{switch}} - R_{th(j-s)} \quad (8),$$

where $R_{th(j-s)}$ is the thermal resistance of the junction to the heatsink in K/W, T_j is the junction temperature of the device, and T_a is the ambient temperature [13].

The volume of the inductor Vol_L is calculated by Area Product [15]. Note that the required inductance is determined by the inductor ripple current. The volume of the inductor is given by

$$Vol_L = K_v \left(\frac{2W_L}{K_u B_m J_w} \right)^{\frac{3}{4}} \quad (9),$$

where K_v is the constant value which is determined by the shape of the core, K_u is the window utilization factor, B_m is the flux density, J_w is the current density, W_L is maximum energy of the inductor. The volume of the inductor is determined by the maximum energy of the inductor with K_v, K_u, B_m, and J_W are kept constant.

The capacitance is decided by the ripple current. The capacitor is selected based on the standard of the capacitor manufacturer. In particular, the volume of the capacitor is calculated by the dimension provided in the datasheet.

Figure 7 shows the switching loss and device conduction loss characteristics of the proposed circuit and the conventional circuit with varying the switching frequency from10 kHz to 100 kHz. The device loss of the proposed circuit is smaller than the conventional circuit at over 20 kHz because of the low switching loss.

Figure 8 shows the loss distribution of the proposed circuit and conventional circuit at 10 kHz and 100 kHz switching frequency. In the proposed circuit, conduction loss of the device is dominant because the high number of the conduction devices. However, switching loss of the proposed circuit is lower than the conventional circuit because the cell D (PWM cell) is low voltage. In addition, copper loss of inductor is

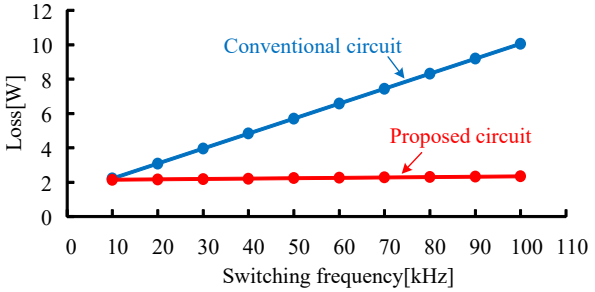


Fig. 7. Operation waveform with capacitor voltage control

TABLE II. EXPERIMENTAL CONDITIONS.

Parameter		Symbol	Value
Output power		P_{out}	1 kW
Grid voltage		V_{grid}	200 V
Grid output current		I_{out}	5 A
Grid frequency		f_{grid}	50 Hz
Condition (I)	Cell A voltage	E_A	190 V
	Cell B voltage	E_B	95 V
Condition (II)	Cell A voltage	E_A	172 V
	Cell B voltage	E_B	84 V
Condition (III)	Cell A voltage	E_A	185 V
	Cell B voltage	E_B	68 V
C_3 capacitor voltage		E_C^*	32 V
C_4 capacitor voltage		E_D^*	32 V
Cell C capacitor		C_3	3300 μF (H=1.69 ms)*1
Cell D capacitor		C_4	3300 μF (H=1.69 ms)*1
Step down inductor		L_1	1.57 mH (%Z=1.2%)*2
Snubber capacitor		C_{snb}	4.4 μF
Snubber resistance		R_{snb}	47 kΩ
PWM Carrier Frequency		f_{sw}	20 kHz
PI1	Response	f_{PI1}	2 kHz
	Danping factor	ζ_{PI1}	0.7
	Propotional gain	K_{P1}	27.6
	Integral time	T_{i1}	111 μs
PI2	Response	f_{PI2}	10 Hz
	Danping factor	ζ_{PI2}	0.7
	Propotional gain	K_{P2}	0.15
	Integral time	T_{i2}	22.2 ms
PI3	Response	f_{PI3}	10 Hz
	Danping factor	ζ_{PI3}	0.7
	Propotional gain	K_{P3}	0.29
	Integral time	T_{i3}	22.2 ms

*1 H : unit capacitance constant[17] based on an output average current I_{out_ave} and a capacitor voltage(V_{C3}^* or V_{C4}^*).
*2 %L based on an output voltage V_{out}, an output current I_{out}, and an output frequency f_{out}.
*3 Proportional gain based on an output voltage V_{out}, an output current I_{out}.

reduced in high frequency due to a reduced number of the turn of small inductance. From the above reasons, the power loss reduced by up to 74.1% at the switching frequency of 100 kHz.

Figure 9 shows the Pareto front curves of the proposed circuit and the conventional circuit. The Pareto front curve shows the trade-off between two parameters, which are the efficiency and the power density in this paper [16]. Note that the switching frequency is varied from 10 kHz to 1 MHz in the conventional circuit, 10 kHz to 10 MHz in the proposed circuit. As shown in Fig. 9, both the efficiency and the power density of the proposed circuit are higher than the conventional circuit at the same switching frequency because the low switching loss and the inductor current ripple reduction due to the multi-level characteristic.

IV. EXPERIMENTAL RESULTS

Table II shows the condition of the experiments. The fundamental operation of the proposed circuit and capacitor voltage control ware verified by a 1.0-kW prototype with Si-MOSFETs. In the experiment, the resistance load is connected at the output. Note that each voltage condition of (I)–(III) is applied to the cell A and cell B in the experiment.

Figure 10 shows the operation waveforms at the steady state at the rated output power. The cell A and cell B output square-wave-voltage waveform. The cell C and cell D output difference between the sinusoidal waveform and square-

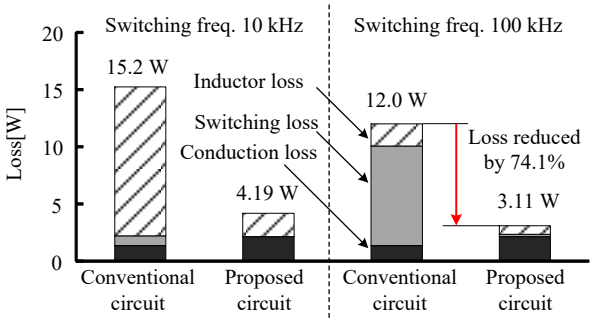


Fig. 8. Loss distribution of the proposed circuit and conventional circuit.

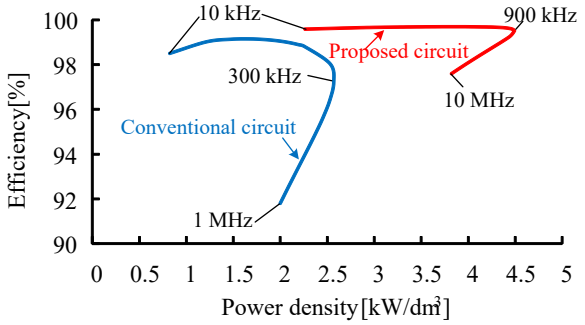


Fig. 9. Pareto front curve of the proposed circuit and conventional circuit.

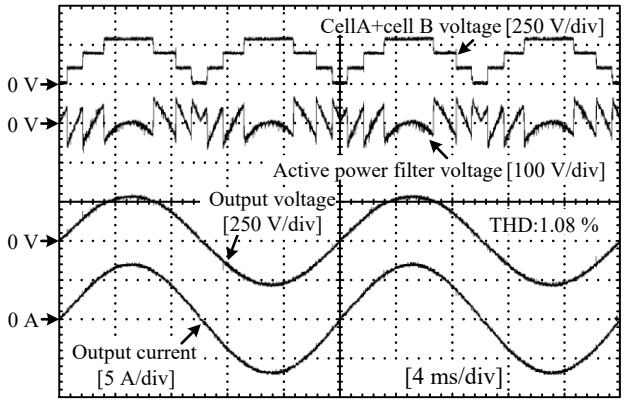
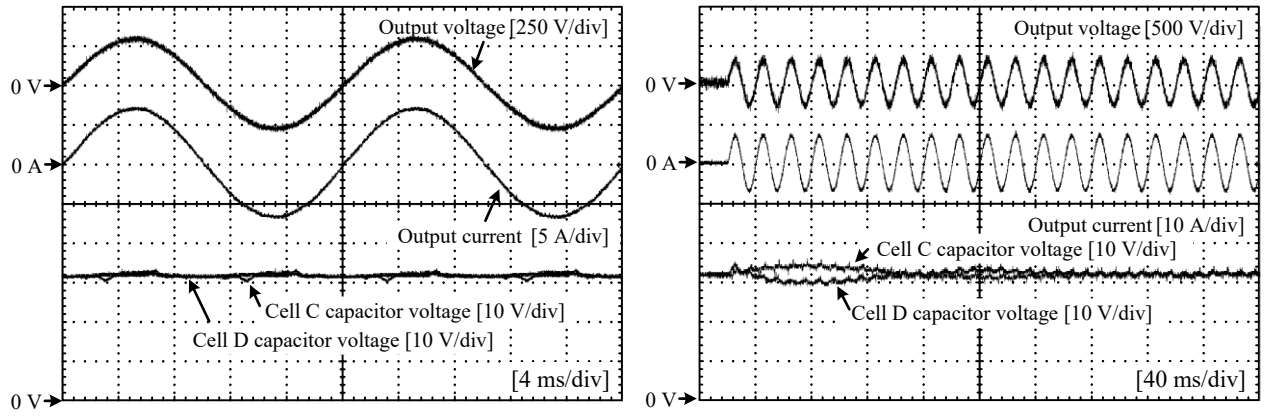


Fig. 10. Operation waveform with capacitor voltage control at rated power (1 kW), Voltage condition (I) E_A=190 V, E_B=95 V E_C=E_D=32 V.

wave-voltage waveform. It is demonstrated that the output voltages of the cell A–D are the full-wave rectified waveform. In this operation condition, the total harmonic distortion (THD) of the output voltage is 1.08%.

Figure 11 shows the capacitor voltage waveforms. Fig. 11 (a) shows the steady state. In Fig. 11(a), the capacitor voltage E_C and E_D are regulated by the capacitor voltage control. In addition, the capacitor voltage contains the ripple voltages, which fluctuates at twice grid frequency.

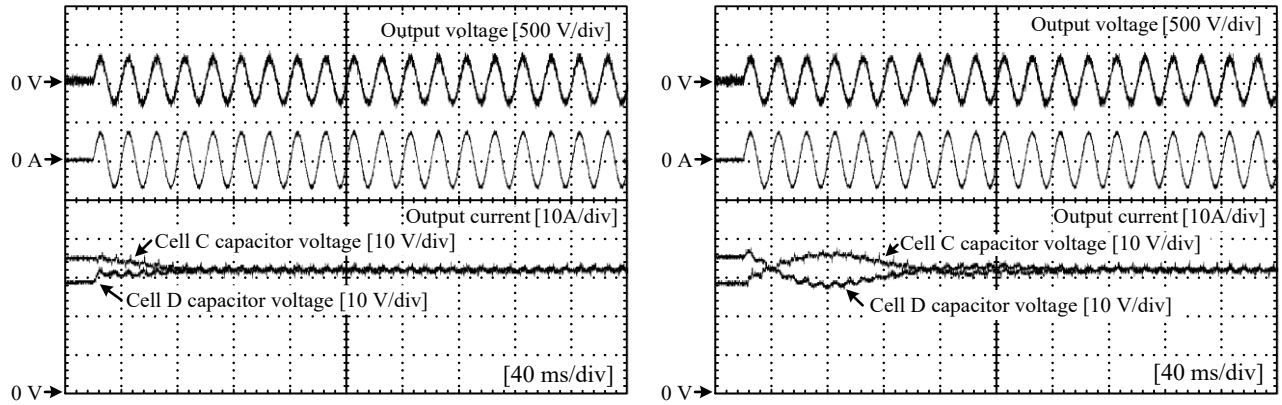
Figure 11(b) shows the capacitor voltage and the output waveforms during the transient state from no-load to full load. During the transient state, the output current and output voltage are sinusoidal. Besides, the capacitor voltage is converged in 220 ms. Thus, the validity of the capacitor voltage control is demonstrated by the experiment.



(a) Capacitor voltage waveform at steady state.

(b) Transient response of the capacitor voltage.

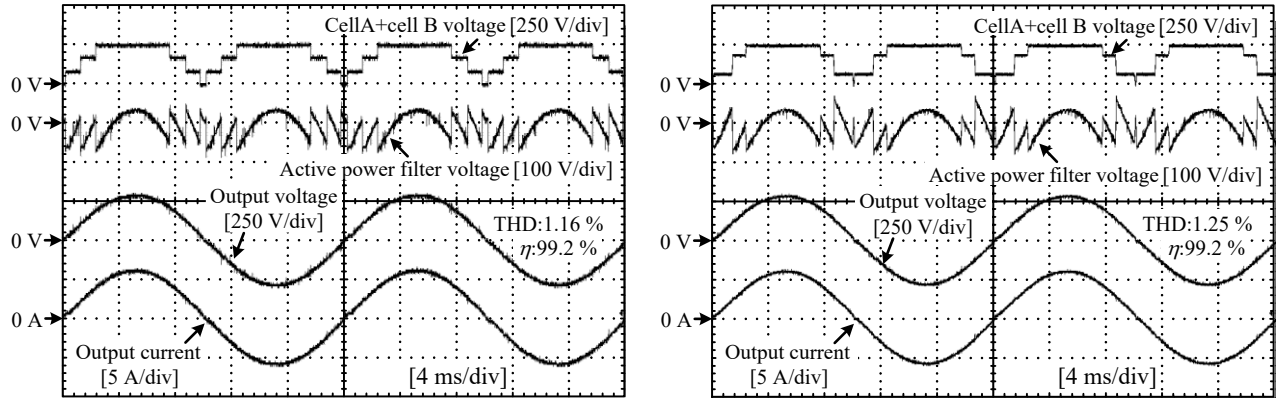
Fig. 11. Capacitor voltage waveform at rated power (1 kW), Voltage condition (I) E_A=190 V, E_B=95 V E_C=E_D=32 V.



(a) V_{C3} initial voltage +10%, V_{C4} initial voltage -10%.

(b) V_{C3} initial voltage -10%, V_{C4} initial voltage +10%.

Fig. 12. Capacitor voltage waveform at each capacitor voltage condition at rated power (1 kW), Voltage condition (I) E_A=190 V, E_B=95 V E_C=E_D=32 V.



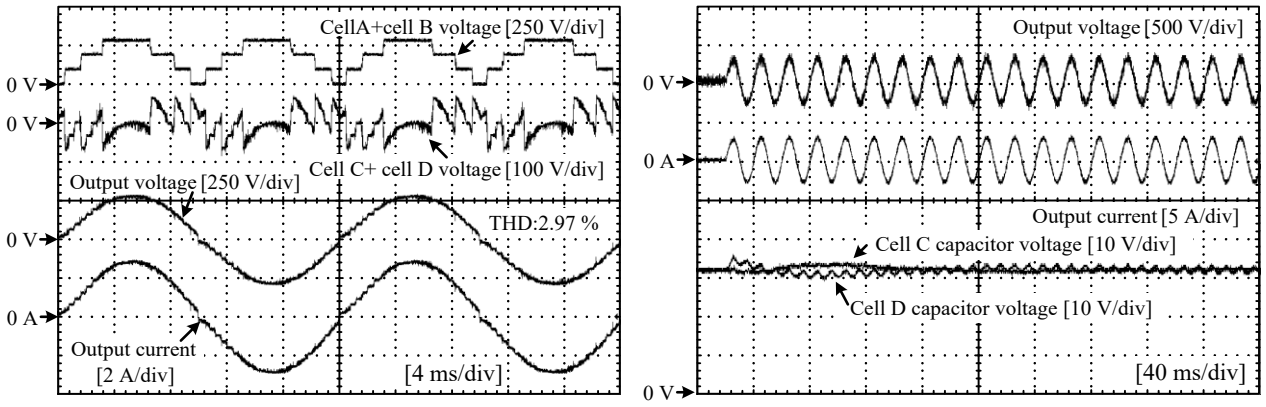
(a) Voltage condition (II) E_A=172 V, E_B=84 V E_C=E_D=32 V.

(b) Voltage condition (III) E_A=185 V, E_B=68 V E_C=E_D=32 V.

Fig. 13. Operation waveform at each voltage condition at rated power (1 kW).

Figure 12 shows the capacitor voltage fluctuation and the output waveforms during the transient state. In Fig. 12(a), the initial voltages of E_C and E_D are set to +10% and -10% to the nominal value, respectively. Similarly, in Fig. 12(b), the initial voltage of E_C and E_D are set to -10% and +10%, respectively. From Fig. 12, the capacitor voltages converge by the capacitor voltage control from the biased initial voltage conditions. Thus, the capacitor voltage controller is not affected by the initial voltage of the capacitor by unbalanced initial charge.

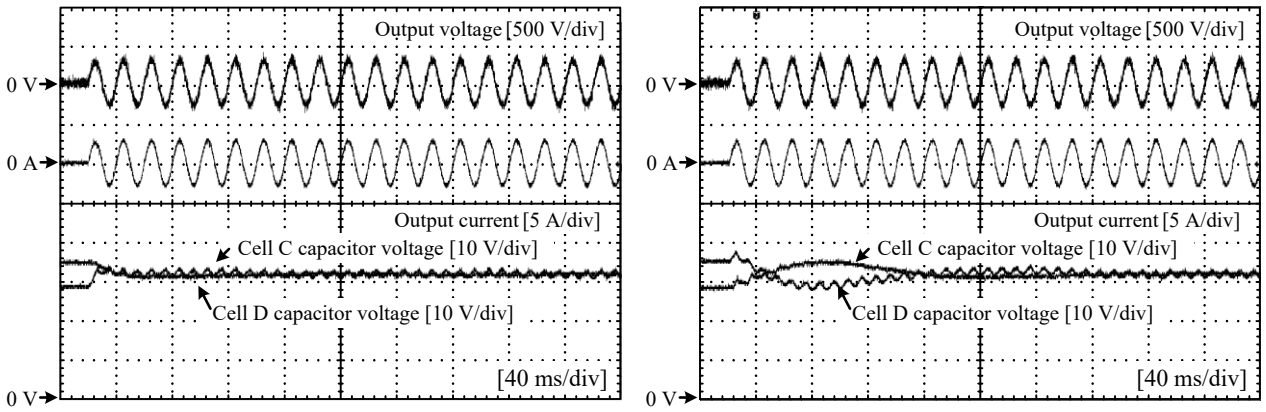
Figure 13 shows the operation waveforms of each voltage condition. In Fig. 13(a), DC-link voltage of the cell A is 172 V, DC-link voltage of the cell B is 95 V. In Fig. 13(b), DC-link voltage of the cell A is 185 V, DC-link voltage of the cell B is 64 V. From the experiments, it is ensured that the output



(a) Operation waveform with capacitor voltage control

(b) Transient respons of the capacitor from non-load to 400 W

Fig. 14. Operation waveform at load of 400 W, Voltage condition (I) E_A=190 V, E_B=95 V E_C=E_D=32 V.



(a) Voltage condition (II) E_A=172 V, E_B=84 V E_C=64 V.

(b) Voltage condition (III) E_A=185 V, E_B=68 V E_C=64 V

Fig. 15. Capacitor voltage waveform at each capacitor voltage condition at 400 W, Voltage condition (I) E_A=190 V, E_B=95 V E_C=E_D=32 V.

voltage and output current is the sinusoidal waveform at each DC-link voltage condition. Consequently, the output waveforms are not affected by DC-link voltage under the voltage condition(I)-(III). However, the voltage condition is not cleared that circuit operation to achieve. Thus, clarification of the voltage conditions is future work.

Figure 14 shows the operation waveforms with a light load: it is 0.4p.u. (400 W). Note that voltage condition is (I). Fig. 14 (a) shows the operation waveforms at the steady state. Fig. 14 (b) shows the capacitor voltage waveforms and output waveforms at light load. In the light load, the output voltage and current is the sinusoidal waveform. Moreover, the total harmonic distortion (THD) of the output voltage is 2.97%. Similarly, the capacitor voltage is stabilized by the capacitor voltage controller at a transient state from Fig. 14(b).

Figure 15 shows the capacitor voltage change from the unbalanced initial voltage during the transient state at the light load condition(400 W). In Fig. 15 (a), the initial voltage of E_C and E_D are set to +10% and -10%, respectively. the initial voltage of E_C is +10% and the initial voltage of E_D is -10%. Similarly, in Fig. 15 (b), the initial voltage of E_C and E_D are set to -10% and +10%, respectively. It is verified that the capacitor voltage is stabilized even at light load condition.

Figure 16 shows the THD characteristic of the output voltage when the output power is changed from 348 W to 1000 W at voltage condition of (I). The minimum THD is 1.06% at a load of 900 W, whereas the efficiency at rated load is 1.08%. The maximum THD is 4.6% at a load of 348 W. In the light load, the output voltage THD is increased caused by the ratio between the fundamental component and the harmonics component increases.

Figure 17 shows the efficiency characteristic with the output power from 348 W to 1000 W at voltage condition of (I). The maximum efficiency is 99.3% at a load of 900 W, whereas the efficiency at rated load is 99.2%. The measured efficiency is compared with the calculated value in section 3. The error of the efficiency between measurement and calculation is 0.4% that is caused by equivalent series resistance (ESR) of the capacitor, snubber circuit, and core loss of the inductor.

V. CONCLUSION

This paper proposed a multi-port DC-AC converter which connects the square-wave-voltage multilevel converter and the active filter in series. The proposed circuit reduced both the circuit volume and the power conversion loss. The loss of the proposed circuit reduced by up to 74.1% compared to the conventional circuit at the switching frequency of 100 kHz.

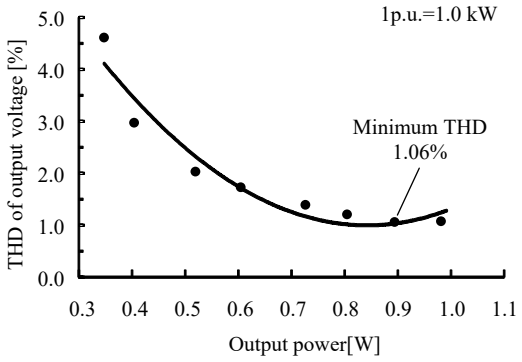


Fig. 16. THD characteristic at voltage condition (I).

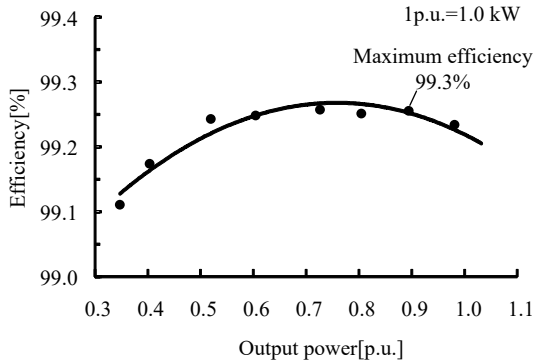


Fig. 17. Efficiency characteristic at voltage condition (I).

The proposed circuit will achieve the power density of 4.0 kW/dm^3 at 100 kHz. The power density of the proposed circuit is calculated by Pareto front optimization at the natural air cooling. Moreover, the validity of the proposed circuit and capacitor voltage control is demonstrated by the experiment results. In particular, it is verified that the THD of output voltage is 1.06% at 900 W. Besides, it was also verified that the prototype circuit achieved the maximum efficiency of 99.3% at 900 W. In addition, operation of the proposed circuit is ensured in each initial capacitor voltage, each DC-link voltage, and each load conditions.

In the future work, the design on the capacitor of active power filter will be clarified in order to improve the power density. Moreover, the voltage conditions are cleared that circuit operation to achieve. Furthermore, the verification of the loss analysis will be conducted.

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