Inverter Output Current Overshoot Suppression during Fault Ride-through Operation for Three-phase Grid-tied Inverter with Minimized Inductor

Satoshi Nagai, Hiroki Watanabe and Jun-ichi Itoh
Nagaoka University of Technology
Nagaoka, Niigata, Japan
satoshi_nagai@stn.nagaokaut.ac.jp; hwatanabe@vos.nagaokaut.ac.jp; itoh@vos.nagaokaut.ac.jp

***Abstract*— This paper proposes an inverter output current overshoot suppression technique for a three-phase grid-tied inverter with a minimized inductor during a fault-ride through operation. The inverter output current overshoots at the grid voltage drop or recovery with the low inductance. In order to suppress the current overshoot, the inverter output vector which reduces the slope of the output current overshoot to approximately zero is derived from the equations of the instantaneous active and reactive current at the voltage drop and recovery. Moreover, it is impossible to detect the grid voltage phase during grid voltage drop whose voltage is down to 0 V. Thus, a maximum-medium-minimum voltage detection and voltage pole detection circuit is applied in order to detect the grid voltage sectors. Furthermore, the three-phase inverter outputs nearly equals the grid voltage with the look-up table which depends on the grid voltage sector at the grid voltage recovery. As experimental results, the inductor current overshoot rate is reduced by 49% at the voltage recovery with the proposed voltage vector output compared to the counter voltage vector output.**

Keywords—three-phase grid-tied inverter, low inductance, fault ride-through, current overshoot

I. INTRODUCTION

In recent years, renewable energy such as photovoltaics (PV), wind turbine and fuel cell systems have been actively studied for energy saving to reduce fossil energy sources [1]-[3]. In order to transmit the renewable energy to the grid, a grid-tied inverter is used. The grid-tied inverter is required to reduce the size. In particular, the inverter-side inductors occupy the majority of the inverter volume. Thus, the inductors are required to reduce the size. High-frequency inverter operation with Silicon carbide (SiC) or Gallium nitride (GaN) devices reduces the inductance under the same condition of the current ripple, resulting in the reduction of the inductor volume. However, the low inductance leads to the decrease in the disturbance suppression performance of the current controller. The inverter output current distorts due to the low disturbance suppression performance. The inverter output current distortion is caused by the disturbance such as the dead-time induced error voltage. Therefore, the increase of the disturbance suppression performance is required to the grid-tied inverter with the low inductance [4].

On the other hand, the grid-tied inverter is required to meet a fault ride-through (FRT) operation during the voltage sag [5]-[13]. However, low inductance of the grid-tied inverter causes the inverter output current overshoot at the grid voltage drop and recovery. The inverter output current overshoot leads to overcurrent protection of the inverter, resulting in the disconnection between the inverter and the grid during the voltage sag. In addition, the maximum inverter output current at the grid voltage recovery has to be suppressed less than 150% of the rated inverter output current peak value in the steady-state operation [12]. Therefore, it is necessary to suppress the inverter output current overshoot during the voltage sag. Several conventional FRT operations have been proposed, in which the DC-link voltage control, and the output power control method are applied during the voltage sag [5]-[6]. However, these conventional methods have not considered the inverter output current overshoot at the voltage drop and recovery. The FRT operation with the counter voltage vector output operation has been proposed [14]. The counter voltage vector output operation suppresses the inductor current overshoot with the reverse voltage vector output for the inductor current at the grid voltage drop and recovery. The inductor current is instantaneously reduced with the counter voltage vector output. Furthermore, the inverter operation is continued by releasing the counter voltage vector output after one carrier period. However, the current overshoot occurs in the inductor due to the transient response by following current command from reduced current with the counter voltage vector output. In addition, it is impossible to detect the grid voltage during zero-voltage ride-through (ZVRT) because the grid voltage is 0 V. Thus, at the grid-voltage recovery, the current overshoot occurs in the inductor because the inverter cannot output the voltage considering the grid voltage. Therefore, in order to achieve the ZVRT operation and suppress the current overshoot at the grid voltage recovery, it is necessary to synchronize quickly the grid and inverter output voltage at the voltage recovery.

This paper proposes a control method for three-phase grid-tied inverter output vectors that achieves the suppression of the inverter output current overshoot at the voltage drop and recovery. Moreover, the current overshoot suppression method is proposed when the phase information detection failure occurs in the phase locked loop (PLL) output. The proposed method uses a three-phase maximum-medium-minimum voltage detection and voltage pole detection circuit. The circuits detect the grid voltage phase area (sector) in every 30 deg. The inductor current overshoot is suppressed by the inverter output voltage in each phase with the detected sector and the voltage recovery detection signal. The original idea of this paper is that the inverter output current overshoot is suppressed by changing the inverter output vector depending on the condition of the grid voltage such as the voltage drop or recovery. In addition, the inductor current overshoot is suppressed at the grid voltage recovery in the ZVRT operation even when the grid voltage phase is not detected. The inverter output vector is derived by the instantaneous active and reactive current during the voltage sag. Moreover, the inverter output vector is controlled so that the slope of the inverter output current becomes zero after the voltage drop or recovery. The proposed control method is verified by a 1-kW prototype.

II. CONVENTIONAL FRT OPERATION

A. FRT operation with current controller

Figure 1 shows a three-phase grid-tied inverter circuit. The three-phase two level inverter is evaluated in this paper. Note that the inductor impedance %Z is 0.38% for the output impedance of the inverter to reduce the size. The inductance is designed in [14].

Figure 2 shows a control block diagram of a conventional current controller for the grid-tied inverter. Note that PI is the controller, i_L is the inductor current, i_{L_det} is the inductor current detection value, i_L^* is the inductor current command, v_{ac} is the grid voltage, v_{ac_det} is the grid voltage detection value, v_{dead} is the dead-time error voltage, s is Laplace operator and T_{delay} is the detection delay time. Moreover, the inverter output switches to the reactive current from the active current when the voltage sag is detected. In addition, Digital Signal Processor (DSP) is used in the conventional current control. However, the control of DSP has the sampling and detection delay time. Thus, the inductor current overshoots at the voltage drop or recovery due to the control and detection delay time and the low inductance.

Figure 3 shows the conventional current controller applying the high-gain disturbance observer (DOB) [4], [15], [16]. The disturbance estimation voltage $\hat{v}_{dis}$ by DOB is expressed as

$$\hat{v}_{dis} = \frac{\omega_c}{s+\omega_c}\left(v_{dis\_PI} + \omega_c L i_{L\_det}\right) - \omega_c L i_{L\_det} \qquad (1),$$

where ω_c is the cutoff angular frequency of DOB, v_{dis_PI} is additional value of the PI output and the DOB output. The high-gain DOB is implemented in a high-speed controller as Field-Programmable Gate-Array (FPGA) to increase the disturbance suppression performance. The inverter output current total harmonic distortion (THD) with the high-gain DOB is achieved below 5% during normal operation with low inductance [4]. The high-gain DOB implemented in FPGA achieves the high cutoff frequency operation. Thus, the disturbance for the inverter current controller is estimated in wideband. Note that the grid voltage is compensated by the feedforward compensation in the FPGA. However, this conventional control method leads to the inductor current overshoot due to the detection and sampling delay time of the grid voltage at the voltage drop or recovery.

B. Counter voltage vector output method

The counter voltage vector output is applied to suppress the current overshoot at the voltage drop and recovery [14]. The principal of the counter voltage vector output is expressed as follows. The circuit equation of the three-phase inverter is expressed as

$$\begin{bmatrix} v_p \\ v_q \end{bmatrix} = \begin{bmatrix} pL & \omega L \\ -\omega L & pL \end{bmatrix} \begin{bmatrix} i_p \\ i_q \end{bmatrix} + \begin{bmatrix} v_{ac} \\ 0 \end{bmatrix} \qquad (2),$$

where v_p and v_q are the instantaneous active and reactive voltages of the inverter, i_p and i_q are the instantaneous active and reactive currents of the inverter, L is the inductance, v_{ac} is the grid voltage, ω is the grid angular frequency, p is the differential operator, and the power factor is unity. Note that the resistance of the inductor is ignored.

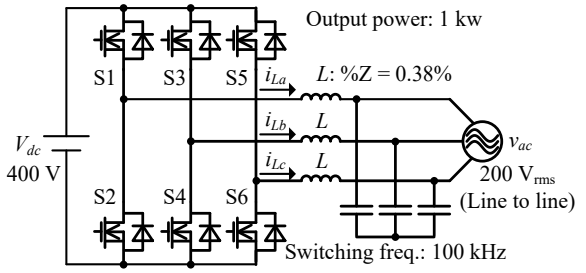


Figure 1. Three-phase grid-tied inverter with minimized inductor. The inductor impedance %Z is 0.38% of the inverter normalized impedance. (%Z is inductor impedance ratio for the output impedance of the inverter.)

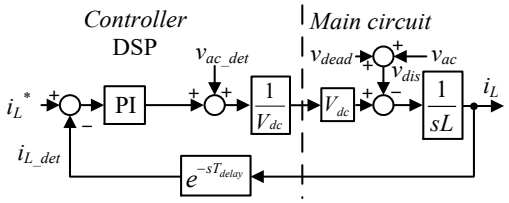


Figure 2. Control block diagram of conventional current controller. The current control with DSP has the sampling and detection delay time.

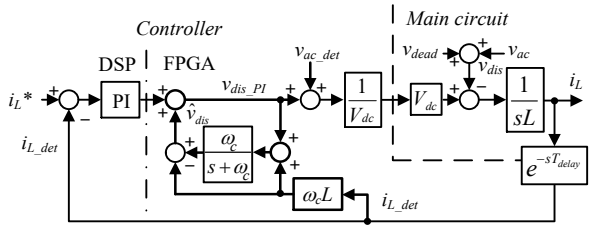


Figure 3. Control block diagram of conventional current controller with high-gain DOB. The high-gain DOB is implemented in FPGA to compensate the disturbance with wideband.

First, considering the inverter operation at the voltage drop. In order to satisfy the grid code even at the worst case, the ZVRT operation is evaluated, where v_{ac} in (2) becomes 0 V from the grid voltage peak value at the voltage drop. Thus, the active and reactive inductor currents i_p and i_q are expressed as

$$i_p = \frac{v_p}{\omega L}\sin\omega t - \frac{v_q}{\omega L}\left(1-\cos\omega t\right) + i_{p0}\cos\omega t - i_{q0}\sin\omega t \qquad (3)$$

$$i_q = \frac{v_p}{\omega L}\left(1-\cos\omega t\right) + \frac{v_q}{\omega L}\sin\omega t + i_{p0}\sin\omega t + i_{q0}\cos\omega t \qquad (4),$$

where t is time, i_{p0} and i_{q0} are the active and reactive inductor currents at the steady-state operation. Differentiating (3) and (4), the current slope of i_p at the moment of the voltage drop becomes positive, whereas the current slope of i_q becomes approximately zero. After the moment of the voltage drop, in order to minimize the current overshoot, the instantaneous active and reactive inverter output voltages v_{pfrt}, v_{qfrt} are controlled such that the current slope of i_p after the moment of the voltage drop becomes negative as much as possible, whereas the current slope of i_q should be maintained at zero. Thus, the instantaneous active and reactive inverter output voltages v_{pfrt}, v_{qfrt} are derived from following equations

$$\frac{di_p}{dt} = \frac{v_{pfrt}}{L}\cos\omega t - \frac{v_{qfrt}}{L}\sin\omega t - \omega i_{p0}\sin\omega t - \omega i_{q0}\cos\omega t = -\infty \quad (5)$$

$$\frac{di_q}{dt} = \frac{v_{pfrt}}{L}\sin\omega t + \frac{v_{qfrt}}{L}\cos\omega t + \omega i_{p0}\cos\omega t - \omega i_{q0}\sin\omega t = 0 \quad (6).$$

Solving (5) and (6) with v_{pfrt}, v_{qfrt} as variables, the instantaneous active and reactive inverter output voltages become as $v_{pfrt} = -\infty$, $v_{qfrt} = -\omega L i_{p0}$. However, the inverter output voltage is limited to $V_{dc}/2$. In addition, v_{qfrt} nearly equals to zero when the low inductance is applied. Therefore, the inverter output current reduction effectiveness becomes the maximum, when the instantaneous active and reactive inverter output voltage are set as $v_{pfrt} = -V_{dc}/2$, $v_{qfrt} = 0$. Consequently, the output voltage vector is equal to reverse vector for the inverter output current (the counter voltage vector).

Second, considering the inverter operation at the voltage recovery. In order to satisfy the grid code even at the worst case, the ZVRT operation is evaluated, where v_{ac} in (2) changes from 0 V to the grid voltage peak value at the voltage recovery. Similar to the inverter operation at the voltage drop, the active and reactive currents i_p and i_q at the voltage recovery are expressed as

$$i_p = \frac{v_p}{\omega L}\sin\omega t - \frac{v_q}{\omega L}(1-\cos\omega t) - \frac{v_{ac}}{\omega L}\sin\omega t + i_{p0}\cos\omega t - i_{q0}\sin\omega t \quad (7)$$

$$i_q = \frac{v_p}{\omega L}(1-\cos\omega t) + \frac{v_q}{\omega L}\sin\omega t - \frac{v_{ac}}{\omega L}(1-\cos\omega t) + i_{p0}\sin\omega t + i_{q0}\cos\omega t \quad (8),$$

where the current slope of the active current i_p at the moment of the voltage recovery is negative, whereas the slope of the reactive current i_q is approximately zero. Similarly, after the moment of the voltage recovery, in order to minimize the current overshoot, the instantaneous active and reactive inverter output voltages v_{pfrt}, v_{qfrt} are controlled such that the current slope of i_p after the moment of the voltage recovery becomes positive as much as possible, whereas the current slope of i_q should be maintained at zero. Therefore, the active and reactive inverter output voltage v_{pfrt} and v_{qfrt} are derived as following equations

$$\frac{di_p}{dt} = \frac{v_{pfrt}}{L}\cos\omega t - \frac{v_{qfrt}}{L}\sin\omega t - \frac{v_{ac}}{L}\cos\omega t - \omega i_{p0}\sin\omega t - \omega i_{q0}\cos\omega t = \infty \quad (9)$$

$$\frac{di_q}{dt} = \frac{v_{pfrt}}{L}\sin\omega t + \frac{v_{qfrt}}{L}\cos\omega t - \frac{v_{ac}}{L}\sin\omega t + \omega i_{p0}\cos\omega t - \omega i_{q0}\sin\omega t = 0 \quad (10).$$

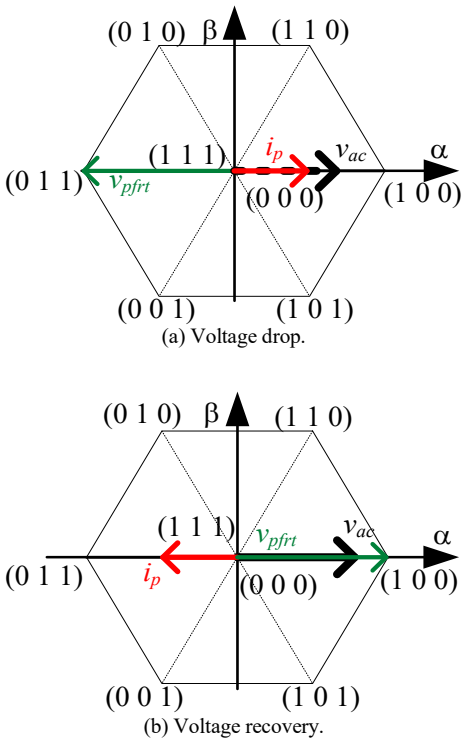


Figure 4. Counter voltage vector output for FRT operation. The counter voltage vector output achieves the inverter output current reduction at the voltage drop and recovery.

Solving (9) and (10) with v_{pfrt}, v_{qfrt} as variables, the instantaneous active and reactive inverter output voltages become as $v_{pfrt} = V_{dc}/2$, $v_{qfrt} = 0$. The output voltage vector equals to the counter voltage vector.

Figure 4 shows the vector diagram of the counter voltage vector output at the grid voltage drop and recovery. The inverter output voltage becomes the reverse vector against the inverter output current vector at the voltage drop and recovery. In particular, the counter voltage vector output is achieved by the momentary gate-block, when the grid voltage fluctuation is detected. After the momentary gate-block is completed, the counter voltage vector output is released to continue the inverter operation during the voltage sag. However, the current overshoot might still occur in the inductor due to the transient response because the instantaneous inverter output current is reduced by applying the counter voltage vector output at the voltage drop and recovery [14]. In the other words, only the momentary gate-block cannot suppress the current overshoot.

III. PROPOSED VOLTAGE VECTOR OUTPUT FOR FRT OPERATION

In order to suppress the overshoot current due to the transient response after the completion of the momentary gate-block, the inverter output voltage vector at the voltage recovery is operated as that the differential of the inverter output current is zero in (9), (10). Thus, equation (9) is modified as follows

$$\frac{di_p}{dt} = \frac{v_{pfrt}}{L}\cos\omega t - \frac{v_{qfrt}}{L}\sin\omega t - \frac{v_{ac}}{L}\cos\omega t - \omega i_{p0}\sin\omega t - \omega i_{q0}\cos\omega t = 0 \quad (11).$$

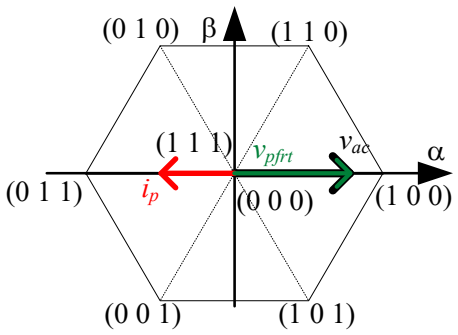


Figure 5. Proposed voltage vector output for FRT operation at the voltage recovery. The proposed voltage vector suppresses the current overshoot and the transient response at the voltage recovery.

Considering the inverter operation at the voltage recovery, in which the active and reactive inverter output voltage vector should become $v_{pfrt} = v_{ac}$, $v_{qfrt} = 0$ according to (10), (11). Therefore, in order to suppress the current overshoot and transient response at the voltage recovery, the inverter output voltage should output same as the grid voltage value. However, the inverter output voltage is affected by the dead-time error voltage in practical. Thus, in order to output the inverter output voltage which equals to v_{ac}, the inverter output voltage command should consider the dead-time error voltage v_{dead} for the grid voltage v_{ac}.

Figure 5 shows the proposed inverter output voltage vector at the voltage recovery. The inverter output voltage v_{pfrt} is same as the grid voltage at the voltage recovery. This control ensures that the differential of the inverter output current is zero at the grid voltage recovery. Thus, the inverter output current overshoot is possible to suppress without the momentary gate-block operation. On the other hand, considering the inverter operation at the voltage drop, in which the active and reactive inverter output voltage vector should become $v_{pfrt} = v_{ac}$, $v_{qfrt} = 0$ according to (5), (6). However, it is impossible to obtain the voltage drop value in advance. Therefore, the counter voltage vector output is still applied at the voltage drop. However, in order to suppress the current overshoot after releasing the counter voltage vector output, the integrator of DOB in Fig. 3 is initialized to reduce the error between the actual and estimated disturbance value.

IV. VOLTAGE RECOVERY DETECTION METHOD AFTER GRID-PHASE DETECTION FAILURE

It is necessary to detect the grid voltage phase at the grid voltage recovery in order to carry out the proposed vector output. However, it is impossible to synchronize the grid phase by applying PLL during voltage sag whose voltage is down to 0 V. Thus, the grid phase after the grid recovery cannot be predicted. Therefore, a maximum-medium-minimum voltage detection and voltage pole detection circuit is applied to detect the grid phase after the grid voltage recovery.

Table I shows the grid voltage sector with the maximum-medium-minimum voltage detection and voltage pole detection circuit, whereas Figure 6 shows the proposed inverter output voltage in each phase when the grid voltage recovers at the sector shown in Table I. Note that Max. is the maximum voltage phase among three-phase voltages, Min. is the minimum voltage phase, Mid. pos. is the positive pole in medium voltage phase, and Mid. neg. is the negative pole in medium voltage phase. Furthermore, the number of sector is twelve by dividing every 30 deg. Hence, the inductor current

Table I. Proposed output vector at grid voltage recovery.

Sector No.	a phase	b phase	c phase	Duty ratio for v_{ac}		
				a	*b*	*c*
Sector 1	Max.	Mid. neg.	Min.	1	-1/2	$-\sqrt{3}/2$
Sector 2	Max.	Mid. pos.	Min.	$\sqrt{3}/2$	1/2	-1
Sector 3	Mid. pos.	Max.	Min.	1/2	$\sqrt{3}/2$	-1
Sector 4	Mid. neg.	Max.	Min.	-1/2	1	$-\sqrt{3}/2$
Sector 5	Min.	Max.	Mid. neg.	$-\sqrt{3}/2$	1	-1/2
Sector 6	Min.	Max.	Mid. pos.	-1	$\sqrt{3}/2$	1/2
Sector 7	Min.	Mid. pos.	Max.	-1	1/2	$\sqrt{3}/2$
Sector 8	Min.	Mid. neg.	Max.	$-\sqrt{3}/2$	-1/2	1
Sector 9	Mid. neg.	Min.	Max.	-1/2	$-\sqrt{3}/2$	1
Sector 10	Mid. pos.	Min.	Max.	1/2	-1	$\sqrt{3}/2$
Sector 11	Max.	Min.	Mid. pos.	$\sqrt{3}/2$	-1	1/2
Sector 12	Max.	Min.	Mid. neg.	1	$-\sqrt{3}/2$	-1/2

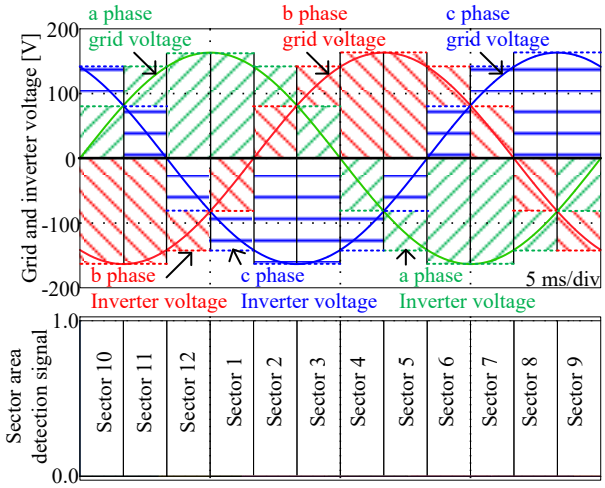


Figure 6. Concept of inverter output voltage for inductor current overshoot reduction.

overshoot at the voltage recovery is suppressed with the inverter output voltage in Table I. The inverter output voltage value in Table I is near the grid voltage value at the voltage recovery. Moreover, the inverter output voltage in each phase for every sector is maximum value of the grid voltage in each phase of every sector as Fig. 6. As the results, the inverter output voltage is kept up higher than the grid voltage, resulting the current overshoot is suppressed.

Figure 7 shows the flowchart for the inverter operation with the proposed voltage vector output to suppress the current overshoot. The sector for the grid voltage is divided to twelve areas with the maximum-medium-minimum voltage detection and voltage pole detection as Table I. Moreover, the duty ratio of the inverter output voltage is derived for every sector as Table I. Furthermore, the proposed inverter output voltage is outputted when the grid voltage recovery is detected, the counter voltage vector is outputted when the grid voltage drop is detected, and the steady state operation is carried out when the grid voltage drop and recovery are not detected.

V. PROPOSED FRT OPERATION METHOD FOR CURRENT OVERSHOOT SUPPRESSION

Figure 8 shows the control block diagram of the proposed FRT control with minimized inductor, corresponding the grid phase detection failure during the voltage sag. Note that v_x is the voltage detection value of the each phase, v_{sag_x} is the detection signal of grid disturbance in each phase ($x = a, b, c$), i_{Ld}^*, i_{Lq}^* is the current command in dq-axis, i_{Ld_det}, i_{Lq_det} is the inductor current detection value in dq-axis, v_{acd_det}, v_{acq_det} is

the grid voltage detection value in dq-axis, and V_{ac} is the grid phase voltage peak. The current control is achieved by the PI controller. In addition, the high-gain DOB which is implemented in FPGA is applied to compensate the disturbance for the current controller such as the dead-time error voltage as Fig. 3. The grid voltage drop and recovery detection signals *drop_det* and *recover_det* become one at the voltage drop and recovery. Moreover, the voltage drop and recovery are detected with the analog circuit at high speed. Thus, the voltage drop or recovery operation is divided by these signals. The counter voltage vector output is carried out by the voltage drop signal *drop_det*. Moreover, proposed voltage vector output is carried out by the voltage recovery signal *recover_det*. The integrator of DOB is initialized to zero at the voltage drop and recovery in order to reduce the current overshoot. On the other hand, the inverter output vector to reduce the current overshoot is outputted by referring the sector detection in Table I with the grid voltage recovery signal *recover_det* and the table of MUX1 in Fig. 8. The output period of inverter vector suppressing current overshoot is short enough for the grid frequency. In this paper, the period is two cycles of switching period (switching period is 10 μs). The operation period of proposed vector includes the wait time to update in order that the grid voltage detection value becomes the actual grid voltage value after releasing the proposed vector operation. The wait time to update the grid voltage detection is as the grid voltage detection delay time.

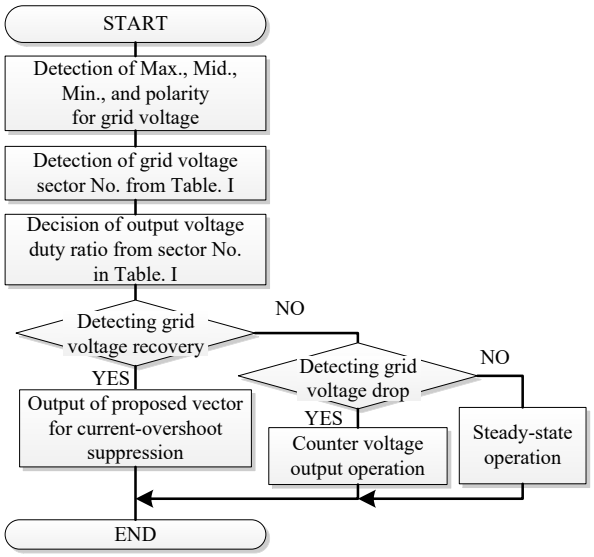


Figure 7. Flowchart for proposed voltage vector output to suppress current overshoot at voltage drop and recovery.

Figure 9 shows the voltage sag detection circuit and the voltage drop and recovery signal generator for the proposed voltage vector output operation. Note that v_x is the phase voltage (x = *a, b, c*), V_{ac_th} is the threshold of voltage sag detection for a high-pass filter (HPF) output. The voltage sag detection circuit is composed in analog circuit such as HPF and a comparator. The voltage sag is detected at high speed by the analog circuit. Furthermore, the voltage drop and recovery signals *drop_det* and *recover_det* are generated in the FPGA using the voltage sag detection signal v_{sag_x} and voltage detection value of q axis v_{acq_det}. In addition, the proposed voltage vector output period is set to two cycle of the carrier period to continue the inverter operation. Thus, application of the analog circuit and FPGA reduce the delay time of the proposed voltage vector output operation.

Figure 10 shows the operation waveform of the voltage sag detection circuit and the grid voltage drop and recovery signals generator. The HPF output HPF_{out} overshoots at the grid voltage fluctuation. In addition, the HPF output HPF_{out} is compared with the threshold V_{ac_th}. Thus, the voltage-sag detection circuit output v_{sag_x} becomes the low signal at the voltage drop or recovery. After that, the voltage drop and recovery signals *drop_det* and *recover_det* are generated in the FPGA by the low signal of voltage-sag detection circuit output v_{sag_x} and voltage detection value of q axis v_{acq_det} as in MUX2 of Fig. 8.

VI. EXPERIMENTAL RESULTS

Table II shows the experimental conditions for the FRT operations. The inductance designed in [14] is applied to the prototype. The carrier frequency is 100 kHz, whereas the sampling frequency of the current controller (Auto current

MUX1			
sector	1	2	3
$d_{a\_frt\_0}$	V_{ac}	$V_{ac}\sqrt{3}/2$	$V_{ac}/2$
$d_{b\_frt\_0}$	$-V_{ac}/2$	$V_{ac}/2$	$V_{ac}\sqrt{3}/2$
$d_{c\_frt\_0}$	$-V_{ac}\sqrt{3}/2$	$-V_{ac}$	$-V_{ac}$
sector	4	5	6
$d_{a\_frt\_0}$	$-V_{ac}/2$	$-V_{ac}\sqrt{3}/2$	$-V_{ac}$
$d_{b\_frt\_0}$	V_{ac}	V_{ac}	$V_{ac}\sqrt{3}/2$
$d_{c\_frt\_0}$	$-V_{ac}\sqrt{3}/2$	$-V_{ac}/2$	$V_{ac}/2$
sector	7	8	9
$d_{a\_frt\_0}$	$-V_{ac}$	$-V_{ac}\sqrt{3}/2$	$-V_{ac}/2$
$d_{b\_frt\_0}$	$V_{ac}/2$	$-V_{ac}/2$	$-V_{ac}\sqrt{3}/2$
$d_{c\_frt\_0}$	$V_{ac}\sqrt{3}/2$	$-V_{ac}$	V_{ac}
sector	10	11	12
$d_{a\_frt\_0}$	$V_{ac}/2$	$V_{ac}\sqrt{3}/2$	V_{ac}
$d_{b\_frt\_0}$	$-V_{ac}$	$-V_{ac}$	$-V_{ac}\sqrt{3}/2$
$d_{c\_frt\_0}$	$V_{ac}\sqrt{3}/2$	$V_{ac}/2$	$-V_{ac}/2$

MUX2			
v_{sag_x}	0		1
v_{acq_det}	$< v_{ac}*0.8$	$\geq v_{ac}*0.8$	-
drop_det	0	1	0
recover_det	1	0	0

- : Don't care

MUX3		
recover_det	0	1
d_a'	d_a	d_{a_frt}
d_b'	d_b	d_{b_frt}
d_c'	d_c	d_{c_frt}

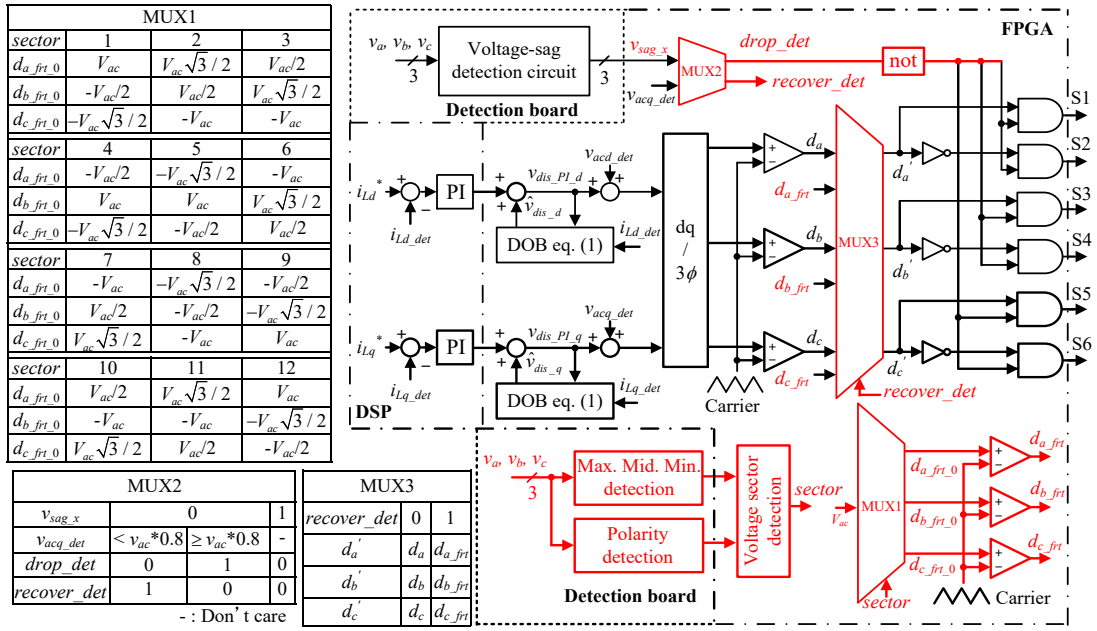


Figure 8. Control block diagram of proposed FRT control with minimized inductor corresponding to detection failure of grid phase information. The current overshoot at the voltage recovery is suppressed with the table of MUX1 and the voltage recovery detection signal.

regulator: ACR) is 20 kHz which is implemented in DSP, and the sampling frequency of the high-gain DOB is 100 kHz which is implemented in FPGA. Furthermore, the detection delay time of the voltage drop and recovery is less than 6.0 μs. In this experiment, ZVRT operations are verified with the conventional FRT operation applying the high-gain DOB, the counter voltage vector output, and the proposed voltage vector output. Moreover, the grid voltage drop and recovery occurrence at the voltage peak is evaluated in order to verify the worst condition for the current overshoot rate, where the inductor current is negative direction peak value when the voltage recovery occurs in the grid at the positive peak value. In addition, the current controller cannot keep the phase information at the voltage recovery due to the ZVRT operation causing error between the PLL information and the grid voltage phase without grid voltage detection value.

Figure 11 shows the experimental results of the ZVRT operations with the three methods. The three methods are the conventional FRT operation with the high-gain DOB, the counter voltage vector output, and the proposed voltage vector output. Note that the grid voltage drop and recovery occur in the grid at the a phase voltage peak. In Fig. 11 (a), the inverter output stops at the voltage drop with the conventional FRT operation with the high-gain DOB. However, In both Fig. 11 (b) and (c), the inverter operation is possible to continue with either the counter voltage vector output or the proposed voltage vector output at the voltage drop and recovery. However, the current overshoot is different in each method.

Figure 12 shows the magnified waveform at the voltage drop with the conventional FRT operation applying the high-gain DOB, and the counter voltage vector output. Note that the counter voltage vector output is applied in the proposed FRT operation at the voltage drop operation. In Fig. 12 (a), the current overshoot occurs in the inductor at the moment of the voltage drop with the conventional FRT operation applying the high-gain DOB. Furthermore, inverter operation stops due to the large current overshoot. The current overshoot occurs in the inductor due to the delay time for the update of inverter output voltage considering the instantaneous value of the grid voltage at the voltage drop. The delay time for the update of inverter output voltage is caused by the detection and sampling delay time and the calculation delay time of controller. On the other hand, the inductor current overshoot at the voltage drop is suppressed by the application of the counter voltage vector output. The delay time for the update of inverter output voltage is reduced with the counter voltage vector output applying the voltage drop detection with the analog circuit and FPGA. Thus, the current overshoot with the counter voltage vector output is suppressed by the high speed operation compared with the conventional FRT operation applying the high-gain DOB. In particular, the inductor current overshoot rate with two methods at the voltage drop are 335% (conventional FRT operation with the high-gain DOB) and 118% (counter voltage vector output) of the rated inductor current peak, respectively. The current overshoot is reduced by 217%.

Figures 13 and 14 show the magnified waveform at the voltage recovery with the counter voltage vector output, and the proposed voltage vector output. In Fig. 13, the inductor current is reduced by the counter voltage vector output at the voltage recovery. However, the current overshoot occurs in the inductor after releasing the counter voltage vector. The

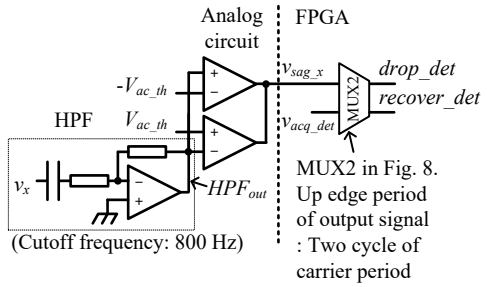


Figure 9. Voltage sag detection circuit and voltage drop and recovery signal generator. The voltage drop and recovery signals are generated at fast speed by applying the analog circuit and FPGA.

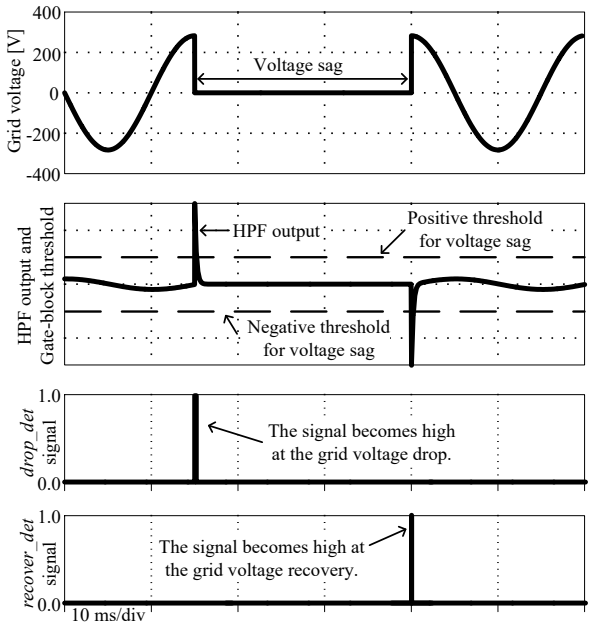
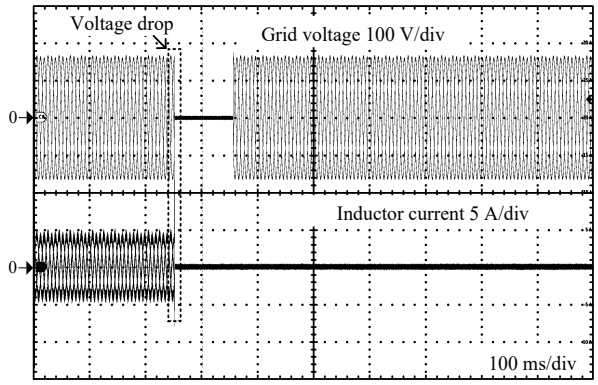


Figure 10. Operation of voltage sag detection circuit and voltage drop and recovery signals generator.

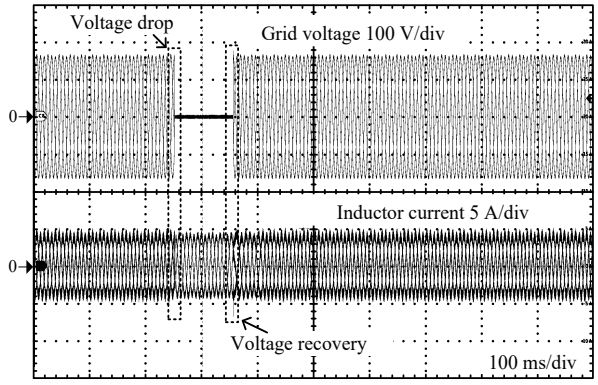
Table II. Experimental conditions

Output power	P_{out}	1 kW	Ang. fre. of ACR	ω_n	4000 rad/s
DC link vol.	V_{dc}	400 V	Samp. fre. of ACR	f_{samp}	20 kHz
Grid voltage (line to line)	v_{ac}	200 V_{rms}	Samp. fre. of DOB	f_{so}	100 kHz
			Cutoff fre. of DOB	f_c	2 kHz
Conv.-side Induc. (%Z)	L	0.48 mH (0.38%)	Dead time	t_{dead}	500 ns
Filter cap.	C	2.2 μF	Volt. sag det. delay time	t_{sag_d}	< 6.0 μs
Carrier fre.	f_{cry}	100 kHz			

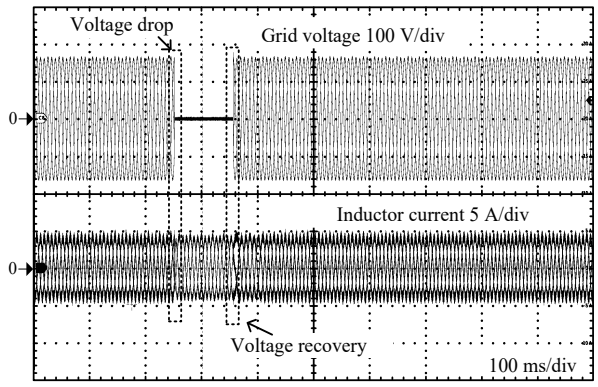
current overshoot occurs in the inductor due to that the reduced inductor current follows the current command. Thus, the transient response should be reduced to suppress the current overshoot. The inductor current overshoot rates with the counter voltage vector output at each phase voltage recovery operation are 169%, 171%, and 170%. Moreover, the counter voltage vector output operation does not meet the FRT requirements due to that the current overshoot rate exceeds 150%. On the other hand, the inductor current overshoot in Fig. 14 is suppressed by the proposed voltage vector output compared with Fig. 13. The proposed voltage vector is outputted approximately as same as the grid voltage at the grid voltage recovery. Thus, the inductor current is kept because the inductor current slope becomes zero. Therefore, the transient response and the current overshoot at the voltage recovery are suppressed by the proposed method. The inductor current overshoot rates with the proposed method at each phase voltage recovery operation are 123%, 132%, and



(a) Conventional FRT operation with high-gain DOB.



(b) Conventional FRT operation with counter voltage vector output.



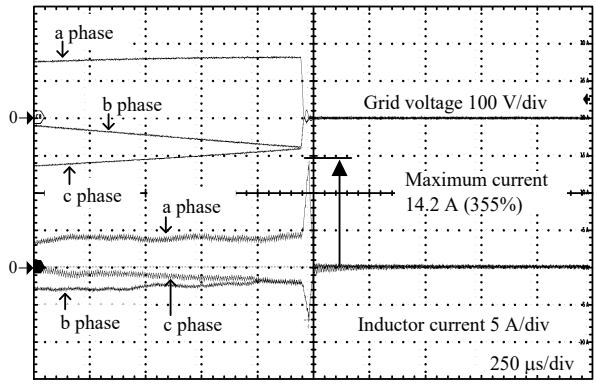
(c) Proposed voltage vector output operation.

Figure 11. Experimental results for the ZVRT operation at the a phase voltage drop and recovery. The counter voltage vector output and the proposed voltage vector output continue the inverter output during the voltage sag.

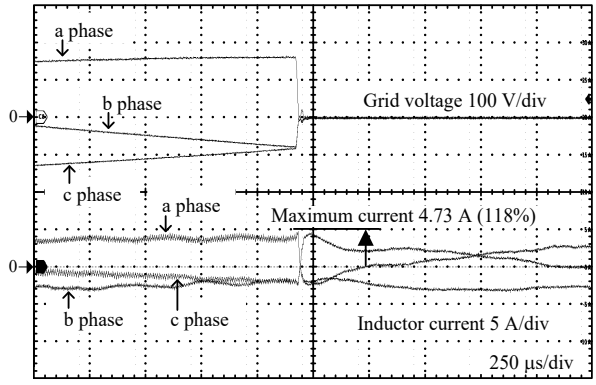
131%. Hence, the proposed FRT operation meets the FRT requirements due to that the current overshoot rate is less than 150%. Furthermore, the current overshoot rates with the proposed FRT operation at each phase voltage recovery operation are reduced by 46% (a phase), 39% (b phase), and 39% (c phase).

VII. CONCLUSION

This paper proposed the inductor current overshoot suppression method at the grid voltage recovery with the inverter output vector considering the transient response. Moreover, the current overshoot suppression method was proposed when the phase information detection failure occurs in the PLL output. The inductor current overshoot rate was reduced by 46% at the voltage recovery with the proposed FRT operation compared to the counter voltage vector output. Moreover, the proposed method met the FRT requirements as



(a) Conventional FRT operation with high-gain DOB.



(b) With counter voltage vector output.

Figure 12. Experimental results at the a phase voltage drop operation. The inductor current overshoot is suppressed with the counter voltage vector output.

the current overshoot less than 150% at the voltage recovery. Therefore, the validity of the proposed method was confirmed with the experimental results.

In future work, the verification of the asymmetrical voltage sag operation will be considered.

REFERENCES

[1] M. Ushiroda, T. Wakimoto, H. Yamada, T. Tanaka, M. Okamoto, and K. Kawahara, "Voltage Rise Suppression and Load Balancing by PV-PCS with Constant DC-Capacitor Voltage-Control-Based Strategy in Single-Phase Three-Wire Distribution Feeders," *IEEJ Journal of Industry Applications*, Vol. 6, No. 5, pp. 303-310, 2017.

[2] L. Valverde, C. Bordons, and F. Rosa, "Integration of Fuel Cell Technologies in Renewable-Energy-Based Microgrids Optimizing Operational Costs and Durability", *IEEE Trans. Ind. Electron*., Vol. 63, No. 1, pp. 167-177, 2016.

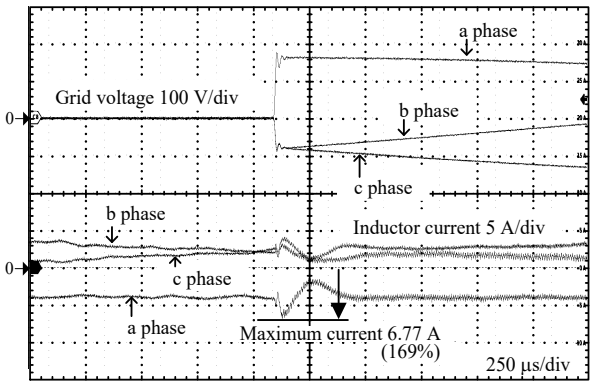
[3] Z. Zhang, H. Fang, F. Gao, J. Rodríguez, and R. Kennel, "Multiple-Vector Model Predictive Power Control for Grid-Tied Wind Turbine System With Enhanced Steady-State Control Performance", *IEEE Trans. Ind. Electron*., Vol. 64, No. 8, pp. 6287-6298, 2017.

[4] S. Nagai, H. N. Le, T. Nagano, K. Orikawa and J. Itoh, "Minimization of interconnected inductor for single-phase inverter with high-performance disturbance observer," *in Proc. IEEE 8th Inter. Power Electron. and Motion Control Conf.* (*IPEMC-ECCE Asia*), pp. 3218-3225, 2016.

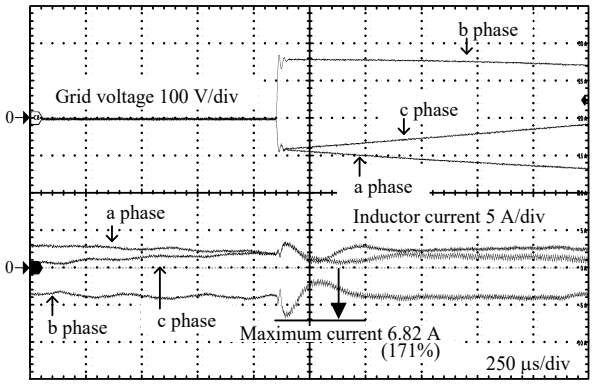
[5] G. Ding, F. Gao, H. Tian, C. Ma, M. Chen, G. He, and Y. Liu, "Adaptive DC-Link Voltage Control of Two-Stage Photovoltaic Inverter During Low Voltage Ride-Through Operation", *IEEE Trans. Power Electron*., Vol. 31, No. 6, pp. 4182-4194, 2016

[6] J. Alipoor, Y. Miura, and T. Ise, "Voltage Sag Ride-through Performance of Virtual Synchronous Generator", *IEEJ Journal of Industry Applications*, Vol. 4, No. 5, pp. 654-666, 2015.

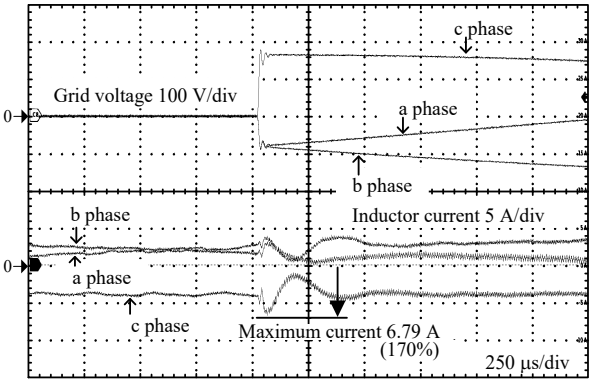
[7] H. Chen, C. Lee, P. Cheng, R. Teodorescu and F. Blaabjerg, "A LowVoltage Ride-Through Technique for Grid-Connected Converters With Reduced Power Transistors Stress," *in IEEE Trans. Power Electron*., Vol. 31, No. 12, pp. 8562-8571, 2016.



(a) a phase voltage recovery operation.

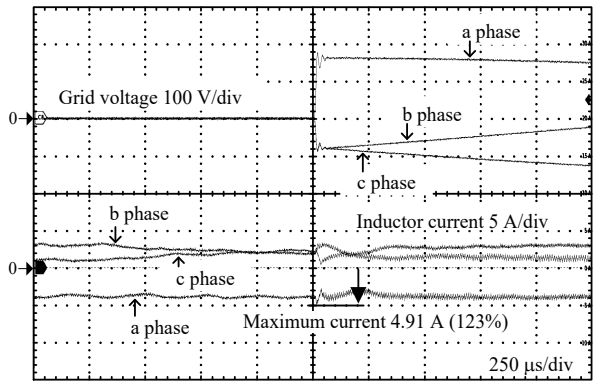


(b) b phase voltage recovery operation.

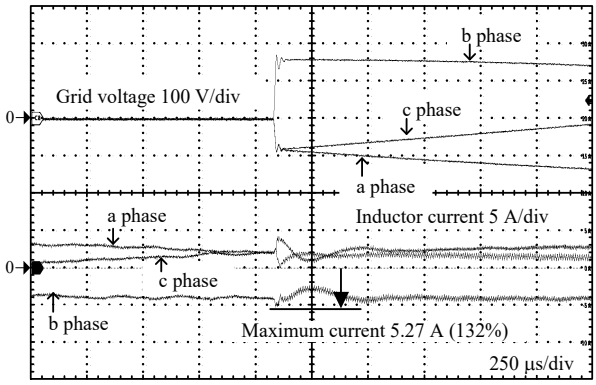


(c) c phase voltage recovery operation.

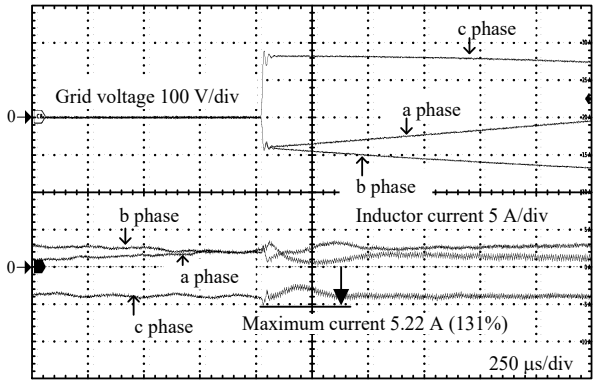
Figure 14. Experimental results for ZVRT operation with counter voltage vector output operation. The inductor current overshoot occurs due to the detection failure of grid phase after the voltage recovery.



(a) a phase voltage recovery operation.



(b) b phase voltage recovery operation.



(c) c phase voltage recovery operation.

Figure 15. Experimental results for ZVRT operation with proposed voltage vector output operation. The inductor current overshoot is suppressed by the grid voltage sector detection and the inverter output vector approximately same as the grid voltage at the voltage recovery.

[8] B. Liu, T. Yoshino, and A. Kawamura, "Seamless Control of Grid-Connected Inverter during Single Phase Disconnection after Single Phase Fault in a Weak Grid," *IEEJ Journal of Industry Applications*, Vol. 7, No. 6, pp. 506-516, 2018.

[9] H. Chen, C. Lee, P. Cheng, R. Teodorescu and F. Blaabjerg, "A Low-Voltage Ride-Through Technique for Grid-Connected Converters With Reduced Power Transistors Stress," *IEEE Trans. Power Electron*., Vol. 31, No. 12, pp. 8562-8571, 2016.

[10] S. Nagai, K. Kusaka, J. Itoh, "FRT Capability of Single-phase Gridconnected Inverter with Minimized Interconnected Inductor", *in Proc. IEEE Appl. Power Electron. Conf. and Expo.* (*APEC*) *2017*, pp. 2802-2809, 2017.

[11] M. Tsili, S. Papathanassiou, "A review of grid code technical requirements for wind farms", *IET Renew. Power Gener*., Vol. 3, No. 3, pp. 308-332, 2009.

[12] *RPI-M20A*, Delta Electronics, Inc., Taipei, Taiwan. 2014. [Online]. Available: http://www.deltaww.com/fileCenter/Products/Download /05/ 0501/RPI-M20A_TechData_20141126.pdf

[13] T. Ito, A. Kikuchi, M. Taniguchi, Y. Takemoto, and M. Ichinose, "Disturbance-robust Current Control Technique for Large-scale PV Inverter," *IEEJ Journal of Industry Applications*, Vol. 8, No. 2, pp. 314-321, 2019.

[14] S. Nagai and J. Itoh, "FRT Capability of Three-phase Grid-tied Converter with Minimized Inductor", *in Proc. IEEE Appl. Power Electron. Conf. and Expo.* (*APEC*) *2019*, pp. 1070-1077, 2019.

[15] N. Hoffmann, M. Hempel, M. C. Harke and F. W. Fuchs, "Observer-based Grid Voltage Disturbance Rejection for Grid Connected Voltage Source PWM Converters with Line Side LCL filters", *in Proc. IEEE Energy Conversion Congress and Expo.* (*ECCE*), 2012, pp. 69-76.

[16] K. Lee, T. M. Jahns, T. A. Lipo, V. Blasko and R. D. Lorenz, "Observer-Based Control Methods for Combined Source-Voltage Harmonics and Unbalance Disturbances in PWM Voltage-Source Converters", *IEEE Trans. Ind. Appl*., Vol. 45, No. 6, pp. 2010-2021, 2009.