Switching Device Number Reduction for Three-Phase Cascade-Modular Solid-State Transformer System with Employment of Three-Phase T-Type Converter

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Abstract—This paper proposes a three-phase cascade-modular solid-state-transformer (SST) system employed with a three-phase T-type converter to reduce the switching device number. A conventional three-phase SST system requires three single-phase SST subsystems, whereas the proposed three-phase SST system requires only two single-phase SST subsystems due to the application of the three-phase T-type converter. The operation of the proposed three-phase SST system is confirmed by both simulation and experiment. In the simulations, the three-phase SST system with the input voltage of 6.3 kV and the output voltage of 400V is evaluated. The unity power factor operation and the low grid current total distortion harmonic (THD) of 0.96% is achieved, where the output current with low current ripple is also achieved, satisfying the condition of the grid quality. In the experiments, the grid currents with high current THD of about 13.0% is obtained.

Keywords—DC grids, solid state transformers, three-phase T-type converter

I. INTRODUCTION

Nowadays, power grids face many challenges with an increasing employment of renewable energy sources. Solid-State Transformer (SST) is considered as an enabling technology for "Energy Internet", which provides full control of power flow and protection against disturbances caused by such renewable energy sources. One of the SST applications is the interface between medium voltage AC grids and low voltage smart-grids. Several SST topologies has been considered for this application [1]-[17].

Input-Series-Output-Parallel (ISOP) structure is generally employed due to the properties of the application where the input is high voltage / low current and the output is low voltage / high current. In [1]-[2], [5], the ISOP structure is applied for the SST system with the input of the single-phase medium-voltage AC grid. Similarly, three single-phase SST systems connecting in a delta connection can be employed in the three-phase medium-voltage AC grid [1], [5]. However, this three-phase SST system faces many drawbacks, one of which is a high number of switching devices.

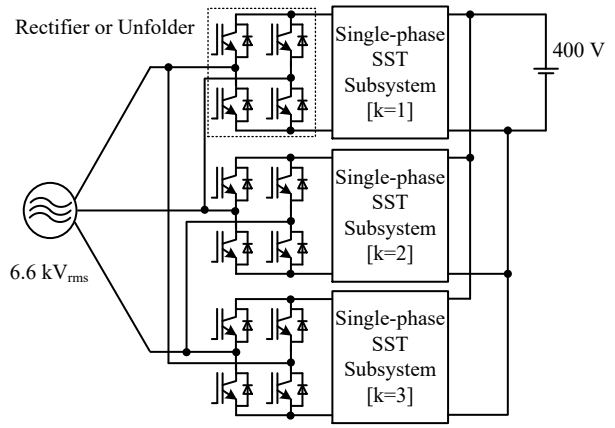
On the other hand, the SWISS Rectifier, or three-phase T-type converter in bidirectional operation mode, converts the input of three phases into the output of two phases, i.e. the phase between the maximum-to-medium phase, and the medium-to-minimum phase. This conversion is accomplished by the low switching frequency of the switching devices in the three-phase T-type converter, reducing significantly the switching loss. Therefore, many application of the three-phase T-type converter taking advantage of this property have been proposed [18]-[20]. Nevertheless, this property of the three-phase T-type converter has not been employed into the three-phase SST system to reduce the switching device number.

This paper proposes a three-phase cascade-modular SST system employed with a three-phase T-type converter to reduce the switching device number. The original idea of this paper is the employment of the three-phase T-type converter with low switching frequency operation into the three-phase cascade-modular SST system. In particular, the high voltage rating devices in the three-phase T-type converter is operated at twice the grid frequency, leading to a significant switching loss reduction. The simulation and experimental results confirm the operation of the proposed system.

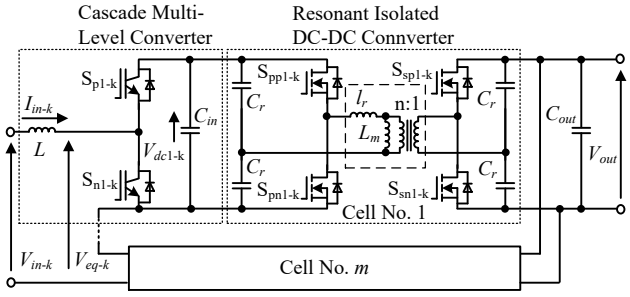
II. CIRCUIT TOPOLOGY

Fig. 1 depicts the conventional and proposed three-phase cascade-modular SST systems. First, in the conventional system, three rectifiers are connected to the three-phase medium-voltage AC grid in a delta connection. The rectifier converts line-to-line AC voltages to full-wave-rectification waveforms, which are input into single-phase SST subsystems.

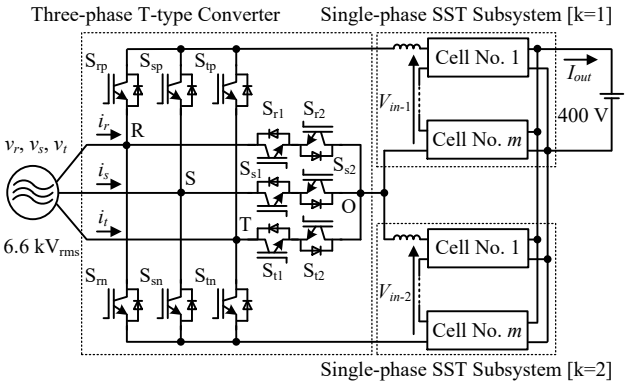
Second, the ISOP structure is employed in the single-phase SST subsystem consisting of a cascade multi-level converter and multiple resonant isolated DC-DC converters. The cascade multi-level converter regulates the input current I_{in} into the full-wave-rectification waveforms similarly to the operation of the typical Power-Factor-Correction (PFC) converter. Thanks to the multi-level topology, low switching frequency in each cell still results in a high



(a) Conventional three-phase cascade-modular SST system



(b) Single-phase SST subsystem



(c) Proposed three-phase cascade-modular SST system

Fig. 1. Conventional and proposed three-phase cascade-modular SST systems.

equivalent-frequency in the current ripple, leading to a minimization of an input inductor without increasing switching loss.

Third, DC-link in each cell is connected with the resonant isolated DC-DC converter. The series-series resonance compensation is selected for this DC-DC converter due to the employment of a loosely-coupled transformer, which enables the integration of the auxiliary inductor l_p into the transformer. The resonant isolated DC-DC converter can achieve Zero-Voltage Switching (ZVS) at turn-on of the switching devices, reducing the turn-on switching loss [21]. One of the main drawbacks of the conventional system is the high number of switching devices due to the requirement of three single-phase SST subsystems.

On the other hand, the proposed three-phase cascade-modular SST system with the three-phase T-type converter requires only two single-phase SST subsystems. Furthermore, the input voltage $V_{in\text{-}k}$ of the single-phase SST subsystem in the proposed system is lower than that of the conventional system due to a star connection in the proposed system. Consequently, the cell number of the single-phase SST subsystem in the proposed system can also be reduced.

Table I shows the comparison of switching device number between the conventional and proposed three-phase cascade-modular SST systems. Note that the high-voltage-rating switching devices of the three-phase T-type converter in the proposed system are same as those of three rectifiers in the conventional system. Besides, the high-voltage-ratings switching devices can be constructed by the series connection of several Si-switching devices. Note that the low switching frequency of the switching devices in the three-phase T-type converter also results in the small snubber loss when the CR snubbers are connected in parallel with the series-connected switching devices. Furthermore, the number of cell is calculated by the voltage rating of the switching devices and the input voltage $V_{in\text{-}k}$ of the single-phase SST subsystem. It is concluded from Table I that the proposed system reduces the number of the switching devices by over 40% in any selection of the voltage rating. Note that S_{rp}, S_{rn}, S_{sp}, S_{sn}, S_{tp} and S_{tn} can be employed with the diode if only the unidirectional power flow is required.

III. Control Method

A. Switching pulse generation for three-phase T-type converter

Fig. 2 depicts the switching pulse generation for the three-phase T-type converter, whereas Table II shows the switching table. In this digest, the three-phase T-type converter is assumed to operate at unity power factor with powering mode; therefore, S_{rp}, S_{rn}, S_{sp}, S_{sn}, S_{tp}, and S_{tn} are always turned off. Next, the phase with the mid amplitude compared to two other phases is connected to point O. In particular, six states are determined from the relationship among three phase voltages as shown in Fig. 2(a); then, the switching pulses are generated based on the state numbers as shown in Fig. 2(b) and Table II. Consequently, the high-voltage-rating IGBTs S_{r1}, S_{r2}, S_{s1}, S_{s2}, S_{t1}, and S_{t2} are switched at only twice the grid frequency, leading to the significant switching loss reduction.

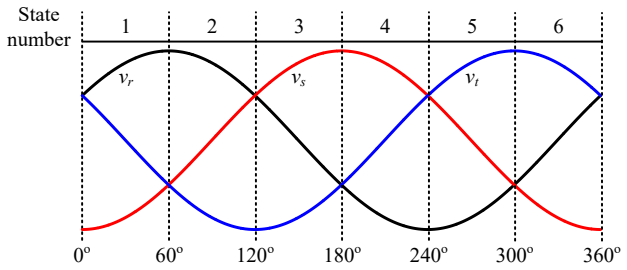
B. Control system of single-phase SST subsystem

The control system of the single-phase SST subsystem consists of the feedback current control for the cascade multi-level converter and the open loop control for the resonant isolated DC-DC converter.

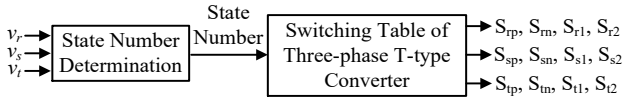
TABLE I

COMPARISON OF SWITCHING DEVICE NUMBER BETWEEN CONVENTIONAL AND PROPOSED THREE-PHASE SST SYSTEMS.

Voltage Rating	Cell Number		Number of Switching Device	
	Conv. SST	Prop. SST	Conv. SST	Prop. SST
650 V	24	21	432	252
1.2 kV	13	11	234	132
1.7 kV	9	8	162	96
3.3 kV	5	4	90	48



(a) Relationship between phase voltages and state number



(b) Switching pulse generation

Fig. 2. Switching pulse generation for three-phase T-type converter.

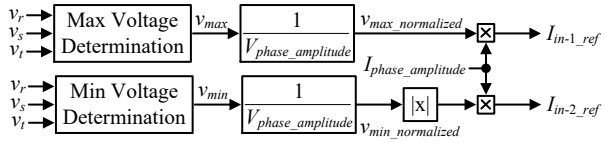
TABLE II

SWITCHING TABLE OF THREE-PHASE T-TYPE CONVERTER.

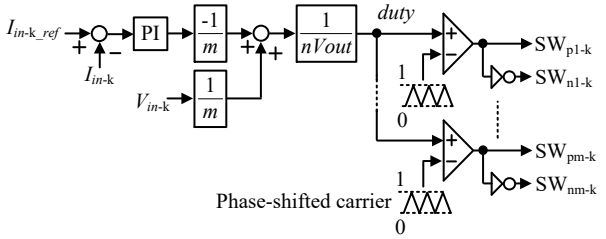
State no.	S_{r1}, S_{r2}	S_{s1}, S_{s2}	S_{t1}, S_{t2}	S_{rp}, S_{rn}, S_{sp}, S_{sn}, S_{tp}, S_{tn}
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0
4	0	0	1	0
5	0	1	0	0
6	1	0	0	0

Fig. 3 depicts the control block diagram of the feedback current control for the cascade multi-level converter. In Fig. 3(a), first, the maximum and minimum voltages v_{max}, v_{min} among v_r, v_s, v_t in each states are determined. Then, v_{max}, v_{min} are divided by the phase voltage amplitude to obtain the normalized maximum and minimum voltages $v_{max\_normalized}$, $v_{min\_normalized}$. Next, $v_{max\_normalized}$ is multiplied with the grid current amplitude $I_{phase\_amplitude}$ to generate the input current command of the first single-phase SST subsystem $I_{in\text{-}1\_ref}$, whereas the absolute value of $v_{min\_normalized}$ is multiplied with $I_{phase\_amplitude}$ to generate the input current command of the second single-phase SST subsystem $I_{in\text{-}2\_ref}$.

The PI controller is employed in the feedback current control system as shown in Fig. 3(b). The output of the PI controller is divided by the number of cells m due to the



(a) Current command generation



(b) Feedback current control system

Fig. 3. Control block diagram of feedback current control for cascade multi-level converter.

TABLE III

SIMULATION PARAMETERS.

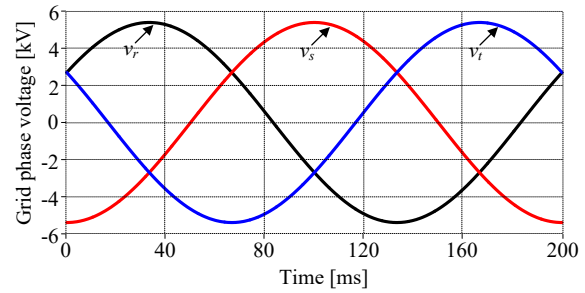
Parameters	Symbols	Values
Line-to-line grid voltage	v_g	6.6 kV_{rms}
Rated output apparent power	S_{out}	45 kVA
Grid frequency	f_g	50 Hz
Rated output voltage	V_{out}	400 V
Device voltage rating	V_{DS}	1.7 kV
Number of cells	m	8
Boost inductor	L (%Z)	5 mH (0.16%)
Primary side capacitor	C_{in}	40 µF
Transformer turn ratio	n:1	2.55:1
Sw. freq. multi-level converter	f_{sw_multi}	12 kHz
Sw. freq. isolated converter	f_{sw_iso}	48 kHz

characteristic of the multi-level operation. Then, the input voltage of each single-phase SST subsystem $V_{in\text{-}k}$ is feed forward to compensate for the disturbance. The result is divided by the multiplication of the output voltage V_{out} and the turn ratio n of the transformer. Finally, the switching pulses are generated by the comparison between the duty and the carriers. Note that phase of each carriers in each cell is shifted to further reduce the current ripple.

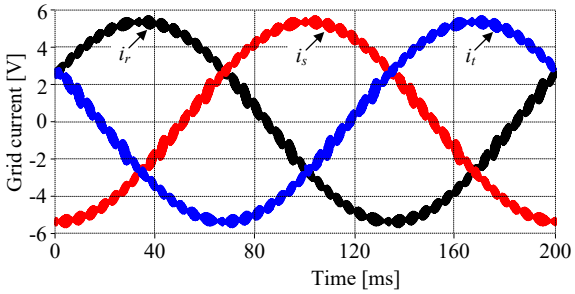
Meanwhile, the voltage control for the primary side capacitor C_{in} in each cell is unnecessary in this system. The voltage of the primary side capacitor V_{dc1_k} might become imbalanced due to the variation of C_{in}. Nevertheless, the parallel connection of the resonant isolated DC-DC converter, whose duty ratio of each switch in one leg is kept constant at 50%, clamps the average value of V_{dc1_k} to nV_{out}. Consequently, the voltage control for C_{in} is not required.

IV. SIMULATION RESULTS

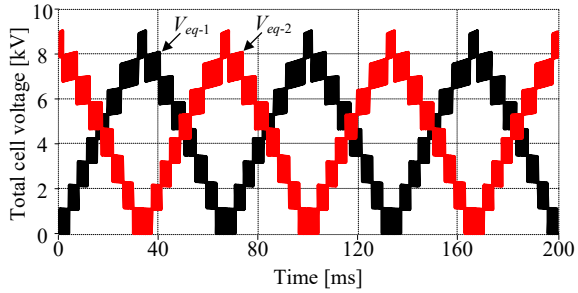
Table III shows the simulation parameters. The proposed three-phase SST system is adopted with a three-phase 6.6-kV AC grid, whereas the power rating of the system is 45 kVA. Note that the switching devices with the voltage rating of 1.7 kV are employed in the proposed three-phase SST system.



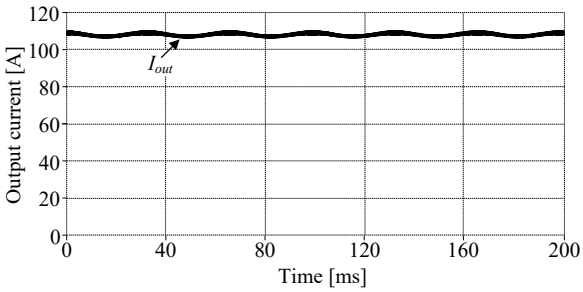
(a) Grid phase voltages



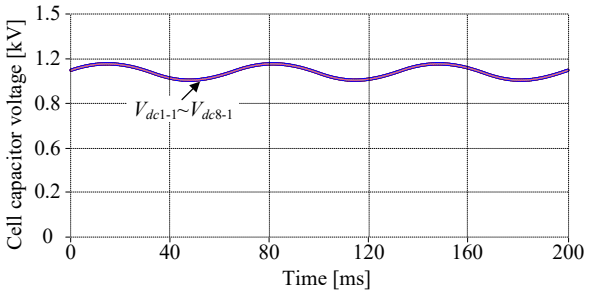
(b) Grid currents



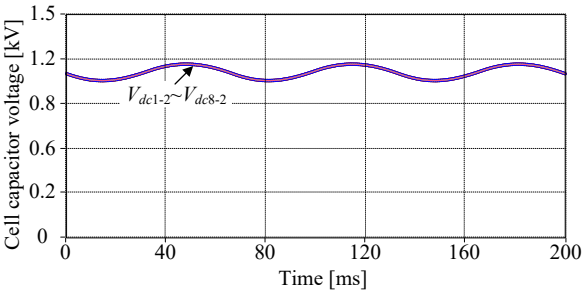
(c) Total cell voltages



(d) Output current



(e) Cell voltages of first single-phase SST subsystem



(f) Cell voltages of second single-phase SST subsystem

Fig. 4. Operation of proposed three-phase SST system.

Fig. 4 depicts the operation of the proposed SST system. Fig. 4(a)-(f) shows the grid phase voltages v_r~v_t, the grid currents i_r~i_t, the total cell voltages $V_{eq\text{-}1}$, $V_{eq\text{-}2}$, the output current I_{out}, and the cell voltages of the first and second single-phase SST subsystems $V_{dc1\text{-}1}$~$V_{dc8\text{-}1}$, $V_{dc1\text{-}2}$~$V_{dc8\text{-}2}$, as shown in Fig. 1(b)-(c), respectively. According to Fig. 4(a)-(b), the unity power factor operation and the low grid current total distortion harmonic (THD) of 0.96% are achieved. Note that in the simulation, the input filters have not been considered, leading to the remaining current ripple in the grid currents; furthermore, the current THD is calculated up to 40th harmonic component. In Fig. 4(c), the multi-level waveforms of total cell voltages $V_{eq\text{-}1}$, $V_{eq\text{-}2}$ are clearly observed, resulting in the high current-ripple equivalent-frequency despite of the low switching frequency of the switching devices in each cell. In Fig. 4(d), the constant output current I_{out} with very low current ripple is observed. Note that in the simulation, the output filter has also not been considered. The carrier phase shifting of the resonant isolated DC-DC converter in each cell contributes to the reduction of the output current ripple, leading to the minimization of the output filter. According to Fig. 4(e)-(f), the cell voltages of both the first and second single-phase SST systems $V_{dc1\text{-}1}$~$V_{dc8\text{-}1}$, $V_{dc1\text{-}2}$~$V_{dc8\text{-}2}$ are maintained stably even without any voltage control. The stable cell voltages are achieved thanks to the parallel connection of the resonant isolated DC-DC converters, clamping the voltage in each cell to the output voltage. It can be observed that the cell voltages consist of a relatively high voltage ripple. The reason is because the primary side capacitor C_{in} is designed with a low capacitance to avoid the requirement of the high-voltage high-capacitance capacitors. As a result, the operation of the proposed three-phase SST system is confirmed with these results.

V. Laboratory Setup

Fig. 5 depicts the experimental circuit diagram and prototype, Table IV shows the experimental parameters, and Fig. 6 depicts the miniature prototype of the three-phase cascade-modular solid-state transformer system with three-phase T-type converter. The miniature prototype is constructed with a three-phase T-type converter and two

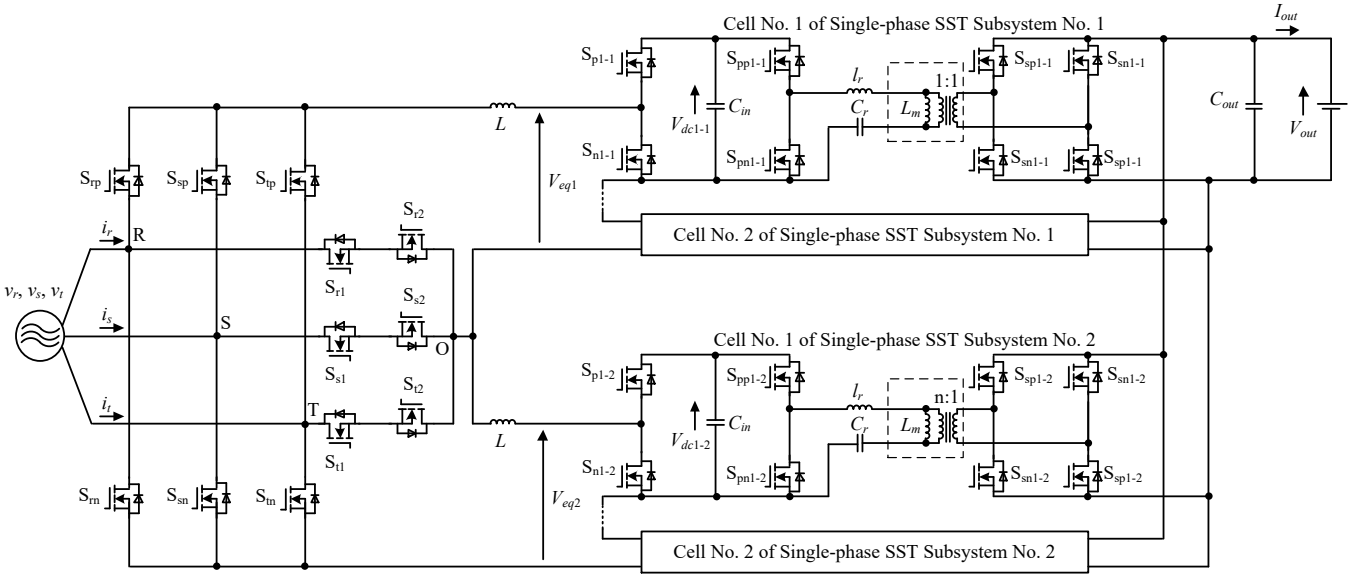


Fig. 5. Circuit diagram of miniature prototype of three-phase cascade-modular solid-state transformer system with three-phase T-type converter.

TABLE IV
EXPERIMENTAL PARAMETERS.

Parameters	Symbols	Values
Line-to-line grid voltage	v_g	120 V_{rms}
Rated output power	P_{out}	0.3 kW
Grid frequency	f_g	50 Hz
Rated output voltage	V_{out}	40 V
Number of cells	m	2
Boost inductor	L	4 mH
Primary side capacitor	C_{in}	50 µF
Output capacitor	C_{out}	1500 µF
Transformer turn ratio	n:1	1:1
Sw. freq. multi-level converter	f_{sw_multi}	20 kHz
Sw. freq. isolated converter	f_{sw_iso}	50 kHz
Switching Device	*SiC Rohm*	*SCT2080KE*

Fig. 6. Miniature prototype of proposed three-phase SST system with one three-phase T-type converter and four cells of single-phase SST subsystem.

single-phase SST subsystems, which have two cells each. Switches S_{rp}, S_{sp}, S_{tp}, S_{rn}, S_{sn}, and S_{tn} are turned off because

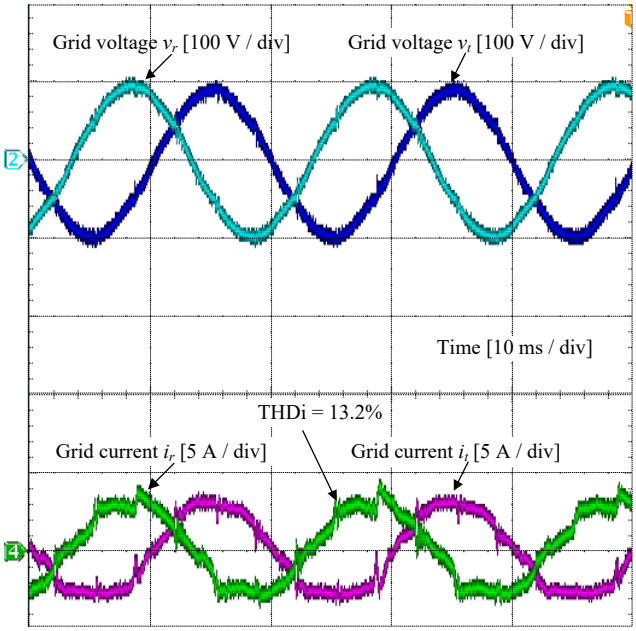
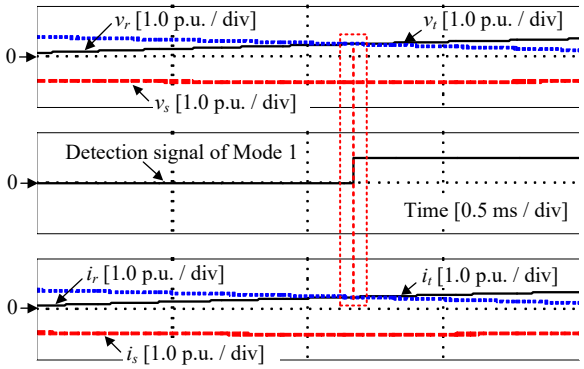


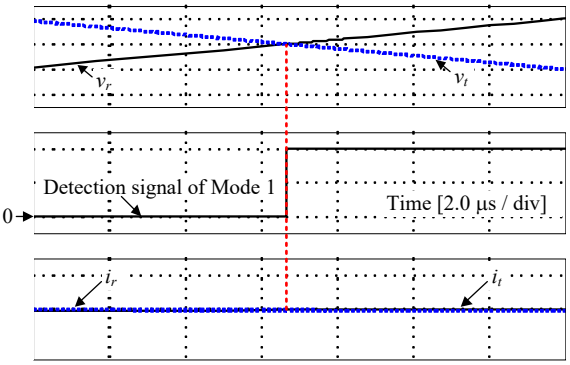
Fig. 7. Operation waveforms of grid voltages and grid currents.

only the powering mode with a unity power factor is operated. The SiC devices from ROHM (SCT2080KE) are employed for all the switches; however, the high voltage rating IGBTs are applied for the switches in the three-phase T-type converter in practical. Note that the primary side capacitor value is much smaller than that of the output capacitor in order to avoid the use of the high-voltage high-capacitance capacitor.

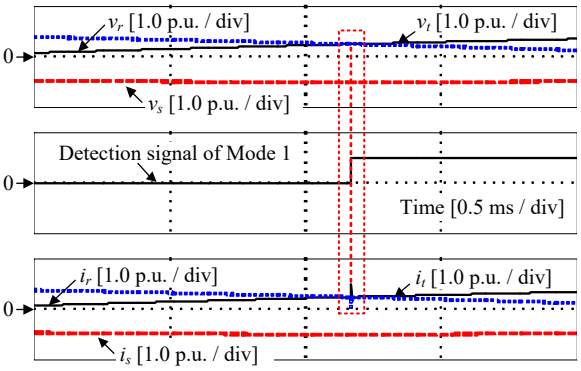
Fig. 7 depicts the operation waveforms of the grid voltages and the grid currents. The same phase between the



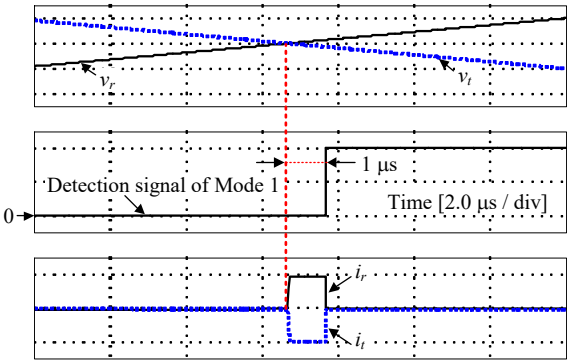
(a) Accurate voltage relationship detection



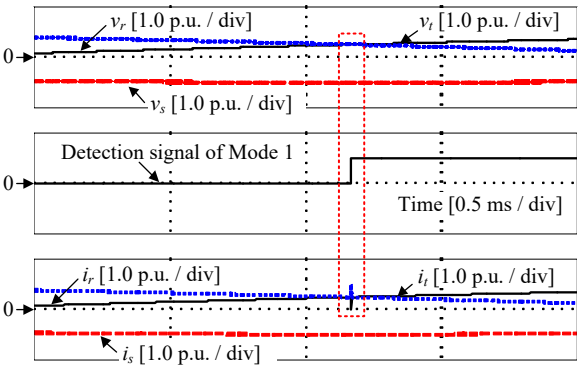
(b) Magnified waveforms of Fig. 8(a)



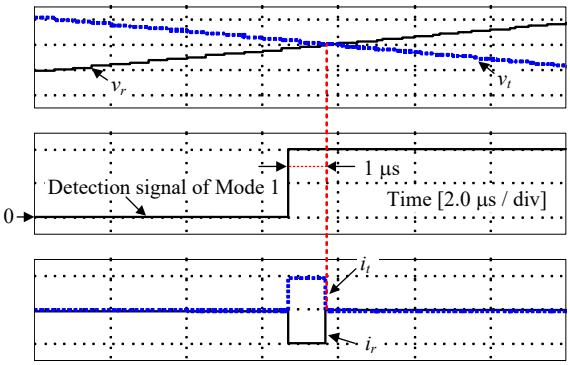
(c) Voltage relationship detection: Lagging



(d) Magnified waveforms of Fig. 8(c)



(e) Voltage relationship detection: Leading



(f) Magnified waveforms of Fig. 8(e)

Fig. 8. Simulated waveforms of grid voltages, detection signal of Mode 1, and grid currents under three cases of voltage relationship detection.

s-phase voltage and s-phase current is confirmed as well as that of the t-phase; this confirms the powering mode operation. It is observed that the grid currents i_r and i_t have relatively high THD of over 13.0%. Note that the current distortion is clearly observed at the changing point of the operation mode shown in Fig. 2(a). The reason of this current distortion is because time delay between the mode detection and the actual grid voltage relationship exists in practical.

Fig. 8 depicts the simulated waveforms of the grid voltages, the detection signal of Mode 1, and the grid currents under three cases of voltage relationship detection. In Fig. 8(a)-(b), there is no time delay between the mode detection and the actual grid voltage relationship; hence the current commutates smoothly among the phases. However, as shown in Fig. 8(c)-(f), the current overshoots when there is time delay between the mode detection and the actual grid voltage relationship, which is set as 1.0 μs in this evaluation. In particular, as shown in Fig. 8(c)-(d), considering the start of Mode 1, when the detection of Mode 1 is lagging compared to the voltage relationship between r-phase and t-phase, it is observed clearly that the current overshoot happens. Similarly, as shown in Fig. 8(e)-(f), when the detection of Mode 1 is leading compared to the voltage

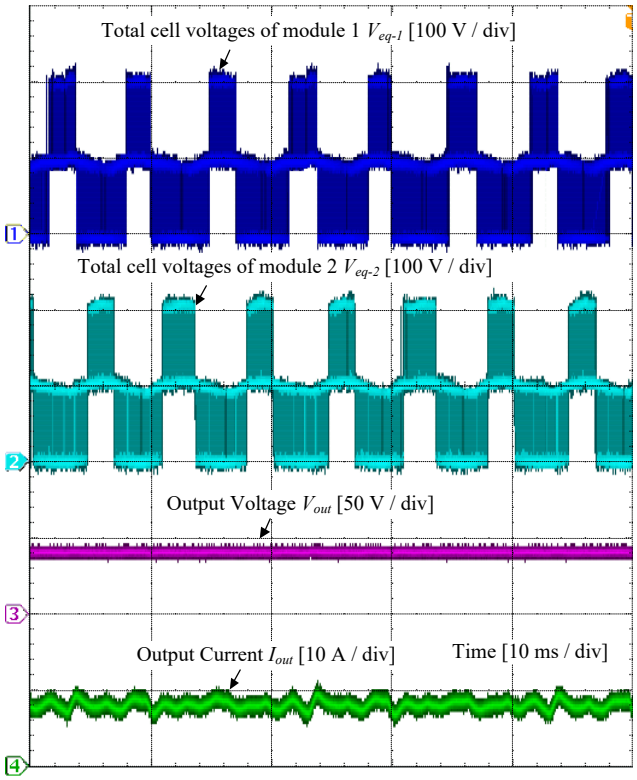


Fig. 9. Operation waveforms of total cell voltages, output voltage and output current.

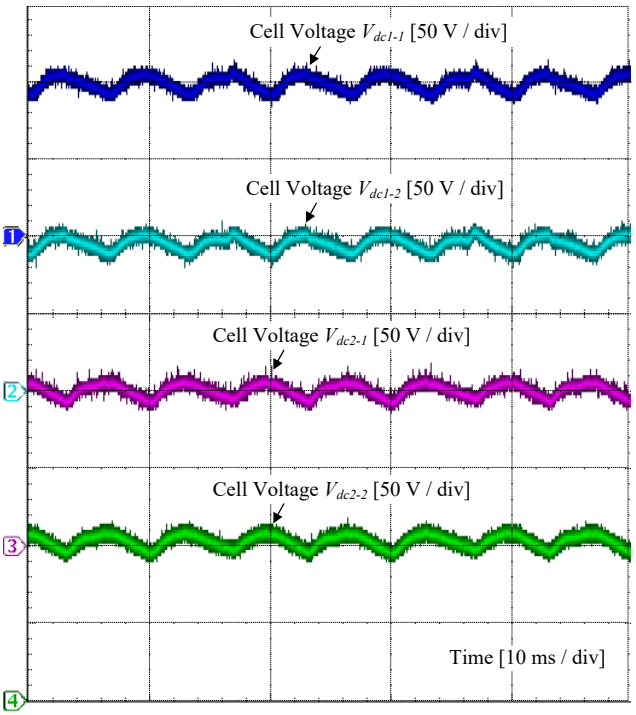


Fig. 10. Operation waveforms of cell voltages.

relationship between r-phase and t-phase, the current overshoot also happens. These current overshoots significantly worsen the grid current THD. In other words, the current overshoots should be avoided to improve the grid current quality. Note that these current overshoots occur due to both the detection delay of the detection board and the commutation delay of the bidirectional switches.

Fig. 9 depicts the operation waveforms of the total cell voltages, the output voltage and the output current. The two-level waveforms of total cell voltages V_{eq-1}, V_{eq-2} are clearly observed, resulting in the high current-ripple equivalent-frequency despite of the low switching frequency of the switching devices in each cell. It is observed that the output current has small ripple. The reason of this ripple is because the high current THD of the grid current, causing the ripple in the input power as well as the output power. The increase of the primary side capacitor in each cell C_{in} greatly contributes to the power decoupling between the input and output, which indicates that the input power ripple does small effects on the output power quality. Nevertheless, this design is against the avoidance of the high-voltage high-capacitance capacitor design.

Fig. 10 depicts the operation waveform of the cell voltages. The cell voltages of both the first and second single-phase SST systems V_{dc1-1}~V_{dc1-2}, V_{dc2-1}~V_{dc2-2} are maintained stably even without any voltage control. The stable cell voltages are achieved thanks to the parallel connection of the resonant isolated DC-DC converters, clamping the voltage in each cell to the output voltage. It can be observed that the cell voltages consist of a relatively high voltage ripple. The reason is because the primary side capacitor C_{in} is designed with a low capacitance to avoid the requirement of the high-voltage high-capacitance capacitors.

Fig. 11 depicts the operation waveforms of the r-phase grid voltage, and the three-phase T-type converter gate signals. It is clearly observed that the switching devices of the three-phase T-type converter are switched at very low switching frequency, i.e. twice the grid frequency. Hence, the high-voltage-rating IGBTs can be employed into the three-phase T-type converter without introducing high switching loss. This approach significantly decreases the switching device number compared to the full-bridge converter approach.

VI. Conclusion

This paper proposed the three-phase cascade-modular SST system employed with the three-phase T-type converter to reduce the switching device number. In particular, the high voltage rating devices in the three-phase T-type converter was operated at twice the grid frequency, leading to the significant switching loss reduction. Furthermore, only two single-phase SST subsystems were required in the proposed three-phase SST system compared to three of that in the conventional three-phase SST system. Besides, the cell number in each single-phase SST subsystem of the proposed three-phase SST system was lower than that of the conventional three-phase SST system. Consequently, the proposed three-phase SST system reduced the switching device numbers by over 40% in any selection of the voltage rating compared to that of the conventional three-phase SST system. The operation of the proposed three-phase SST

system was confirmed in both the simulations and experiments.

In the simulations, the three-phase SST system with the input voltage of 6.3 kV and the output voltage of 400V was evaluated. The unity power factor operation and the low grid current total distortion harmonic (THD) of 0.96% were achieved, where the output current with low current ripple was also achieved, satisfying the condition of the grid quality. In the experiments, the grid currents with high current THD of about 13.0% was obtained. This high current THD was caused by the misdetection between the operation mode and the grid voltage relationship. In future works, the improvement of the current THD will be focused. Furthermore, the design of the prototype with high input voltage will be evaluated.

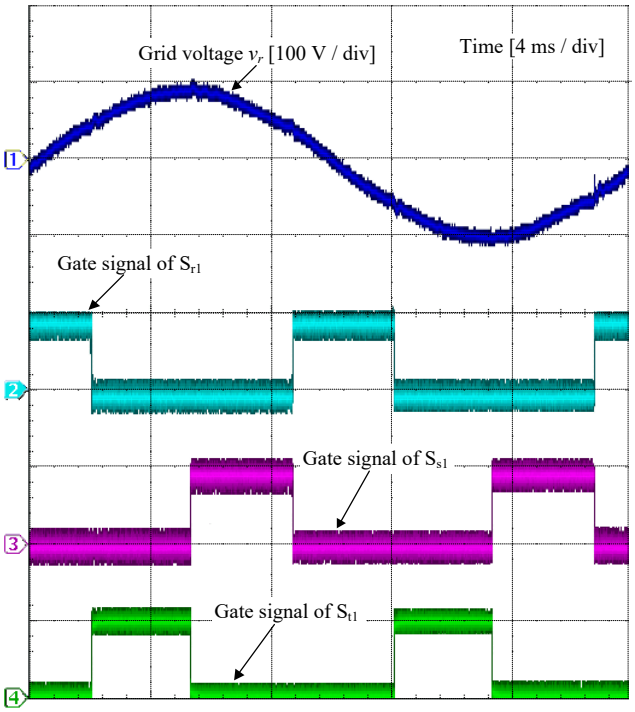


Fig. 11. Operation waveforms of r-phase grid voltage, and three-phase T-type converter gate signals.

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