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Paper

Development of Solid-State Transformer for 6.6-kV single-phase grid with Automatically Balanced Capacitor Voltage

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This paper proposes a solid-state transformer (SST) for a 6.6-kV single-phase grid using multiple cells, which have a power factor correction stage and an isolated DC-DC converter. In the SST, the capacitor voltage of each cell is automatically balanced on a primary side owing to the use of a resonant DC-DC converter. The main topic of this paper is calculating the fundamental loss of the proposed topology assuming a 6.6-kV single-phase grid. From the calculation, the maximum efficiency of the full model SST reaches 99%. The scaled model with an input voltage of 1320 V, which is 1/5 of the full model, is tested to confirm the calculation of the power loss and fundamental operation. As a result, it is confirmed that the input current is sinusoidal and a total harmonic distortion is 4.3%. Moreover, the automatic capacitor voltage balancing capability is tested. The capacitor voltage on each cell is automatically balanced without any control for voltage balance. Besides, the bidirectional operation is verified. Finally, the power loss of the proposed topology is separated into each conversion part. The power loss shows a good agreement with the calculation with an error of less than 5%.

Keywords : Solid-State Transformer, Power factor correction converter, Resonant DC-DC converter, High-frequency transformer

1. Introduction

In recent years, DC distribution systems have been actively studied to save the power consumption of data-centers or large buildings[1-2]. The DC distribution systems have a capability of downsizing and efficient conversion in comparison with an AC distribution system because the number of power conversion will be decreased[3]. In such a DC distribution system, a 6.6-kV AC grid is employed as one of the power sources.

A transformer is employed for the DC distribution system with the AC power grid for achieving the step-down from 6.6 kV to the distribution voltage of several hundred volts. The transformer plays a role as galvanic isolation between the DC distribution system and the AC power grid [4–5]. Generally, the conventional transformer which is used at the grid frequency, e.g., 60 Hz or 50 Hz is bulky and heavy.

As one of the solutions to downsizing the isolation stage, a transformer-less PWM converter is proposed [6]. The high voltage IGBTs with the voltage rating more than 4.5 kV are required in a five-level diode-clamped converter. The five-level diode-clamped converter requires the balancing circuit as the auxiliary circuit in order to balance the capacitor voltage in the DC link. Besides, the five-level diode-clamped converter is operated with a low switching frequency because the loss of high voltage rating devices is large compared to low voltage rating devices. The operation in low-switching frequency results in large passive components because harmonic distortion of input current and voltage ripple of output DC voltage should be suppressed.

As another solution, solid-state transformers (SST) have much attention[7–9]. SSTs achieve significant volume reduction of the converter in comparison with the low-frequency transformer by high-frequency switching using the characteristics of wide-bandgap semiconductors, e.g., silicon carbide (SiC) and gallium nitride (GaN) devices [10]. Moreover, the use of high-frequency transformer for isolation and the step-down function provides the advantage to the SST in terms of the downsizing. SST has the following advantages in consequence[11]:

- AC voltage adjustment
- DC voltage output
- Reduction in size and weight of the system
- Active and reactive power control
- Low harmonics components in AC side

Furthermore, the converters with cells based on multilevel topologies have advantages because it enables to reduce the required voltage rating of the switching devices. Thus, the switching devices with low on-state resistance and high-speed switching can be used. In addition, the switching frequency is equivalently increased by the multilevel topology. Thus, the size of the inductors in the converter can also be reduced[12].

One of the problems of the multilevel topology is the number of switches. The number of switches greatly increases owing to the multiple cells. In addition, the control system driving the main circuit will be complicated since the number of the gate signal will be increased with an increased number of the switch[13]. Moreover, a balance control for each capacitor on the cells must be employed in the multilevel converters such as a modular multilevel converter (MMC)[14]. The balance control may cause an unstable if a feedback control has a delay due to isolation or signal transmission[15]. Furthermore, the DC link capacitor with a large capacitance is required to maintain the capacitor voltage on each cell[16].

This paper proposes a simple circuit configuration of the single-

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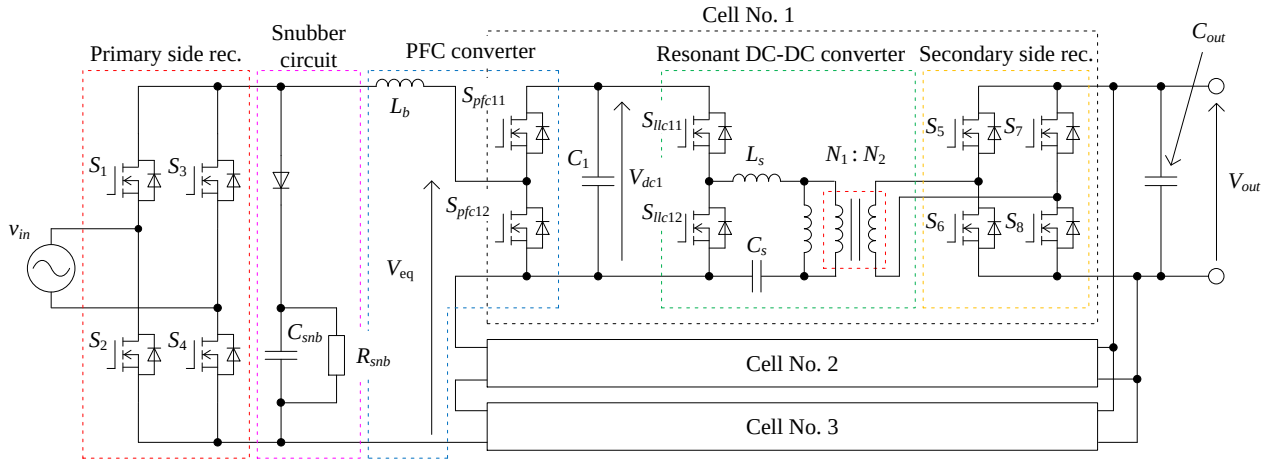

Fig. 1. Circuit configuration of proposed bidirectional single-phase SST.

phase SST. The proposed SST has the automatic voltage balancing capability without a complex voltage balance control with a small primary side capacitor. In the proposed SST, the number of devices is smaller than the conventional SST because a single-phase rectifier is employed for all of the cells. Moreover, the effect of reducing the number of devices increases according to the number of cells. The originality of this paper is proposing the new topology of the SST, which has an automatic voltage balancing capability using an open-loop controlled resonant DC-DC converter. By connecting the resonant DC-DC converter with an open-loop control in parallel on the secondary side, the DC-link voltage on each cell is automatically balanced. Thus, a small capacitor on the primary side in comparison with the conventional SST is used because the proposed circuit decouples a power pulsation at twice the grid frequency in the secondary side. The proposed SST in this paper makes the control simple. The proposed SST has been tested with a unidirectional miniature model with the input voltage of 200 V. The fundamental operation had been demonstrated in (17) by authors. In this paper, the proposed SST is experimentally tested under a derated voltage of 1320 V, which is 1/5 of the full model. Moreover, the bidirectional operation is demonstrated in this paper. Additionally, the equations for a calculation of the power loss is derived for separating the power loss of the proposed SST. The validity of the equations is confirmed with the experimental result with the prototype. Then, the proposed SST is designed for a 6.6-kV grid as the input voltage.

2. The system configuration of Proposed SST

2.1 Circuit configuration Figure 1 shows the circuit configuration of the proposed SST. At the primary side, the full-bridge rectifier with switches with the high-voltage rating is connected. These switches are switched at the grid frequency, so the high-voltage switched can be used even if the switching speed of the high-voltage switches is slow. The characteristic of the proposed topology is the SST has the full-bridge rectifier in the input stage. The power factor correction (PFC) is ensured by the full-bridge rectifier and each chopper cell connected in series. The PFC circuit controls the input current to the sinusoidal waveform with the unity power factor. For this reason, the voltage per cell is reduced. Consequently, it is possible to apply the switching device with a low voltage rating and low on-state resistance on the primary side. In each cell, the resonant DC/DC converter is employed. The resonant DC-DC converter is operated in high-frequency for the downsizing the transformer. Moreover, the duty ratio of the resonant DC-DC converter is operated in fixed duty. Thus, the switching loss is small by the zero-current switching.

Table 1. Comparison of switching device between conventional SST and proposed SST.

Rated Voltage	Number of cell	Number of Switching devices	
		Conventional SST (PWM rec. + DAB)	Proposed SST
3.3 kV	6	72	52
1.7 kV	11	132	92
1.2 kV	16	192	132

In general SST topology, a large capacitor should be used in the primary side as the DC-ling capacitor to smooth the DC-link voltage. By contrast, small capacitors are used because the proposed circuit decouples a power pulsation at twice the grid frequency in the secondary side in this system.

Table 1 shows the comparison of the number of switches between the conventional SST, which includes a PWM rectifier and a dual active bridge converter[18] and the proposed SST and. Note that the number of cells is calculated from each rated voltage of the switches with considering the voltage margin. As shown in Table 1, the number of devices is reduced by 30% in comparison with the conventional SST because the proposed SST save the number of switched using one rectifier on the primary side. Consequently, the proposed circuit increases the utilization rate of the circuit compared to the MMC.

2.2 Control system Figure 2 shows the control block diagram of the proposed SST. The control block diagram has an automatic current regulator (ACR) for the current control of the boost inductor. The ACR controls the inductor current into full wave rectified waveform synchronized with the rectified input voltage to achieve a PFC operation. The inductor current command I_L^* is given by

$$I_L^* = I_{amp}\left|\sin(\omega t)\right| \quad \text{.....(1)},$$

where I_{amp} is the amplitude command value of the boost inductor current. The inductor current command I_L^* is generated by the

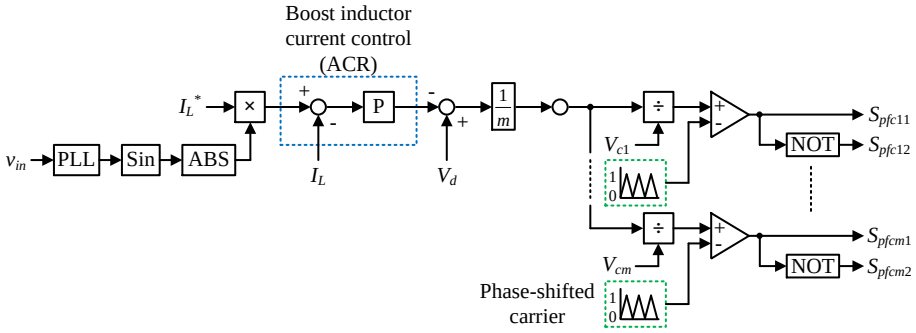

Fig. 2. Control block of PFC converter in proposed circuit.

multiplication of I_{amp} and the full-wave rectified waveform in phase to the input voltage.

The gate signal for PFC is generated by phase shifted carriers of a triangular wave. Thus, the input voltage is equally divided because the switching timing is different. In addition, low voltage switches can be used. Note that the ripple current is reduced because the inductor voltage is reduced by the series connection in the PFC converter. Then, the phase shift angle θ is given by

$$\theta = \frac{2k}{m}\pi \ (k = 0, 1, \cdots, m-1) \quad \text{.....(2).}$$

Meanwhile, the proposed topology does not need the balance control of the capacitor on the primary side V_{dc1}. The voltage of the primary side capacitor may be imbalanced owing to a difference of transient response or variation of capacitances in general multilevel topology. However, DC-link voltage of each cell is automatically balanced because the resonant DC-DC converters, which is operated with the constant duties are connected in parallel on the secondary side. Consequently, the capacitor voltage on the primary side is naturally clamped by the voltage, which is determined by the turn ratio and the secondary voltage because the cell with high DC-link voltage will supply much power than the cell with low voltage. Thus, capacitor voltage management on the high-voltage side is not required.

Figure 3 shows the switching pulse generation of the primary side rectifier. The switching pulse is generated by comparing the input voltage v_{in} and the thresholds voltage of positive/negative (V_{thp}/V_{thn}). The switching states are the following:

- $v_{in} > V_{thp}$
  Switches S_1 and S_4 are a turn-on
  Switches S_2 and S_3 are a turn-off
- $v_{in} < V_{thn}$
  Switches S_2 and S_3 are a turn-on
  Switches S_1 and S_4 are a turn-off
- $V_{thn} < v_{in} < V_{thp}$
  All of switches S_1, S_2, S_3, and S_4 are a turn-off

During the period, all of switches $S_{1\text{-}4}$ are a turn-off, the input current commutates into the body diode of MOSFETs in the power running operation. In contrast, the current flows to the snubber circuit during the regeneration mode.

Table 2 shows the switching state of the rectifier on the primary side, the resonant DC-DC converter, and the rectifier on the secondary side. In the rectifier on the primary side, the switching frequency is the same as the grid frequency in order to achieve the polarity inversion. In the resonant DC-DC converter, the switching frequency is set to the resonant frequency for the ZCS operation,

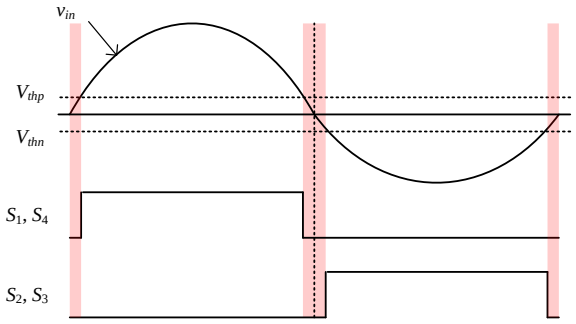

Fig. 3. Pulse generation for primary side rectifier.

Table 2. Switching mode of
resonant DC-DC converter and rectifier.

	$S_1 \sim S_4$	$S_{llc11} \sim S_{llc12}$	$S_5 \sim S_8$
Switching frequency	50 Hz	50 kHz (= f_o)	
Duty ratio	50%		

and the switches are modulated with a duty ratio of 50%. Hence, the resonant DC-DC converter is operated with the open-loop control with constant duty. Thus, the control is simple in this system because the current control is achieved by only the switches of PFC (S_{pfc}). In the rectifier on the secondary side uses the synchronized switching pulse with the resonant DC-DC converter.

3. Design of Proposed SST

3.1 Snubber circuit A snubber circuit is used for both the powering operation and the regeneration operation in the proposed SST. During the regeneration operation, the continuous current flow is ensured by the snubber circuit. In other words, the boost inductor current commutates into the snubber circuit during the dead time. The snubber circuit has to absorb all energy stored in the boost inductor when all of the switches are a turn-off with an over-current detection. Thus, the capacitor of the snubber circuit should be larger as expressed by

$$C_{snb} \geq \frac{L_b I_{\max}^2}{\Delta V^2} \quad \text{.....(3),}$$

where ΔV is the voltage rise of the capacitor, and I_{max} is current at an over-current detection. The resistor of the snubber circuit is given by

$$R_{snb} \le \frac{2V_{clamp}^{\ 2}}{L_b I_{\max}^2 f_{sw\_rec}} \quad \text{.....(4),}$$

where V_{clamp} is the clamp voltage, f_{se_rec} is the switching frequency of the rectifier on the primary side. The clamp voltage is designed to have a margin concerning the rated voltage of the device. In the miniature model SST, the margin is 20%.

3.2 Power-factor-correction (PFC) converter The boost converter on each cell is used for the PFC operation. The boost inductor current is controlled into full-wave rectified waveform as same as general PFC circuit[19–20]. The boost inductor L_b in the PFC circuit is given by

$$L_b = \frac{\sqrt{2}V_{in}}{4 f_{eq} \Delta I_{Lb}} \quad \text{.....(5),}$$

where f_{eq} is the equivalent switching frequency of the output voltage V_{eq}, and ΔI_{Lb} is the ripple current of the inductor current, and. Then, the equivalent switching frequency f_{eq} is given by

$$f_{eq} = m \times f_{sw} \quad \text{.....(6),}$$

where f_{sw} is the switching frequency of the PFC circuit, m is the number of cells. Each cell is modulated with the phase-shifted carrier each other. Consequently, the switching frequency component in V_{eq} is increased in proportional to the number of cells. Thus, the size of the boost inductor is reduced because the inductance is inversely proportional to frequency.

3.3 Resonant DC-DC converter The galvanic isolation is ensured by the resonant DC-DC converter [21]. The high-frequency operation contributes to the minimization of the isolation transformer. In addition, the zero-current switching (ZCS) is achieved by the series resonance between the inductor L_s and the capacitor C_s. ZCS greatly reduce the switching loss of the proposed SST system.

Furthermore, the leakage inductance is designed to be negligibly smaller than the excitation inductance. Then, the switching frequency f_o of the resonant DC-DC converter is given by (7). From resonance frequency, the duty ratio of the switch is 50%.

$$f_o = \frac{1}{2\pi\sqrt{L_s C_s}} \quad \text{.....(7)}$$

In the proposed SST, the operation mode is always the boost operation with respect to the primary side voltage. Thus, the turn ratio of the transformer is designed by (8).

$$N = \frac{N_1}{N_2} \ge \frac{\sqrt{2}V_{in}}{2m\lambda V_{out}} \quad \text{.....(8)}$$

where V_{in} is the input voltage, V_{out} is the output voltage, N_1 and N_2 are the numbers of turns for the primary/secondary side of the high-frequency transformer, and λ is the modulation index of the boost converter.

4. Experimental Results

4.1 Power running operation Table 3 shows the specifications and the circuit parameters. In this experiment, the fundamental operation is tested with the prototype, which has three cells. The input voltage of the prototype is derated to 1320 V which is 1/5 of the full model.

Figure 4 shows the waveforms of the input voltage, the input current, and the output voltage. The operation of the miniature model is confirmed. The input power factor of the proposed SST is unity. The input current THD is 4.3% at the rated load. At the output side, the step-down operation is achieved because the output voltage is regulated to 320 V.

Figure 5 shows voltage changes of the primary DC-link capacitors in each cell when the output power is changed from

Table 3. Circuit parameter of proposed SST for the miniature model

Parameter	Symbol	Value
Input voltage	v_{in}	1320 V_{rms}
Rated output power	P_{out}	2 kW
Rated output voltage	V_{out}	320 V
Snubber capacitor	C_{snb}	0.2 μF
Sunbber resistance	R_{snb}	2.5 MΩ
Boost inductor	L_b	24 mH (%Z = 0.87%)
Primary side capacitor	C_1	48 μF
Resonant capacitor	C_s	204 nF
Leakage inductor	L_s	50 μH
Secondary side capacitor	C_{out}	8200 μF
Switching frequency of rec.	f_{sw_rec}	50 Hz
Switching frequency of PFC	f_{sw_pfc}	10 kHz
Resonant frequency	f_o	50 kHz
Number of cells	m	3
Trans turns ratio	N_1/N_2	1.0

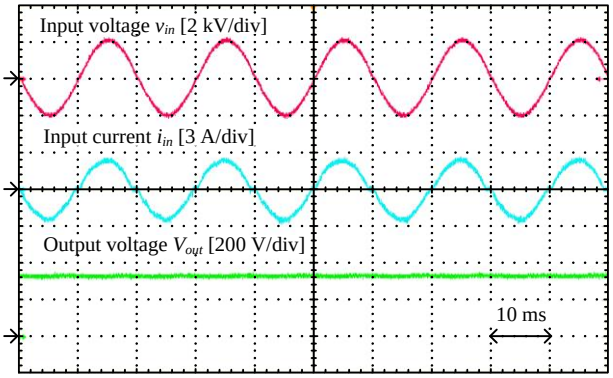

Fig. 4. Operation waveform at power running.

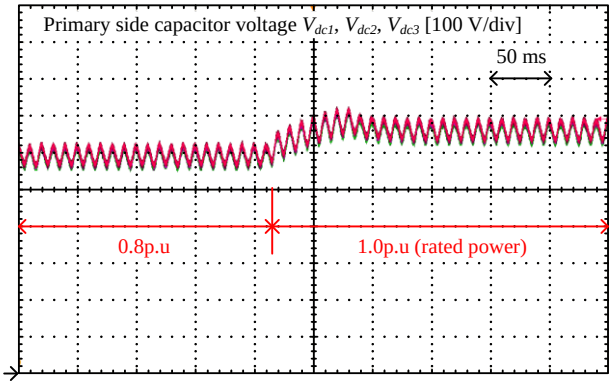

Fig. 5. Primary side capacitor voltage in each cell.

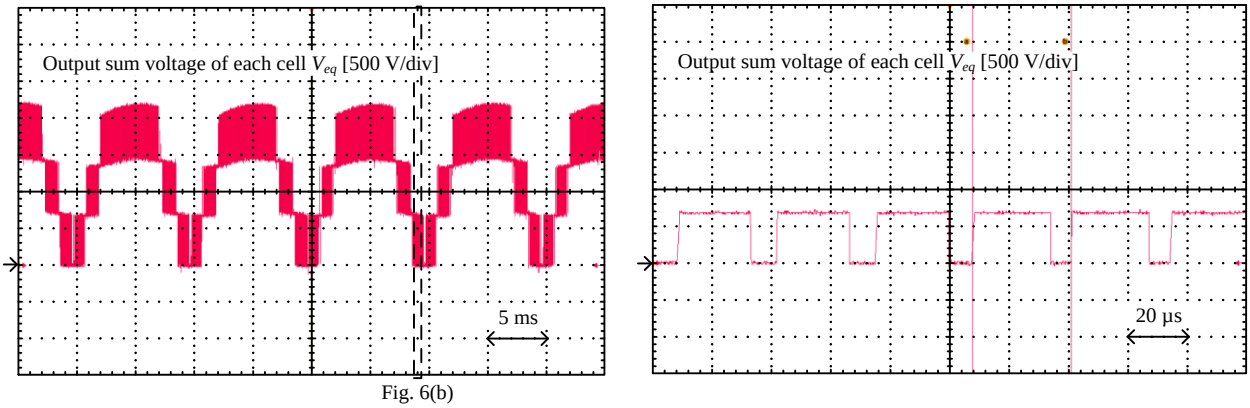

Fig. 6(b)

(a) Whole figure (b) Enlarged figure

Fig. 6. Output voltage of all cells at power running.

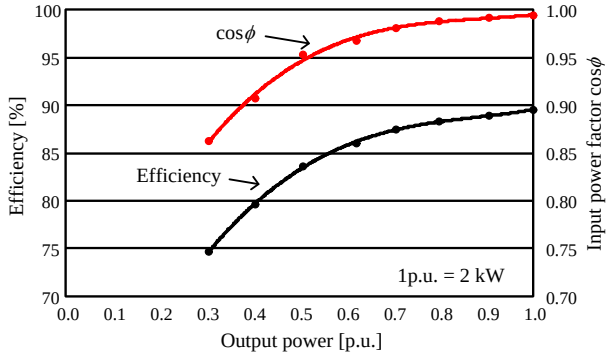

Fig. 7. Characteristic of efficiency and power factor.

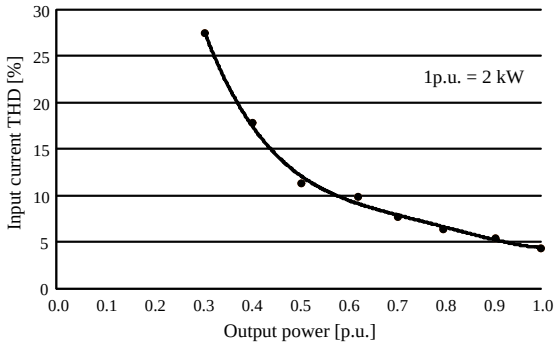

Fig. 8. Characteristic of input current THD

0.8p.u. to 1.0p.u. Note that the rated power is 1.0p.u. = 2 kW. The primary capacitor voltage is balanced in both the steady state and transient state. Moreover, the maximum DC-link capacitor voltage on the primary side is almost matched. Thus, it is confirmed that the DC-link capacitor voltage on the primary side is automatically balanced among all cells without the balancing control despite the output power changes.

Figure 6 shows the input voltage of all cells. From Fig. 6(a), the input voltage is equally divided into each cell because the output voltage of all cells forms a balanced multilevel waveform. In Fig. 6(b), it is also confirmed that the equivalent switching frequency f_{eq} is 30 kHz. The equivalent switching frequency is determined by the switching frequency in PFC and the number of the cells.

Figure 7 shows the efficiency and input power factor characteristic. The maximum efficiency is 89.5% at the rated power. The input power factor is over 0.95 with the output power from 0.5p.u. to 1.0p.u.

Figure 8 shows the input current THD characteristic with changing the output power of the SST. Input current THD is relatively high in the low-power region. This is because the rate of the low-order harmonics component appears remarkably with respect to the fundamental component because the input current is low when the output power is low.

4.2 Bidirectional operation The miniature model is tested to confirm the fundamental operation with the input voltage of 200 V because of the limitation of the experimental facilities in this experiment. The regenerative power supply is used for the output side for the test of the regeneration.

Figure 9 shows the bidirectional operation of the proposed SST when the operation mode is switched from the power running to regeneration at the center of the horizontal axis. It is confirmed that the unity power factor on the input side is achieved in both the power running and regeneration operation. The input current THD is 4.2% during the operation. From the waveforms of the sum of the output voltage of each cell, it is confirmed that the waveform is four-level staircase voltage. Note that an equivalent switching frequency f_{eq} is 30 kHz. Thereby, the stable operation of the miniature model without any large distortion is achieved even when the operation abruptly changes.

Figure 10 shows the DC-link capacitor voltage on the primary side of three cells in the bidirectional operation. Despite the change of the power flow, the DC-link capacitor voltage on the primary side is balanced among all cells without the balance control even when the operation rapidly changes.

5. Loss Analysis and Estimation for Full Model

The loss of SST is separated based on the components shown as follows:

(i) Diode bridge rectifier on the primary side
(ii) Switches of PFC converter
(iii) Switches of the resonant DC-DC converter
(iv) Rectifier on the secondary side

Table 4 shows the switching devices for each part. In the proposed SST, the rated voltage of 3.3 kV is used in the primary side rectifier.

First, the primary DC-link capacitors are selected for the full model. The current which flows into the electrolytic capacitor includes not only the power ripple component but also the switching frequency component from the inverter. Thus, it is very impossible to analytically derive the ripple current on the DC-link capacitor. Thus, the capacitor ripple current is evaluated by the simulation[22]. The capacitor ripple current is the function of the output power factor angle φ and the modulation index λ, which is a nonlinear value. Then, the effective value of the capacitor ripple current is given by (9).

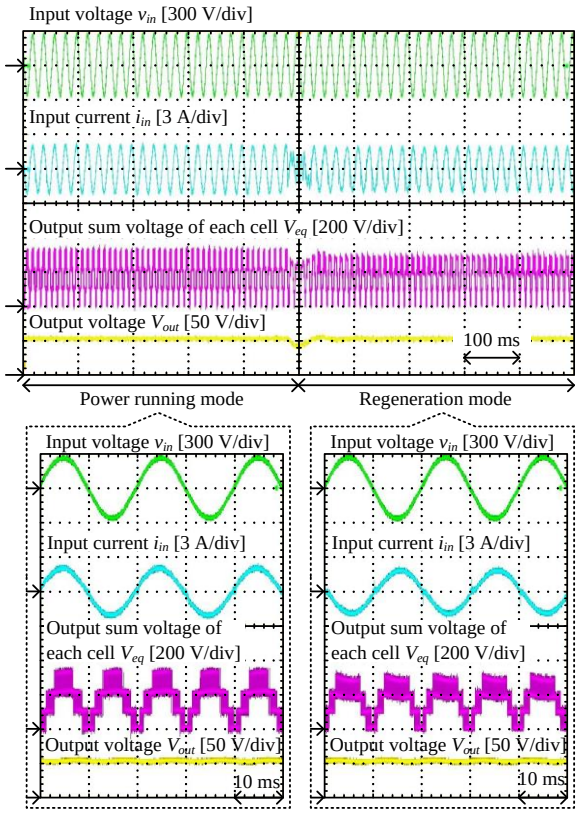

Fig. 9. Bidirectional operation of proposed circuit.

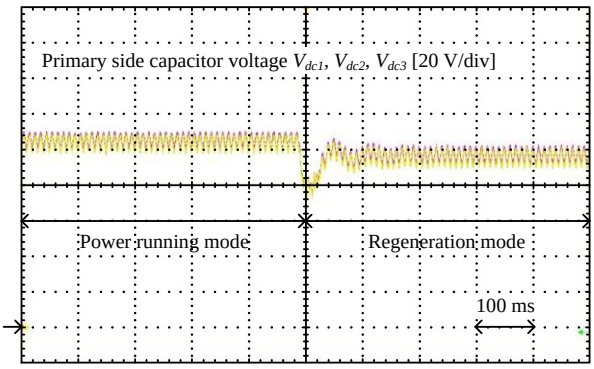

Fig. 10. Primary side capacitor voltage of each cell at

$$I_{rms\_cap} = K_{cap}(\varphi, \lambda) I_{out} \quad \text{.....(9)}$$

where I_{out} is the average value of the output current, and K_{cap} is the coefficient which is obtained by the simulation.

Figure 11 shows the simulation result of $K_{cap.}$ The modulation index, which expresses the ratio of the voltage per cell and the dc-link voltage, is 0.94 in the miniature model SST. Therefore, from Fig. 11, K_{cap} (1.0, 0.94) is 0.83.

5.1 Primary side diode bridge The loss of switches, which is calculated by the on-voltage of the switch and the current through the switch, is given by (10).

$$P_{con} = \frac{1}{2\pi}\int_0^{\pi} v_{on}\, i_{sw}\, d\omega t \quad \text{.....(10)}$$

where v_{on} is the on-voltage of the switch, i_{sw} is the current through the switch. In this case, v_{on} and i_{sw} are given by (11), (12).

$$v_{on} = r_{on}\sqrt{2}\frac{P}{V_{in}}\sin(\omega t) + v_0 \quad \text{.....(11)}$$

$$i_{sw} = \sqrt{2}\frac{P}{V_{in}}\sin(\omega t) \quad \text{.....(12)}$$

where r_{on} is the on-resistance of the switch, P is the rated power of SST. In (11), v_0 is defined as zero because the MOSFETs are used in the prototype. Moreover, the phase difference between the input voltage and the input current is not considered because the power factor is always unity. The loss of the switches in the primary side rectifier is given by (13).

$$P_{con\_pri\_rec} = \frac{1}{2} r_{on}\left(\frac{P}{V_{in}}\right)^2 \quad \text{.....(13)}$$

5.2 PFC converter The conduction loss of the

Table 4. Switching devices for bidirectional operation.

Circuit topology	Part	Type	Maximum ration
Single-phase rectifier	$S_1 \sim S_4$	-	3300 V
PFC converter	$S_{pfc11} \sim S_{pfc12}$	SCT2080KE	1200 V 40 A
Resonant DC-DC converter	$S_{llc11} \sim S_{llc12}$		
Secondary side rectifier	$S_5 \sim S_8$		

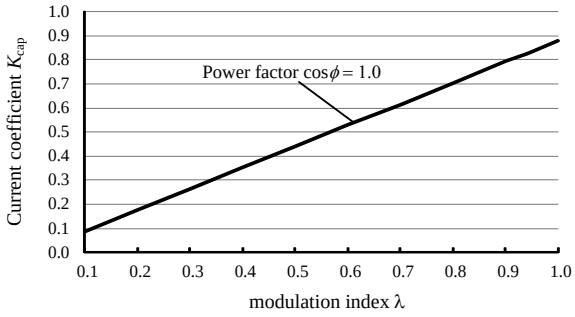

Fig. 11. Current coefficient of output capacitor.

switches in PFC is given by

$$P_{con\_PFC} = \frac{1}{2} r_{on} I_L^2 \quad \text{.....(14),}$$

where I_L is the RMS value of the boost inductor current on the PFC stage.

On the other hand, the switching loss, which is assumed that it is directly proportional to the voltage and the current of the switch, is calculated using

$$P_{sw\_PFC} = \frac{1}{\pi} \frac{e_{on} + e_{off}}{E_{nom} I_{nom}} \frac{V_{dc}}{V_{cell}} \frac{P}{m} f_{sw} \quad \text{.....(15),}$$

where P is the rated power, m is the number of cells, V_{dc} is the voltage of the primary side capacitor, f_{sw} is the carrier frequency, e_{on} and e_{off} are the turn-on and the turn-off energy per switching, which are provided by the datasheet, E_{nom} and I_{nom} are the voltage and the current under the measurement condition of the switching loss from the datasheet, and V_{cell} is the input voltage of each cell.

5.3 Resonant DC-DC converter Only the conduction loss is considered in this power loss calculation of switches because the ZCS is assumed overall operation regions.

Therefore, the conduction loss is given by

$$P_{con\_LLC} = \frac{1}{2} R_{on} \left(\frac{N_2}{N_1} \right)^2 \frac{I_{out}^2 - I_{rms\_cap}^2}{m^2} \quad \text{.....(16).}$$

At the secondary side, the conduction loss is given by (17).

$$P_{con\_sec\_rec} = \frac{1}{2} R_{on} \frac{I_{out}^2 - I_{rms\_cap}^2}{m^2} \quad \text{.....(17).}$$

5.4 High-frequency transformer In this subsection, the high-frequency transformer is evaluated. As one of the power loss on the transformer, an iron loss is calculated from the magnetic flux density on the core. The AC magnetic flux density B_{ac} is given by

$$B_{ac} = \frac{V_{out}}{4 f_o A_e N} \quad \text{.....(18),}$$

where N is the turns ratio of the transformer, A_e is the effective cross-section of the core. The core loss, which is provided in the datasheet of the core is used for this analysis considering the magnetic flux density of the core (19). Therefore, the iron loss is given by

$$P_{iron\_loss} = P_{cv} V_e \quad \text{.....(19),}$$

where V_e is the effective volume of the core.

The high-frequency transformer of full model SST is designed using Gecko MAGNETICS which uses improved-improved Generalized Steinmetz Equation (i^2GSE) for the calculation of the iron loss of the high-frequency transformer [23]. The optimum core shape, core material, and winding shape can be selected using Gecko MAGNETICS. From the analysis of Gecko MAGNETICS, EPCOS N95 is the optimum core to minimized the transformer.

5.5 Loss distribution Figure 12 shows the shakedown of the power loss, which is measured by the experiments and calculation. The power loss in the powering and regeneration operation are presented. It should be noted that the power loss is normalized with the experimental results as 100%. The calculation shows a good agreement with the experimental results. The error of

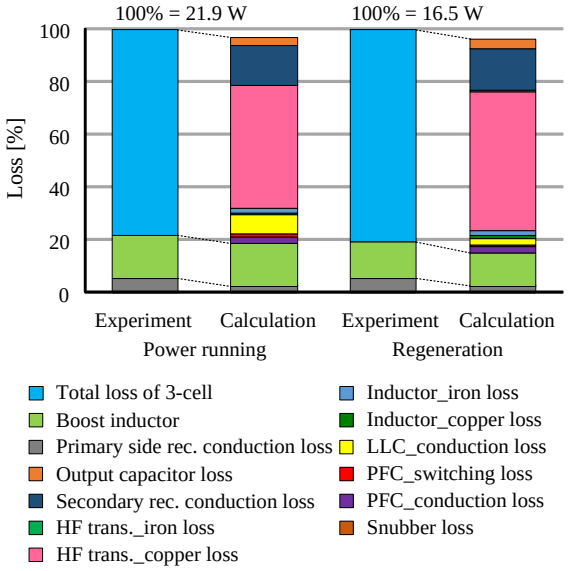

Fig. 12. Loss distribution result by experiment and calculation at bidirectional operation. (Explanatory note corresponds to each color of graph.)

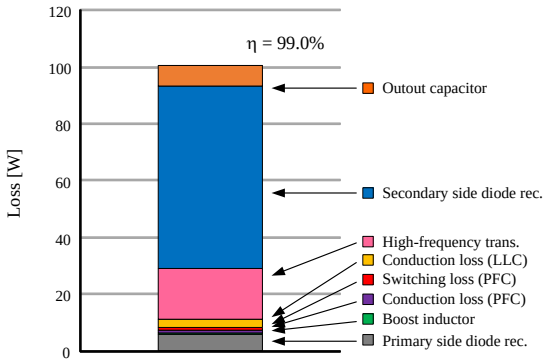

Fig. 13. Loss distribution of 6.6 kV/ 10 kW full model SST by calculation.

the power loss between the calculation and the experiment is less than 5%.

Figure 13 shows the calculation result on the power loss of the full model SST. The power loss is calculated with assuming an input voltage of 6.6 kV and an input power of 10 kVA. Then, the number of cells is 15 because the use of 1.2-kV switching devices is assumed. From this calculation, the efficiency of the 10-kVA full mode will reach to a 99% conversion efficiency at the rated power. The dominant power loss is the conduction loss of the diode on the secondary side. The proposed SST will achieve higher efficiency by applying the synchronous rectification on the secondary side.

6. Conclusion

This paper has proposed a new topology of SST. In the proposed SST, the DC-link capacitor on the primary side is automatically balanced without any voltage balancing control. The power running operation of SST is confirmed with the input voltage of 1320 V which is 1/5 of the full model from the experimental results. Moreover, the bidirectional operation and switch between the powering and regenerating operation is tested. As a result, the sinusoidal waveform of the input current is obtained at the primary

side. Furthermore, the average DC-link capacitor voltage on the primary side is stable and balanced among all cells despite the change of power flow.

Finally, the power loss of each part of the system is calculated and compared with the experimental result. As a result, the error of the loss between the experimental result and the calculation is less than 5%. Using the calculation, the efficiency of the full model of the proposed SST is estimated that it will reach a 99% conversion efficiency.

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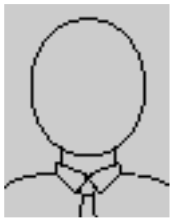

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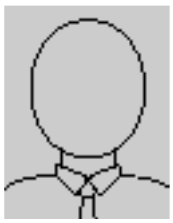

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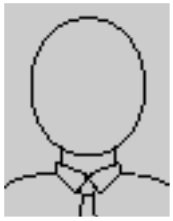

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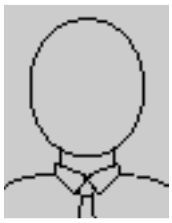

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