Isolated DC to Single-phase AC Converter with Active Power Decoupling Capability for Battery Storage System

Nagisa Takaoka, Hiroki Watanabe, Jun-ichi Itoh
Dept. of Electrical, Electronics and Information Engineering
Niigata, Japan
ntakaoka@stn.nagaokaut.ac.jp, hwatanabe@vos.nagaokaut.ac.jp, itoh@vos.nagaokaut.ac.jp

Abstract— **This paper proposes a new active power decoupling topology circuit, which does not require any additional passive components and switching devices for battery storage systems. This converter operates as the bidirectional isolated DC to single-phase AC converter with the power decoupling capability using the coupled inductor. The pulse density modulation (PDM), which achieves zero voltage switching (ZVS) is applied for the secondary side converter using a matrix converter (MC) in order to reduce the switching losses. This paper mentioned that the proposed circuit reduces the double-line frequency power ripple on the input current to 10.3% by the experiment. In addition, the output voltage THD is lower than 3.0% overwide load range.**

Keywords—Battery Storage System; Electronic Vehicle; Single-phase converter; Power ripple compansetion

I. INTRODUCTION

Recently, the research of Electric Vehicle (EV) and Plug-in Hybrid Electric Vehicle (PHV) have been rapidly expanded [1]. An isolated DC to single-phase AC converter is the main component of a battery storage system for these vehicles in order to achieve a safe connection.

The converter topologies for the battery storage system have been studying for following requirements; (i) long life-time, (ii) high efficiency, (iii) small volume, (iv) high reliability, (v) galvanic isolation. The EV/PHV with the battery storage system become increasingly popular to meet the all following conditions. However, in the conventional topologies, the large electrolytic capacitor is required to absorb a double-line frequency power ripple, which is caused by instantaneous power mismatch between DC and the AC grid side. As a result, the using large electrolytic capacitor is brought to limit the life-time and results in low reliability of the conventional converter.

As one of the solution, active power decoupling topologies, leading to the elimination of the bulky electrolytic capacitors in the DC-link have been studying [2-6]. These active power decoupling topologies charge and discharge the buffer capacitor by the additional switching devices and passive components in order to compensate the double-line frequency power ripple. It is possible to ensure the reliability and the life-time compared to the conventional method by the buffer capacitors, which enable to use of film or ceramic capacitor instead of the bulky electrolytic capacitor. The problems of almost conventional active power decoupling topologies and control methods are the switching losses due to hard switching of an entire converter and additional switching devices for active power decoupling capability. However, these additional components prevent the high efficiency, high reliability and the downsizing of the converter system.

This paper proposes a new active power decoupling topology for an isolated DC to single-phase AC converter based on matrix converter (MC). The originality of this proposed active power decoupling topology is not require any additional components, owing to the employment of the coupled inductor. The coupled inductor assumes the boost operation and the power decoupling operation without additional magnetic component in the proposed converter. Furthermore, in order to reduce the converter losses, MC is applying to the secondary side. MC is achieved to reduce in the number of the conversion from two stages to one stage compared to a typical converter configuration as a rectifier and a full bridge converter, In addition, a pulse density modulation (PDM) is applied to MC in order to achieve the zero voltage switching (ZVS). This paper presents the validity of the proposed method by experiment.

II. CIRCUIT CONFIGURATION

A. Conventional circuit

Figure 1 shows an isolated DC to single-phase AC converter with the conventional power decoupling circuit. This power decoupling circuit is applied at the primary side in order to eliminate the bulky electrolytic capacitor. In the conventional power decoupling method, the buffer capacitor voltage is actively fluctuated in order to absorb the power ripple. Therefore, the DC-link capacitance is achieved to minimize the comparison with that in C_{dc} as shown in Fig. 1 because the buffer energy is ensured by the capacitor voltage. However, the conventional power decoupling method requires the additional switching devices and magnetic components. In addition, the conventional converter configuration has a number of the four stages power conversion including the active power decoupling method. Consequently, this method increases the volume of the cooling system and the converter loss.

B. Proposed circuit

Figure 2 presents the proposed isolated DC/AC converter, which is composed by a matrix converter and a full-bridge inverter with the coupled inductor. The third-winding N_3 of the coupled inductor is galvanic isolation between the primary side. In particular, the buffer capacitor C_{buf} absorbs the double-line frequency power ripple by charging and discharging it, whereas full-bridge inverter controls the buffer capacitor voltage. In the secondary-side, MC is employed to eliminate the DC-link smoothing capacitors. Furthermore, the MC is achieved to reduce the number of the power conversion from two stages to one stage in the secondary side compared to a general configuration of a rectifier and a full-bridge inverter. Thus, MC as a secondary converter contribute the improvement of the power density of the converter system and the converter efficiency.

Figure 3 shows the operation modes of full-bridge inverter with the coupled inductor. The proposed inverter has four operation modes which generate a phase shift between the switching of each arm. Fig. 3 (a) and (b) is power transfer operation mode to secondary side. On the other hand, Fig. 3 (c) and (d) is power decoupling operation mode in order to charge and discharge the buffer capacitor. A leakage inductor of the coupled inductor is utilized as the boost inductor L_{boost}. Note that the main power from the battery to the AC grid is controlled by the differential mode, whereas the power ripple component is absorbed by controlling the common mode. The inductance of the boost inductor in worst case, which ripple ratio is maximum is calculated by

$$L_{boost} = \frac{d_{com\_mux} V_{dc}}{2 \Delta i_{dc} f_{sw}} \tag{1}$$

$$\Delta i_{ripple} = \frac{i_{ripple\_pp} / 2}{i_{dc\_\max}} \tag{2}$$

where Δi_{dc} is the allowable current ripple ratio, i_{ripple_pp} is the peak to peak value of the input current i_{dc}, V_{dc} is a DC input voltage and f_{sw} is the switching frequency. Note that the d_{com_max} is the maximum reference of the common mode in a one period, which is explained in next section.

C. Principle of power decoupling

If both the grid current and voltage are sinusoidal, the buffer capacitor voltage v_{Cbuf}, which necessary to compensate the power ripple is calculated based on the energy of the buffer capacitor. First, the energy of the buffer capacitor W_{Cbuf} is expressed by

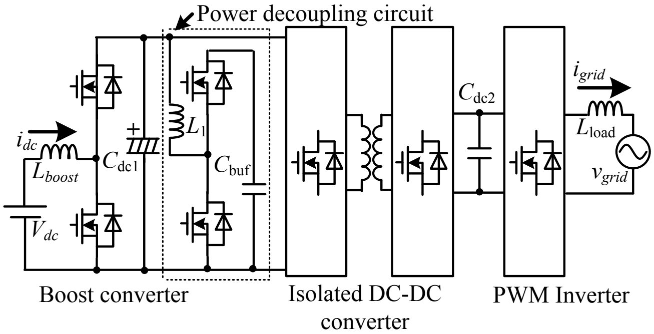


Fig.1 Conventional isolated DC to single-phase AC converter with active buffer circuit. The conventional converter uses a bulky electrolytic capacitor C_{dc} to absorb the power ripple caused by a single-phase load.

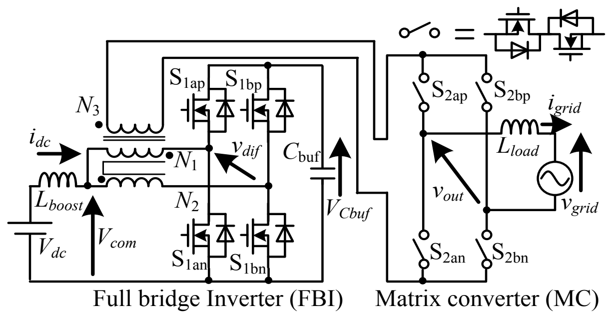


Fig. 2. Configuration of proposed isolated converter. The full-bridge inverter with the coupled inductor and the buffer capacitor is controlled to convert the DC input power to the AC power and absorb the power ripple without additional switching devices and inductors.

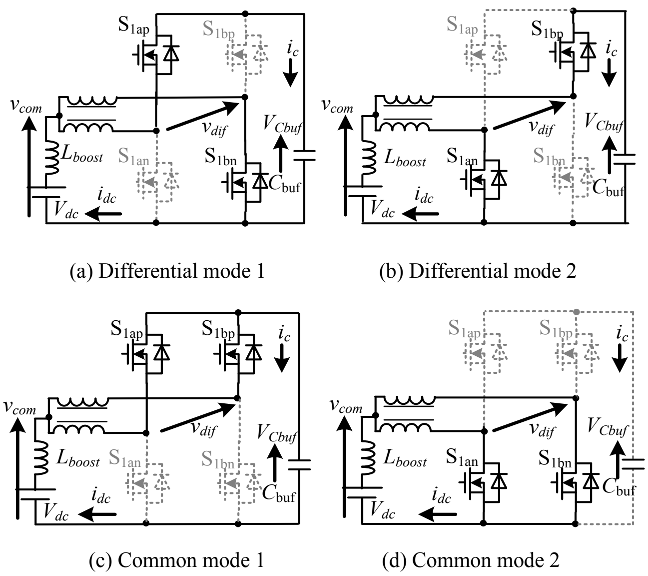


Fig. 3. Operation modes of primary-side converter with coupled inductor. The primary side of the proposed system is operated in two modes; the differential mode as the power transmission and the common mode as a power ripple compensation.

$$\begin{aligned} W_{Cbuf} &= \int_{t_0}^{t} v_{Cbuf} i_{buf} d\tau = \int_{t_0}^{t} v_{Cbuf} \left(C_{buf} \frac{dv_{Cbuf}}{d\tau} \right) d\tau \\ &= \int_{t_0}^{t} P_{ave} \cos(2\omega_0 \tau) d\tau \end{aligned} \tag{3}$$

where i_{buf} is the current of C_{buf}, P_{ave} is the average power of the output-side and ω_0 is the grid-side angular frequency. From (3), the voltage of the buffer capacitor v_{Cbuf} for the compensation of the power ripple is presented by

$$\begin{aligned} v_{Cbuf} &= \sqrt{{V_{C0}}^2 + \frac{P_{ave}}{\omega_o C_{buf}}\left\{\sin(2\omega_0 t) - \sin(2\omega_0 t_0)\right\}} \\ &= \sqrt{{V_{C0}}^2 + \frac{P_{ave}}{\omega_0 C_{buf}}\sin(2\omega_o t)} \end{aligned} \tag{4}$$

where V_{C0} is the buffer capacitor voltage at a start time t_0.

III. Control Strategy

In the control of the differential mode operation as a power transfer, the three-winding voltages of the coupled inductor are controlled into a three-level wave form by operation modes as shown in Fig. 3 (a) and (b). On the other hand, the common mode operation is controlled to absorb the power ripple. In particular, the power ripple component occurs in the buffer capacitor voltage because the input current is regulated into a constant value in the proposed power decoupling method.

Then, the common mode operation of the proposed method is employed for the remaining period after the differential mode operation. Therefore, the duty ratio of the common mode operation is calculated by the following:

$$d_{com\_c} = \left(1 - d_{dif}\right)\frac{{v_{com}}^*}{v_{Cbuf}} \tag{5}$$

where d_{dif} is the duty ratio of the differential mode, whereas d_{com_c} is the duty ratio of the common mode as shown in Fig. 5(c) and v_{com}^* is a command of the common voltage. This common mode voltage command v_{com}^* is output by a PI control of the DC input current as explained in the next section. In addition, d_{dif} is decided to the maximum value of the relationship between the input and output voltage.

Figure 4 shows a relationship among each command, the triangle carrier and the switching pattern of the primary converter in the proposed system. The differential mode voltage of the each duty ratios as shown in Fig. 3(a) and (b) in a carrier period is equal in order to suppress a DC biased magnetization of the coupled inductor, especially. The comprising signals A and B is generated by comprised duties which the sum of "d_{com_c} and d_{dif}" and only d_{com_c} and a triangle carrier as shown in Fig. 4. Thus, the desired operation in each duties of the primary converter is actualized as described previously. The primary converter of the proposed system achieves the power decoupling operation and the transfer power to the secondary side at the same time without the additional passive components and the switching devices.

Figure 5 shows the control block diagram of the proposed system with the power decoupling capability. The DC input

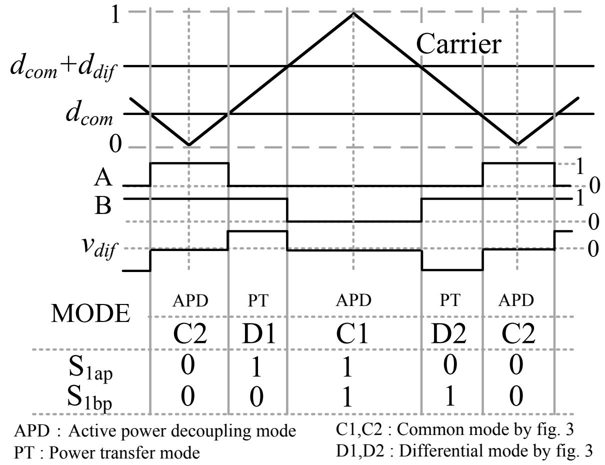


Fig. 4. Relationship among operation modes, signal and carrier.

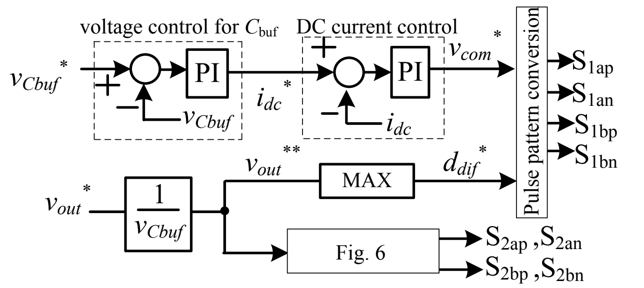


Fig. 5. Control block diagram

current control, which absorbs the power ripple component, is control by using PI controller. The actively fluctuated value of the buffer capacitor voltage command is calculated by (4). Furthermore, the pulse pattern conversion outputs the each gate signal using carrier and signals A and B as shown in Fig. 4.

IV. Modulation method of Matrix Converter

Figure 6 shows the signal generation block of the proposed PDM based on the delta-sigma conversion [6]. In this PDM method, the output grid voltage waveform is generated by using the input voltage pulses of MC as the minimum unit. PDM allows MC to switch at the zero voltage period of the third-winding of the coupled inductor. Moreover, the distortion of the grid voltage, which influences on the output voltage quality of MC is achieved to become low. A delta-sigma conversion generates the inverse voltage pulses in order to cancel the quantization error. Consequently, MC with this PDM method achieves the decrease of the switching loss and the low output voltage THD.

V. Experimental Result

Table 1 shows the experimental conditions and Figure 7 demonstrates the experimental waveforms of the proposed converter with/without the power decoupling method at R-L

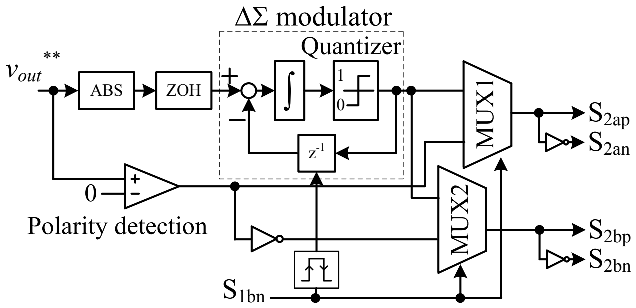


Fig. 6 Gate signal generation block of PDM based on delta-sigma conversion.

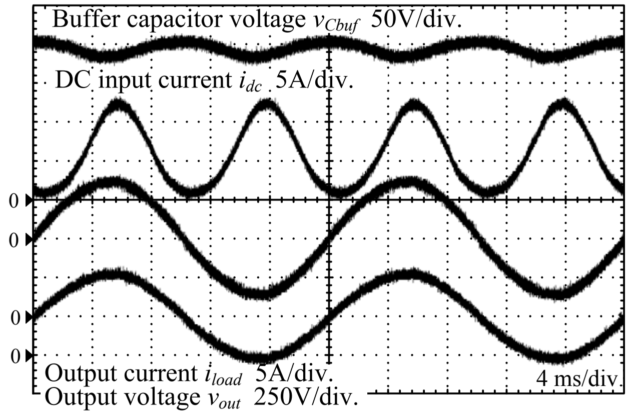
Table 1 Experimental condition

DC input voltage	200 V_{dc}	Load voltage	200 V_{rms}
Rated power	1 kW	Load current	5 A_{rms}
Load frequency	50 Hz	Filter inductor L_{out}	2.0 mH
Boost inductor L_{boost}	1 mH	Turn ratio of coupled inductor N_1:N_2:N_3	1:1:2
Buffer Capacitor C_{buf}	200 μF		
Carrier frequency of primary converter	100 kHz	Carrier frequency of secondary converter	10 kHz

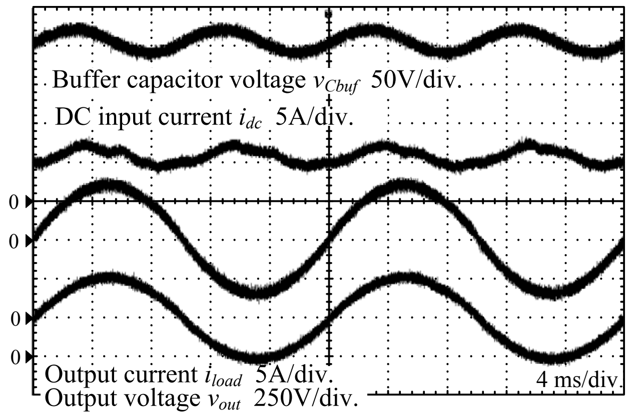
load as the single-phase AC load. As shown in Fig. 7 (a), the input current i_{dc} has a double-line frequency power ripple component without the power decoupling method. The buffer capacitor voltage fluctuation is small because the power ripple component is not compensated by the buffer capacitor in this operation mode, i.e. the passive power decoupling capability. In contrast, the proposed method actively fluctuates the v_{Cbuf} from Fig. 7 (b). Consequently, the 2nd-order harmonics as a 100 Hz in the input current is suppressed greatly.

Figure 8 shows the double-line frequency power ripple component on the input current of the proposed converter. Note that the fundamental harmonic is based on the output frequency of 50 Hz. It is verified from the analysis result in Fig. 8, the double-line frequency power ripple component on the input current is reduced by 79.2% as compared to that without power decoupling method. However, a small ripple component still appears in the input current. This is because the compensation reference shown the (4) has a small error as compared to the actual power ripple.

Figure 9 shows the harmonic analysis result of the input current and the total harmonics distortion (THD) of the output voltage in the proposed converter. The double-line frequency power ripple component as a 100 Hz on the input current is normalized by the each DC component of the input current. From the analysis result, the proposed power decoupling method reduces the double-line frequency power ripple component to 10.3% in maximum. This is attributed that the power pulsation are compensated by the active power decoupling operation. In addition, the output voltage ripple is low because the pulse is output continuously with applying the proposed PDM method in MC of a secondary converter. This PDM method, which based on the delta-



(a) Without power decoupling method.



(b) With power decoupling method.

Fig. 7. Experimental waveforms in steady state when output power is about 1 kW. The fluctuated capacitor voltage is absorb the double-line frequency power ripple on the input current.

sigma conversion is improved by the quantizer. Then, the quantizer outputs the output pulses to cancel the quantization error from the reference value of v_{out}. As a result, the output voltage THD is lower than 3.0% overwide load range.

Figure 10 shows the extended voltage in MC with PDM. The experimental results mentioned the ZVS operation of turn-on at MC with the proposed PDM method. In the all devices are turn-off period, the drain-source voltages are pulsated when the current of devices is near 0 A.

VI. Conclusion

This paper has proposed a new DC to single-phase AC isolated converter with the power decoupling capability by using the coupled inductor. This proposed converter configuration is chosen because of the following advantages;

(i) Boost operation is achieved without additional L,

(ii) Elimination of bulky electric capacitors in the circuit,

(iii) The buffer capacitor using a low capacitance,

(iv) No additional component for the power decoupling,

(v) Low output voltage THD.

A prototype was constructed to validate the power decoupling method and fundamental operation in experiment. As a result, the power ripple component of a secondary-order harmonics was reduced by 79.2% in comparison to the case without the proposed power decoupling method. The result with applying the PDM based on the delta-sigma conversion is verified to achieve ZVS operation in MC and low output voltage THD, which is lower than 3.0% within the entire output power range.

In future work, we will analyze the loss distribution of the proposed converter.

REFERENCES

[1] K.Shiozaki and others, "Design and Verification of High Frequency SiC On-board Vehicle Battery Charger for PHV/EV", SAE of Japan, pp. 25, (2014)

[2] A. Tokumasu and others, "AC/DC Converter Based on Instantaneous Power Balance Control for Reducing DC-Link Capacitance", IEEJ Journal of Industry Applications, Vol. 4, No. 6 pp.745-751 (2015)

[3] S. Yamaguchi, T. Shimizu: "Single-phase Power Conditioner with a Buck-boost-type Power Decoupling Circuit", IEEJ Journal of Industry Applications, Vol. 5, No. 3, pp.191-198 (2016)

[4] T. Shimizu and others, "Flyback-Type Single-Phase Utility Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System", IEEE Trans. On Power Electronics, Vol. 21, No. 5, pp. 1264-1272 (2006)

[5] Y. Tang and others, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit" IEEE Trans. Power Electron., vol. 30, no. 4, pp.1855–1865,(2015)

[6] C.T. Lee and others, "Efficiency Improvement of a DC/AC Converter with the Power Decoupling Capability", 2012 Twenty-Fourth Annu.IEEE Appl. Power Electron. Conf Expo., pp1462-1468 (2012)

[7] S. Kimura, K. Nanamori, T. Kawakami, J. Imaoka, and M. Yamamoto"Allowable Power Analysis and Comparison of High Power Density DC-DC Converters with Integrated Magnetic Components,"IEEJ J. Industry Applications, vol. 6, no. 6, pp. 463-472, 2017.

[8] H.Radwan, M.A. Sayed, T.Takeshita, A.A. Elbaset, G. Shabib," Boost Inverter Topology with High-Frequency Link Transformer for PV Grid-Tied Applications" IEEJ J. Industry Applications,vol. 8, No. 5, pp. 849-856

[9] P. W. Wheeler and others, "Matrix Converters: A Technology Review", IEEE Trans. Ind. Electron., Vol. 49, No. 2, pp. 274-288 (2002)

[10] J. Haruna, J. Itoh: "Control Strategy for a Matrix Converter with a Generator and a Motor", Proc. 26th IEEE APEC, pp. 1782-1789 (2011)

[11] K. Yamamoto, S. Ehira, and M. Ikeda, "Synchronous Frame Control for Voltage Sag/Swell Compensator Utilizing Single-Phase Matrix Converter,"IEEJ J. Industry Applications, vol. 6, no. 6, pp. 353-361, 2017.

[12] Y.Nakata and J.Itoh "A fundamental verification of a single-phase to three-phase matrix converter with a PDM control based on space vector modulation", 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), pp.138-145, (2014)

[13] N.Takaoka, H.Takahashi, J.Itoh: "Isolated Single-Phase Matrix Converter Using Center-Tapped Transformer for Power Decoupling Capability", IEEE Transactions on Industry Applications, Vol. 54, No. 2, pp. 1523-1531 (2018)

[14] E.C. Nho, J.H.Jung, H.S.Kim: "Switching Loss Minimization of 3-phase Interleaved Bidirectional DC-DC Converter" The 2014 IPEC, pp2763-2764 (2014)

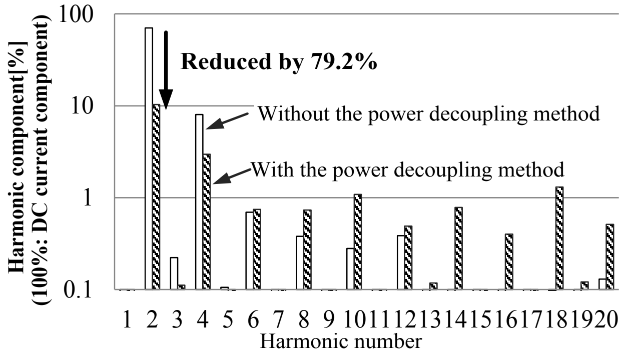


Fig. 8 Harmonic analysis result when output power is 940W. The 2nd order harmonic of 100 Hz component is reduced by 79.2% by proposed converter and the power decoupling method.

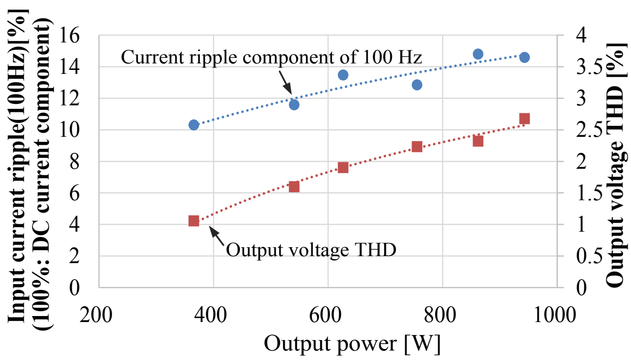


Fig. 9 Harmonic analysis result of input current and total harmonics distortion (THD) of output voltage in proposed converter within output power from 300 W to 1 kW.

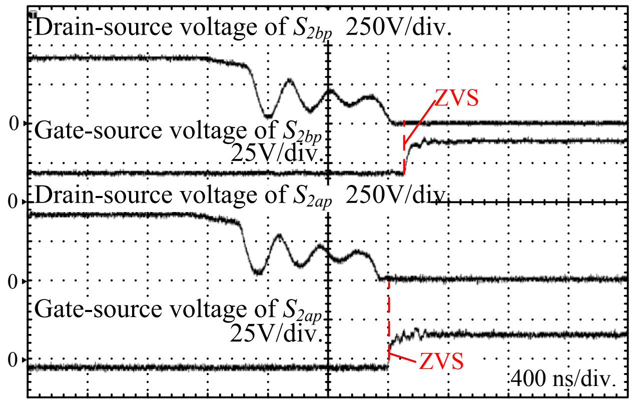


Fig. 10 Gate-source voltages of MC in experiment. The pulse is output to improve the distortion and ZVS operation of the turn-on is achieved by applying PDM based on a delta-sigma conversion in MC.