# Current Stress Reduction for DC-link Capacitors of Three-phase VSI with Carrier-based Continuous PWM

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***Abstract* -- This paper proposes a novel continuous PWM (CPWM) method to reduce DC-link current harmonics in voltage source inverters (VSIs) over wide range of load power factor. This modulation method contributes to a current stress reduction of DC-link smoothing capacitor and a suppression of its temperature rise. Furthermore, a high cost digital hardware such as a field-programmable gate array (FPGA) is not necessary because this modulation is implemented with only one carrier. The DC-link current harmonics are reduced by shifting voltage references in every half control period to reduce a fluctuation of the DC-link current around its average value. Experimental results confirm that the application of the proposed CPWM reduces the DC-link current harmonics by 24.2% at most and lowers an equilibrium capacitor temperature by 6.0℃ compared to the conventional CPWM.**

***Index Terms—Two-level voltage source inverter, DC-link capacitor, Inverter DC-link current harmonics, Continuous PWM***

## I. INTRODUCTION

Three-phase AC motors are widely used in both industrial and household applications [1]–[8]. A lifetime extension of the AC motor drive systems has been actively researched for a decade [9]–[14]. The employment of film capacitors in the DC-link part of the three-phase voltage source inverter (VSI) instead of electrolytic capacitors, of which lifetime expectancy is short, is one of the solution for the lifetime extension. On the other hand, the maximum allowable temperature of poly-propylene, a dielectric material of the film capacitor, is 105℃ [15]; thus, the suppression of its temperature rise is important. It is possible to suppress the temperature rise of the DC-link capacitors by reducing the DC-link current harmonics of VSIs.

So far, several modulation methods of VSI which reduce the DC-link current harmonics have been proposed [10]–[14]. With a space vector PWM (SVPWM) presented in [13], voltage space vectors are selected in order that the zero vector period is shortened to minimize the DC-link current harmonics. Furthermore, this SVPWM adapts to the variation of the load power factor by changing the applied voltage space vectors according to polarities of inverter output phase currents. However, the employment of the SVPWM leads to a constraint of digital hardware, i.e. the requirement of high cost hardware such as field-programmable gate array (FPGA).

As another approach to reduce the DC-link current harmonics, a new single-carrier-comparison discontinuous PWM (DPWM) has been presented in [14]. In this DPWM, voltage references of the classic DPWM are shifted at both the positive-peak and negative-peak of a triangular carrier to reduce the DC-link current harmonics, and only one carrier is used for comparison. Thus, this DPWM can be implemented with the general-purpose micro-computer. However, the DPWM strategy faces challenging disadvantage compared to continuous PWM (CPWM); in particular, the number of switching transition per control period in the DPWM is less than that in the CPWM. This leads to an increase of the AC motor noises due to a high inverter output voltage harmonics. Therefore, the applications of the DPWM are limited.

This paper proposes a novel carrier-comparison CPWM which uses only one carrier to reduce the DC-link current harmonics. This modulation method contributes the current stress reduction of the smoothing capacitor in the motor drive system and can be implemented with the general-purpose micro-computer. In particular, three phase continuous voltage references are shifted in every half control period to reduce the fluctuation of the DC-link current around its average value. By optimizing the shifting manner of the voltage references, it is possible to reduce the DC-link current harmonics over entire region of the load power factor. One more contribution of this CPWM is to overcome the problem of the DPWM, such as large inverter output voltage harmonics. Furthermore, this paper verifies that the current stress reduction with the proposed CPWM contributes the suppression of the DC-link capacitor temperature rise, which has not been demonstrated by our past work in [16].

This paper is organized as follows: First, the reduction method of the DC-link current harmonics by using the shifted voltage references is presented. Second, the effects on the DC-link current, the output phase current harmonics and the inverter efficiency are compared between the conventional and proposed DPWM by analysis and experiment. Finally, the capacitor temperature rise test is presented to confirm the effectiveness of the proposed CPWM.

## II. INVERTER DC-LINK CURRENT HARMONICS WITH CONVENTIONAL CONTINUOUS PWM

Fig. 1 shows the voltage references of CPWM and output phase currents at a modulation index $m$ of 0.7 and a load power factor cos $\varphi$ of 0.707. Three phase voltage references $v^*_x$ ($x = u$, $v$, and $w$) of the conventional CPWM [17] are sinusoidal

waves as

$$\begin{cases} v_u^* = m \cdot \cos(2\pi ft) \\ v_v^* = m \cdot \cos(2\pi ft - 2\pi/3) \\ v_w^* = m \cdot \cos(2\pi ft + 2\pi/3) \end{cases} \quad (1)$$

where $f$ is the fundamental frequency.

Fig. 2 shows zoomed-in waveforms of $v^*_x$, switching functions $s_x$ and the DC-link current $i_{DC.in}$ at $m$ = 0.7, $2\pi ft$ = 25 degrees, and cos $\varphi$ = 0.707. The DC-link current is the superposition summation of the switched current pulses from each leg and calculated as

$$i_{DC.in} = \sum_{x=u,v,w} (s_x \times i_x). \quad (2)$$

The shaded area of the DC-link current waveform in Fig. 2 indicates the instantaneous root-mean-square (rms) value of the current flowing into the smoothing capacitor, which is calculated as

$$i_{C.rms}(T_s) = \sqrt{i^2_{DC.in.rms}(T_s) - i^2_{DC.in\_ave}}$$
$$\begin{cases} i_{DC.in.rms}(T_s) = \sqrt{\dfrac{1}{T_s}\int_0^{T_s} i^2_{DC.in}\,dt} \\ i_{DC.in\_ave} = \dfrac{3}{4} m \cdot I_m \cos\varphi \end{cases} \quad (3)$$

where $T_s$ is the control period, $I_m$ is the maximum value of the output phase current, and $\varphi$ is the load power factor lagging angle. Note that a smaller fluctuation of the DC-link current around its average value results in a smaller rms value of the smoothing capacitor current [18]. With the conventional CPWM, the center of the gate pulses is same as the center of the control period, which results in the longest overlap period of the gate pulses. This leads to the large fluctuation of the DC-link current around its average value, i.e. the high DC-link current harmonics.

## III. Proposed PWM Method to Reduce DC-link Current Harmonics of VSI

It is obvious from (2) and (3) that the DC-link current harmonics are highly influenced by the switching patterns and output phase currents, i.e. the load power factor. Therefore, the proposed CPWM reduces the DC-link current harmonics by shifting output voltage references in every half control period and adjusting the gate pulse timings in the control period. Furthermore, the proposed shifting rule of the voltage references adapts to the load current conditions. In other words, the proposed modulation method reduces the DC-link current harmonics with adaptation for the variation of the load power factor [16].

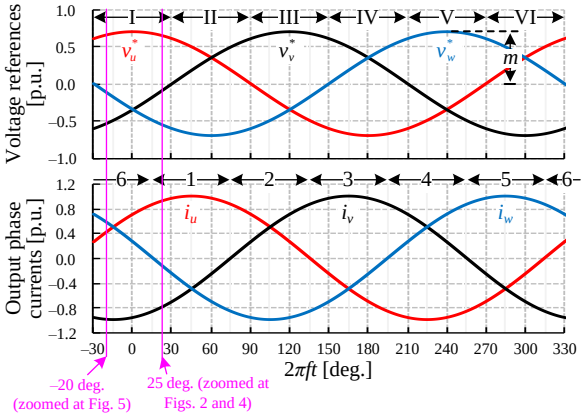



Fig. 1. Continuous voltage references $v^*_x$ and output phase currents $i_x$ at $m$ = 0.7 and cos $\varphi$ = 0.707. The voltage sectors (I~VI) are determined by the polarities of three-phase voltage references. The current sectors (1~6) are determined by the polarities of output phase currents.

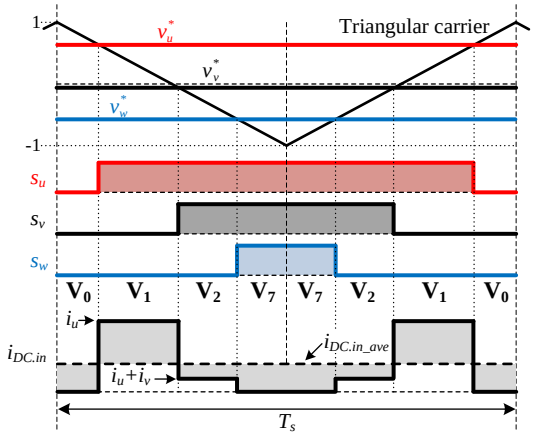



Fig. 2. Zoomed-in waveforms of voltage references of conventional CPWM $v^*_x$, switching functions $s_x$, and $i_{DC.in}$ at $m$ = 0.7, $2\pi ft$ = 25 deg., and cos $\varphi$ = 0.707.

### A. Adjustment Method for Gate Pulse Timings

Fig. 3 shows the adjustment method for the gate pulse timings with the voltage reference shift. Note that the proposed voltage references are realized based on the premise that the references can be updated at both the positive-peak and negative-peak of the triangular carrier with the general-purposed micro-computer. The proposed voltage references are generated by shifting the original continuous voltage references $v^*_x$ alternately to positive side and negative side in every half control period. At first, the shifting coefficient ($A_x$) between the original and shifted reference is defined as a value from 1.0 to 2.0. The shifting coefficient $A_x$ of 1.0 indicates that the voltage reference shift is not performed as in Fig. 3(a). The coefficient $A_x$ of 2.0 indicates that the voltage references are shifted maximally in linear-modulation region as in Fig. 3(b). When $v^*_x$ is positive as in Fig. 3, the maximum shifting amount $\Delta v^*_x$ at $A_x$ of 2.0 is limited by the positive-peak of carrier and calculated as 1– $v^*_x$. In case of the negative $v^*_x$, the maximum

$\Delta v^*_x$ is limited by the negative-peak of the carrier and calculated as $v^*_x+1$. Furthermore, the shifting amount $\Delta v^*_x$ is defined to be varied from zero at $A_x$ of 1.0 to the maximum shifting amount at $A_x$ of 2.0 linearly with regard to the value of $A_x$. Then, the positively-shifted voltage reference $v^*_{xp}$ and the negatively-shifted voltage reference $v^*_{xn}$ can be calculated as

$$\begin{cases} v^*_{xp} = v^*_x + \Delta v^*_x = (2 - A_x)\cdot v^*_x + A_x - 1 \\ v^*_{xn} = v^*_x - \Delta v^*_x = A_x \cdot (v^*_x - 1) + 1 \end{cases} \quad (\text{if } v^*_x \ge 0), \qquad (4)$$

$$\begin{cases} v^*_{xp} = v^*_x + \Delta v^*_x = A_x \cdot (v^*_x + 1) - 1 \\ v^*_{xn} = v^*_x - \Delta v^*_x = (2 - A_x)\cdot v^*_x - A_x + 1 \end{cases} \quad (\text{if } v^*_x < 0).$$

Note that (4) is dependent only on the polarity of $v^*_x$.

The gate pulse timings are adjusted during the control period while maintaining these original pulse widths by shifting the voltage references as in Fig. 3. In particular, the gate pulse adjustment length is determined by the value of $A_x$. In addition, the timing moves to the left when the voltage reference is shifted to the positive side in anterior half control period as in Fig. 3(b); in contrast, the gate pulse timing is shifted to the right when the voltage reference is shifted to the positive side in latter half control period.

### *B. Proposed Voltage References for DC-link Current Harmonics Reduction*

Fig. 4 shows the zoomed-in waveforms of the proposed voltage references, the switching functions, and the DC-link current at $m$ = 0.7, $2\pi ft$ = 25 degrees, and cos $\varphi$ = 0.707. This control period is located within the overlap period between sector I ($v^*_u > 0$, $v^*_v < 0$, and $v^*_w < 0$) and sector A ($i_u > 0$, $i_v < 0$, and $i_w < 0$). In case of the positive load power factor, i.e. driving mode, $i_{DC.in\_ave}$ is also positive according to (3). As observed in Fig. 1, only $i_u$ is positive at $2\pi ft$ = 25 degrees and cos $\varphi$ = 0.707. During this control period, $u$-phase voltage reference should become larger than the other two phase voltage references, and the gate pulse $s_u$ should cover $s_v$ and $s_w$ in the time domain to avoid the $i_{DC.in}$ polarity flip compared to the $i_{DC.in\_ave}$ polarity. If the above criterion is not satisfied, $i_{DC.in}$ becomes negative, leading to the large $i_{DC.in}$ fluctuation against the positive $i_{DC.in\_ave}$. In addition to the above criterion, the overlap of the other two gate pulses $s_v$ and $s_w$ should be shortened to further reduce $i_{DC.in}$ fluctuation around $i_{DC.in\_ave}$. With those modified gate pulse timings, the applying duration of the output voltage vector $\mathbf{V_1}$ (1 0 0), which causes the large difference between $i_{DC.in}$ (= $i_u$) and $i_{DC.in\_ave}$, can be shortened compared to the conventional CPWM shown in Fig. 2. In addition, the applying durations of $\mathbf{V_2}$ (1 1 0) and $\mathbf{V_6}$ (1 0 1), which result in the small $i_{DC.in}$ harmonics, can be extended and generated with those gate pulses. In order to achieve both the criterion for avoiding the $i_{DC.in}$ polarity flip compared to the $i_{DC.in\_ave}$ polarity and the criterion for reducing the $i_{DC.in}$ fluctuation,

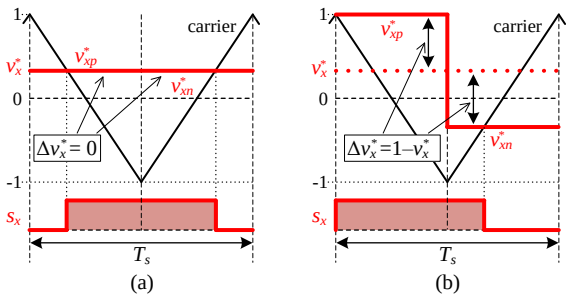



Fig. 3. Adjustment method for gate pulse timings with voltage reference shift. (a) $A_x$ = 1.0. (b) $A_x$ = 2.0.

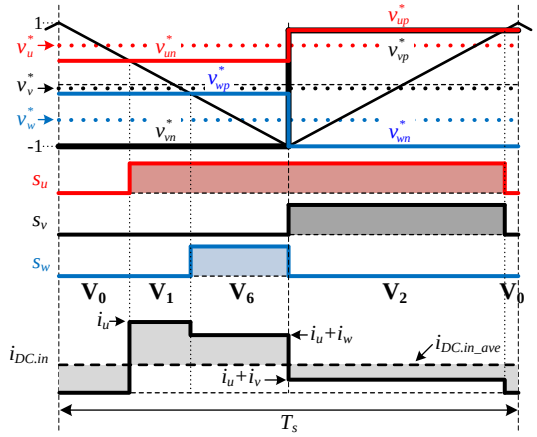



Fig. 4. Zoomed-in waveforms of voltage references of proposed CPWM $v^*_{x.PCPWM}$, switching functions, and $i_{DC.in}$ at $m$ = 0.7, $2\pi ft$ = 25 deg., and cos $\varphi$ = 0.707. The shifting coefficients between the original voltage references and shifted references are set as $A_u$ = 1.68, $A_v$ = 2.00, and $A_w$ = 2.00.

1) $v^*_u$, whose output phase current is positive, is shifted to the positive side simultaneously with the larger phase voltage reference between the other two phases, i.e. $v^*_v$.
2) $v^*_v$ and $v^*_w$ are shifted alternately and maximally to the positive side as long as they do not exceed $v^*_{up}$ and $v^*_{un}$.

Fig. 5 shows another example of the zoomed-in conventional and proposed voltage references at $m$ = 0.7, $2\pi ft$ = –20 degrees, and cos $\varphi$ = 0.707. This control period is located within the overlap period between sector I ($v^*_u > 0$, $v^*_v < 0$, and $v^*_w < 0$) and sector F ($i_u > 0$, $i_v < 0$, and $i_w > 0$). At $2\pi ft$ = –20 degrees and cos $\varphi$ = 0.707, only $i_v$ is negative as observed in Fig. 1. Note that the only different phase current polarity is negative which is inverse from the case in Fig. 4. Even at this case, both of the criterion for avoiding the $i_{DC.in}$ polarity flip and the criterion for reducing the $i_{DC.in}$ fluctuation are effective to reduce the harmonics. In order to achieve those criteria,

1) $v^*_v$, whose output phase current is negative, is shifted to the negative side simultaneously with the smaller phase voltage reference between the other two phases, i.e. $v^*_w$.
2) $v^*_u$ and $v^*_w$ are shifted alternately and maximally to the negative side as long as they do not become smaller than $v^*_{vp}$ and $v^*_{vn}$.

Fig. 6 shows the variation of $A_x$ and the proposed voltage references $v^*_{x.PCPWM}$ during one-cycle operation at $m$ = 0.7 and cos $\varphi$ = 0.707. As described in Figs 4 and 5, the voltage references are shifted in every half control period to satisfy both the criterion for avoiding the $i_{DC.in}$ polarity flip and the criterion for reducing the $i_{DC.in}$ fluctuation. Nevertheless, in case of cos $\varphi$ < 0.866 ($\varphi$ > 30 deg.), there are areas where the criterion for avoiding the $i_{DC.in}$ polarity flip cannot be satisfied. In the phase range of 0~15 degrees in Fig. 6, for example, only $i_v$ is negative; thus, $v$-phase voltage reference should become smaller than the other two phase voltage references to avoid the $i_{DC.in}$ polarity flip. However, the original $v$-phase voltage reference is not the minimum at this phase range and the criterion cannot be satisfied. At these phase ranges, the proposed voltage reference shift further worsens the DC-link current harmonics. Therefore, the conventional CPWM is applied at these phase ranges.

In case of the regenerative braking mode, $i_{DC.in\_ave}$ becomes negative according to (3). In this case, whether the certain phase voltage reference should be maximized or minimized in the criteria for DC-link current harmonics reduction is reversed against the driving mode. Note that whether the motor operating mode is driving or regenerative braking mode is detected from the voltage phase angle conditions and the detected output phase angle conditions [13].

### C. Design Flowchart of Shifting Coefficient $A_x$

Fig. 7 shows the design flowchart for $A_x$. At first, the conditions of the phase angle and the load current are detected from the voltage sector (I~VI) and the current sector (1~6), which are defined in Fig. 1. Then, $A_x$ is calculated to satisfy two criteria for the DC-link current harmonics reduction by using equation (4) and the gate pulse widths $t_x$. The gate pulse widths $t_x$ can be calculated from $v^*_x$ as

$$t_x = \frac{v^*_x + 1}{2}. \tag{5}$$

Note that there are 4 division processes to calculate all shifting coefficients in the worst case, which might result in a heavy computation load. In practical, the calculation of $A_x$ is performed offline and the values of $A_x$ are stored in a look-up table. Note that the offline calculation of $A_x$ provides the same current stress reduction effect as the online calculation because the value of $A_x$ varies only with the phase ($u$, $v$, $w$), the phase angle (0~360 deg.), the modulation index (0~1.0), and the load current conditions (sector 1~6), which is independent from the motor parameters.

## IV. Analytical Evaluations

### A. DC-link Capacitor RMS Current

The DC side of the three-phase VSI operates at six-fold fundamental frequency. Hence, the normalized DC-link capacitor rms current can be calculated based on (3) by considering only a sixth of the fundamental period as

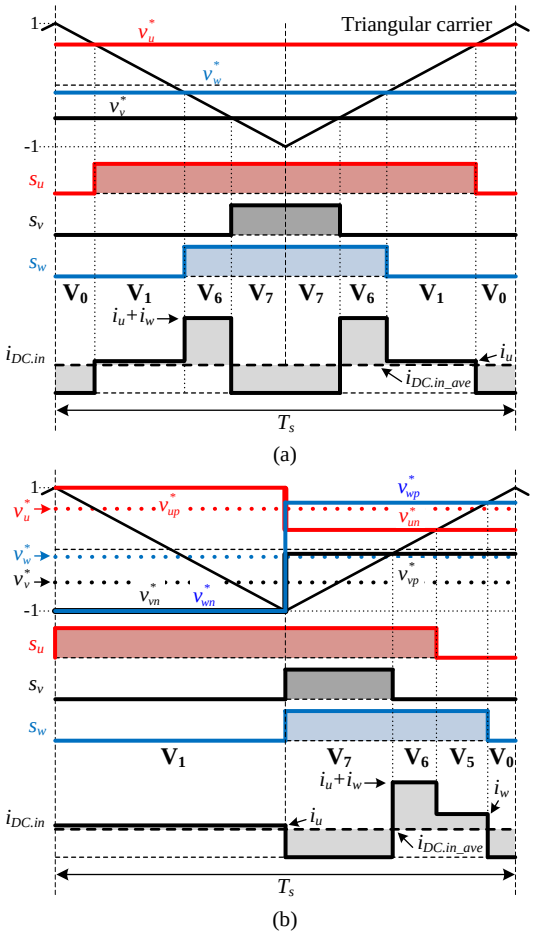



Fig. 5. Zoomed-in waveforms of voltage references, switching functions, and ideal $i_{DC.in}$ at $m$ = 0.7, $2\pi ft$ = –20 deg., and cos $\varphi$ = 0.707. (a) Conventional CPWM. (b) Proposed CPWM with $A_u$ = 2.00, $A_v$ = 2.00, and $A_w$ = 2.00.

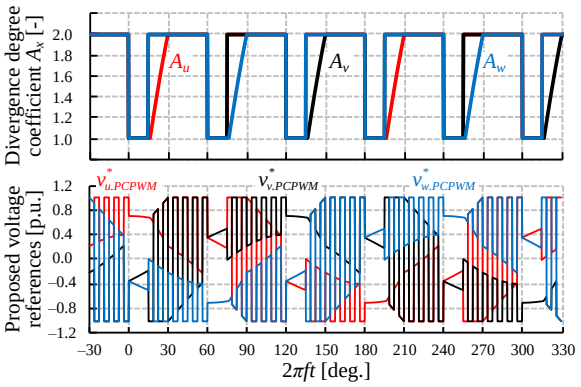



Fig. 6. Variation of $A_x$ and proposed voltage references $v^*_{x.PCPWM}$ during one-cycle operation at $m$ = 0.7 and cos $\varphi$ = 0.707. At the phase ranges of 0~15, 60~75, 120~135, 180~195, 240~255, and 300~315, the DC-link current harmonics cannot be reduced, and the conventional CPWM is applied. Note that the switching frequency is set to be low for better illustration.

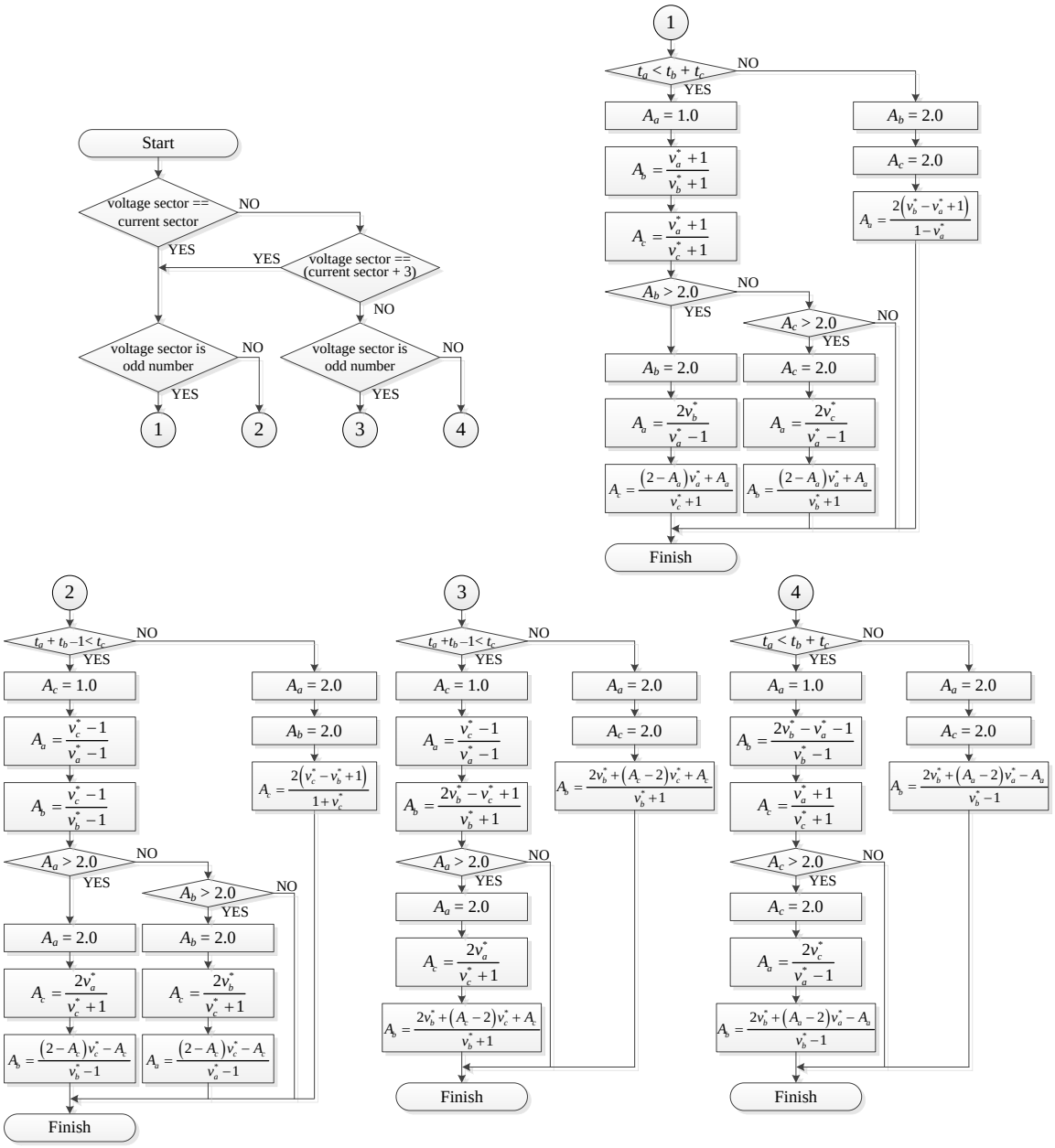



Fig. 7. Design flowchart for $A_x$. The phase with the most positive voltage reference is denoted as phase *a* while the phase with the most negative voltage reference is denoted as phase *c*. The phase which lies between phase *a* and phase *c* is denoted as phase *b*.

$$I_{C.rms(\text{p.u.})} = \frac{1}{I_m}\sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left(\sum\left[\frac{t_k}{T_s}\left(i_{DC.in.k} - i_{DC.in\_ave}\right)^2\right]\right)d\theta} \tag{6}$$

where $t_k$ is the on-duty of a VSI voltage space vector $\mathbf{V_k}$ ($s_u$, $s_v$, $s_w$) within $T_s$, and $i_{DC.in.k}$ is the instantaneous DC-link current value with the voltage space vector $\mathbf{V_k}$.

Fig. 8 shows the analytical results of the DC-link capacitor current with regard to the modulation index and the load power factor angle. Fig. 8(a) confirms that with the application of the conventional CPWM, $I_{C.rms(\text{p.u.})}$ becomes the maximum at around $m$ = 0.6 and absolute value of the load power factor $|\cos\varphi|$ = 1.0 due to the large difference between $i_{DC.in}$ (= 0 A) and $i_{DC.in\_ave}$ at the applying durations of zero vectors $\mathbf{V_0}$ (0 0 0) and $\mathbf{V_7}$ (1 1 1). On the other hand, Figs. 8(b) and (c) confirm that the proposed CPWM reduces $I_{C.rms(\text{p.u.})}$ under any conditions of $m$ and $\varphi$. In addition, a higher $|\cos\varphi|$ leads to a greater reduction effect on $I_{C.rms(\text{p.u.})}$. This trend is resulted from the relationship between $\varphi$ and the application ratio of the shifted voltage references in whole phase range. In case of $|\cos\varphi| > 0.866$, the two criteria for the DC-link current harmonics reduction can be satisfied over whole phase range. Therefore, the shifted voltage references are applied over whole phase range, leading a large reduction of $I_{C.rms(\text{p.u.})}$.

Nevertheless, in case of |cos $\varphi$| < 0.866, the conventional CPWM is partially applied in the phase ranges where the criteria cannot be satisfied. The application ratio of the shifted voltage references decreases as |cos $\varphi$| becomes small, and there is no $I_{C.rms(\text{p.u.})}$ difference between the conventional and proposed CPWM when cos $\varphi = 0$.

### *B. Load Current Quality*

In order to evaluate the load current quality, the concept of harmonic flux presented in [19] is used. This concept does not require the calculation of the harmonic spectrum of the inverter output voltage waveform, which is complicated for the proposed CPWM because of its gate pulse asymmetry in the carrier cycle. When the switching frequency model of the load motor is assumed as an inductance $L$, a harmonic load current vector $\mathbf{I_h}$ has a proportional relationship between the harmonic flux vector $\boldsymbol{\lambda_h}$ (time integral of the instantaneous error voltage vector) as

$$\boldsymbol{\lambda}_{\mathbf{h}} = L\mathbf{I}_{\mathbf{h}} = \int_{NT_s}^{(N+1)T_s} \left(\mathbf{V}_{\mathbf{k}} - \mathbf{V}^*\right) \cdot dt \tag{7}$$

where $\mathbf{V_k}$ ($k$ = 0~7) is the output voltage space vector of the VSI, and $\mathbf{V}^*$ is the voltage reference vector.

Fig. 9 shows one of examples of the harmonic flux trajectories at $m$ = 0.7 and $2\pi ft$ = 25 degrees. The calculation of (7) and Fig. 9 evaluate and visualize the ripple current on a per-carrier cycle base. Since the harmonic flux vector characteristic has six-fold space symmetry, the per-fundamental cycle (per 60 deg. in space) harmonic flux rms value, which characterizes the load current quality and the harmonic losses in the test motor, is calculated as follows

$$\lambda_{RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\int_{NT_s}^{(N+1)T_s} \left\|\boldsymbol{\lambda}_{\mathbf{h}}\right\|^2 dt.d\theta}. \tag{8}$$

Fig. 10 shows the harmonic flux rms values of several modulators. The distance between the trajectories and the origin, which is the initial value of $\boldsymbol{\lambda_h}$ at the beginning of the carrier cycle, corresponds to the magnitude of the harmonic flux [19]. Thus, Figs. 9–10 confirm that the proposed CPWM worsens the harmonic flux compared to those obtained with the conventional CPWM. The reason is because the proposed shifted voltage references result in the application of the voltage space vector which is not the closest to $\mathbf{V}^*$, i.e. $\mathbf{V_6}$ in Fig. 9. On the other hand, the proposed CPWM, of which voltage references do not contain triplen harmonics, has a better performance than the DPWM based DC-link current harmonics reduction modulation method presented in [14].

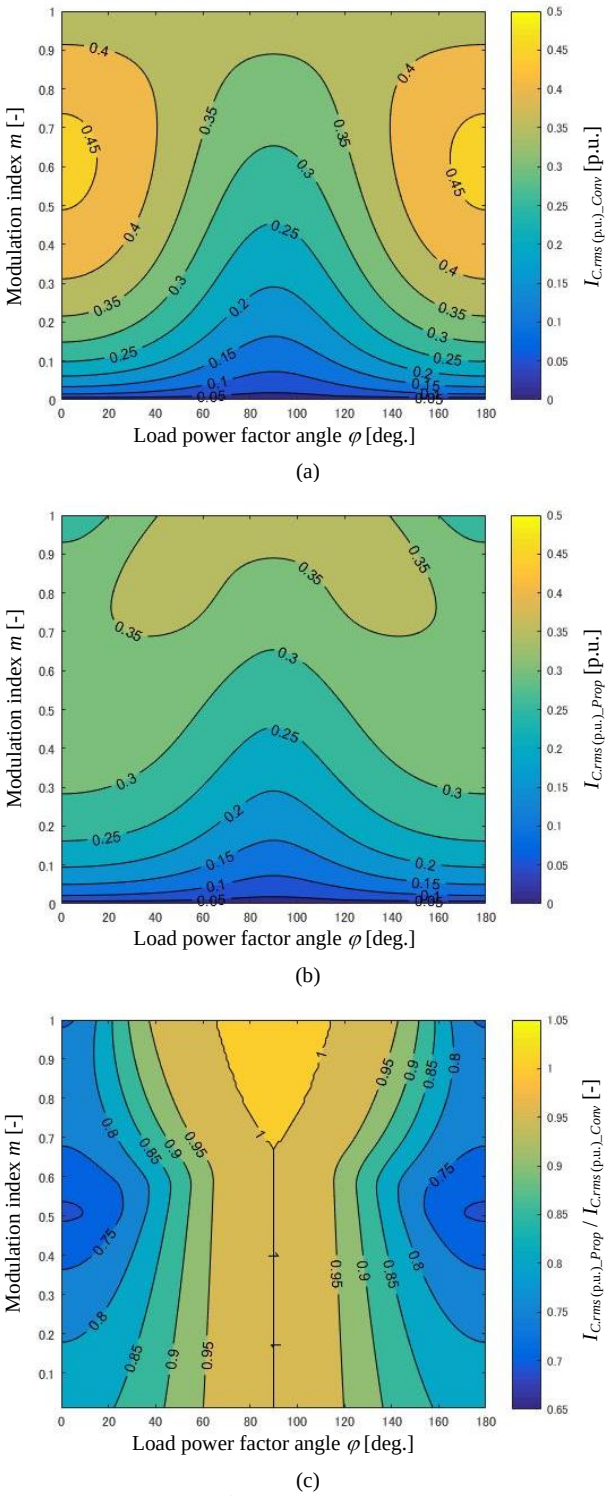



Fig. 8. Analytical results of DC-link capacitor rms current with regard to $m$ and $\varphi$. (a) $I_{C.rms(\text{p.u.})\_Conv}$. (b) $I_{C.rms(\text{p.u.})\_Prop}$. (c) $I_{C.rms(\text{p.u.})\_Prop}$ / $I_{C.rms(\text{p.u.})\_Conv}$ ratio.

## V. Simulation and Experimental Results

The performances of the conventional and proposed CPWM are verified in PLECS simulation and experiment. In this experiment, the three-phase 2-level VSI, composed of IGBT power module (7MBP50RA120, Fuji Electric Co., Ltd.), is operated at the switching frequency of 10 kHz. A three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.), the rated power of which is 3.7 kW, is used as a test motor and

controlled by V/f control with the conventional and proposed CPWM, which are implemented into an evaluation board TMS320C6713, Texas Instruments.

### *A. DC-link Current Harmonics*

Fig. 11 shows the *u*-phase voltage reference, the line-to-line voltage, the DC-link current, and the output *u*-phase current with each modulation method at $m = 0.550$ and $\cos\varphi = 0.866$. Note that the voltage references of the proposed CPWM are shifted in every half control period as shown in Fig. 11(b). As a result, the width of the step change in the DC-link capacitor is reduced. On the other hand, the larger transitions between $+E_{dc}$ and $-E_{dc}$ seem to occur in the line-to-line voltage with the proposed CPWM. However, the zoomed-in waveform of $v_{uv}$ shown in Fig. 11(b) confirms that the instantaneous voltage transition between $+E_{dc}$ and $-E_{dc}$ never occurs due to the dead-time period. Therefore, the proposed CPWM does not increase the motor surge voltage in practice compared to the conventional CPWM.

Fig. 12 shows the harmonic components of the DC-link current under the same conditions in Fig. 11. The maximum value of the vertical axis (100%) indicates the maximum value of the output phase currents. Even though the employment of the proposed CPWM worsens the 1st switching-frequency harmonic component of the DC-link current, the integer multiple components of the switching frequency are reduced compared to those with the conventional CPWM. Consequently, the proposed CPWM reduces the DC-link current harmonics by 24.2%. Note that the DC-link current harmonics is evaluated as $I_{DC.in(\text{p.u.})}$, which is the rms value of the DC-link current ($i_{DC.in.rms}$) normalized by the maximum value of the output phase current.

$$I_{DC.in(\text{p.u.})} = \frac{i_{DC.in.rms}}{I_m} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(\frac{1}{\sqrt{2}}i_{DC.in.n}\right)^2} \qquad (9)$$

where $n$ is the harmonic order, and $i_{DC.in.n}$ is the $n$-order

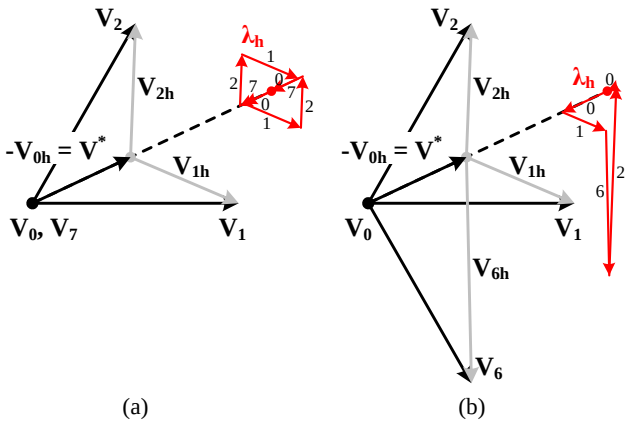



Fig. 9. Harmonic flux trajectories at $m = 0.7$ and $2\pi ft = 25$ deg. (a) Conventional CPWM. (b) Proposed CPWM.

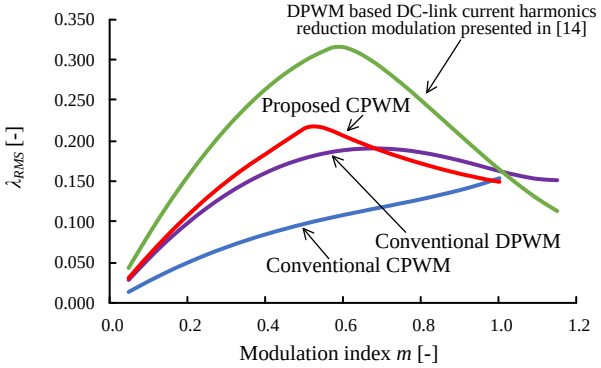



Fig. 10. Comparison of harmonic flux rms values. In the proposed CPWM calculations, the load power factor is set to 1.

component of the DC-link current harmonics. The harmonic components of the DC-link current up to 20th-order of the switching frequency are considered in this evaluation.

Figs. 13–14 show the VSI operating waveforms and the harmonic components of the DC-link current at $m = 0.550$ and $\cos\varphi = 0.643$, i.e. low load power factor condition. When $\cos\varphi = 0.643$, the periods where the proposed shifted voltage references are not adequate for reduction of the DC-link

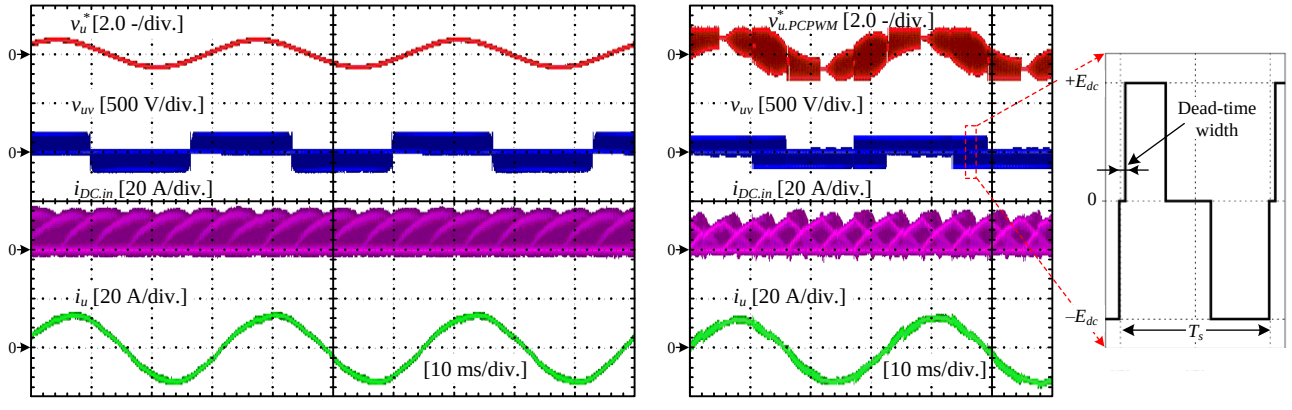



Fig. 11. *u*-phase voltage reference, line-to-line voltage, DC-link current, and output *u*-phase current at $m = 0.550$ and $\cos\varphi = 0.866$ (30 deg. lagging), i.e. high load power factor condition in driving mode. (a) Conventional CPWM. (b) Proposed CPWM. The zoomed-in waveform of $v_{uv}$ is from the simulation model using PLECS.

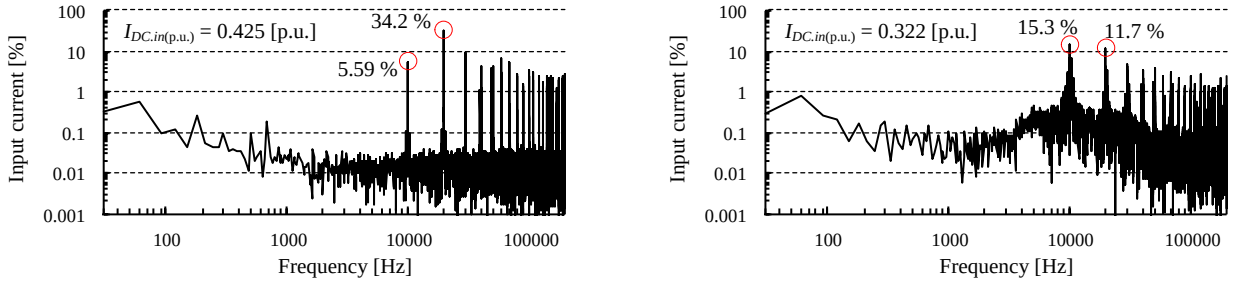



Fig. 12. Harmonic components of DC-link current at $m$ = 0.550 and cos $\varphi$ = 0.866 (under same conditions in Fig. 11). (a) Conventional CPWM. (b) Proposed CPWM.

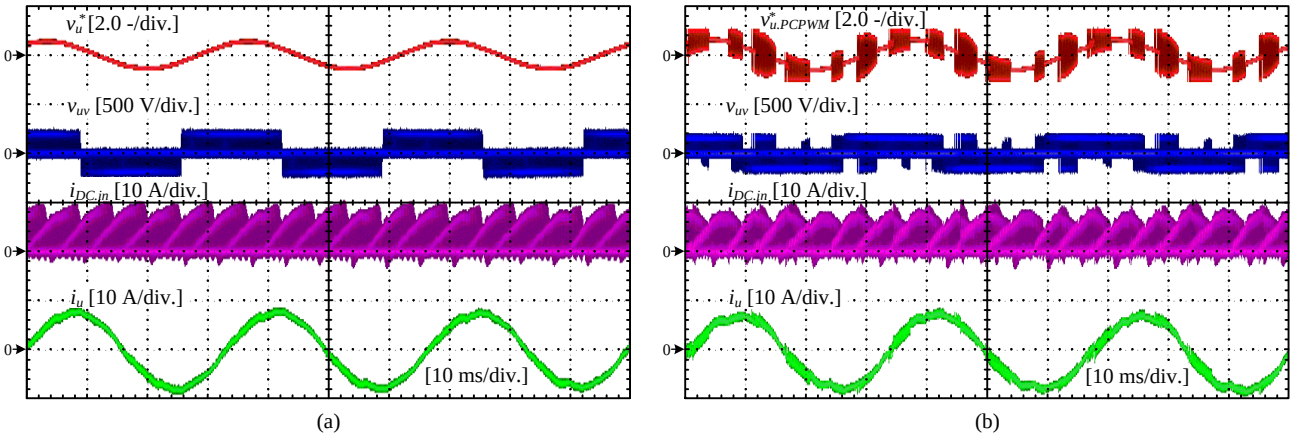



Fig. 13. $u$-phase voltage reference, line-to-line voltage, DC-link current, and output $u$-phase current at $m$ = 0.550 and cos $\varphi$ = 0.643 (50 deg. lagging), i.e. low load power factor condition in driving mode. (a) Conventional CPWM. (b) Proposed CPWM.

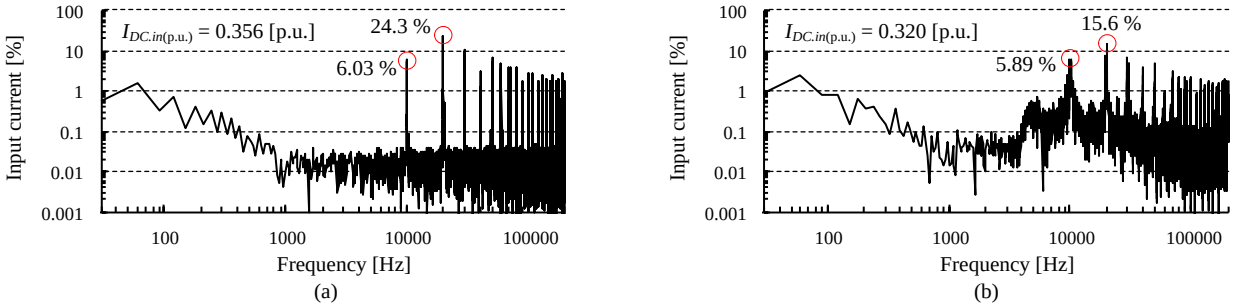



Fig. 14. Harmonic components of DC-link current at $m$ = 0.550 and cos $\varphi$ = 0.643 (under same conditions in Fig. 13). (a) Conventional CPWM. (b) Proposed CPWM.

current harmonics arise. Therefore, the conventional sinusoidal voltage references are partially applied in these periods. As a result, the proposed CPWM reduces the DC-link current harmonics by 10.2%. These results demonstrate that the proposed CPWM is effective in terms of reducing the DC-link current harmonics even when the load power factor is low.

Fig. 15 shows the simulation and experimental results of the DC-link current harmonics at cos $\varphi$ from 0.259 to 0.866, i.e. driving mode. The proposed CPWM reduces the DC-link current harmonics under any conditions of the modulation index and the load power factor. A higher load power factor enables a greater reduction effect on the DC-link current harmonics to be obtained. This trend is resulted from the relationship between $\varphi$ and the application ratio of the shifted voltage references in whole phase range, observed in Fig. 8.

Figs. 16–17 show the VSI operating waveforms and the harmonic components of the DC-link current at $m$ = 0.445 and cos $\varphi$ = –0.766, i.e. regenerative braking mode. The application of the proposed CPWM reduces the DC-link current harmonics even in the regenerative braking mode. These results confirm that the proposed CPWM is effective to reduce the DC-link current harmonics for the motor drive system, of which the variation of the load power factor is considerably wide.

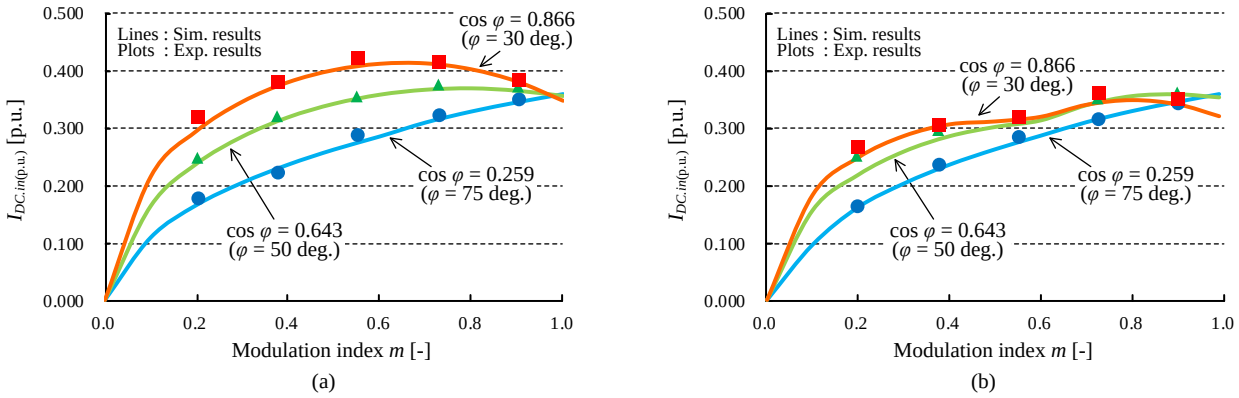



Fig. 15. Simulation and experimental results of DC-link current harmonics in driving mode. (a) Conventional CPWM. (b) Proposed CPWM.

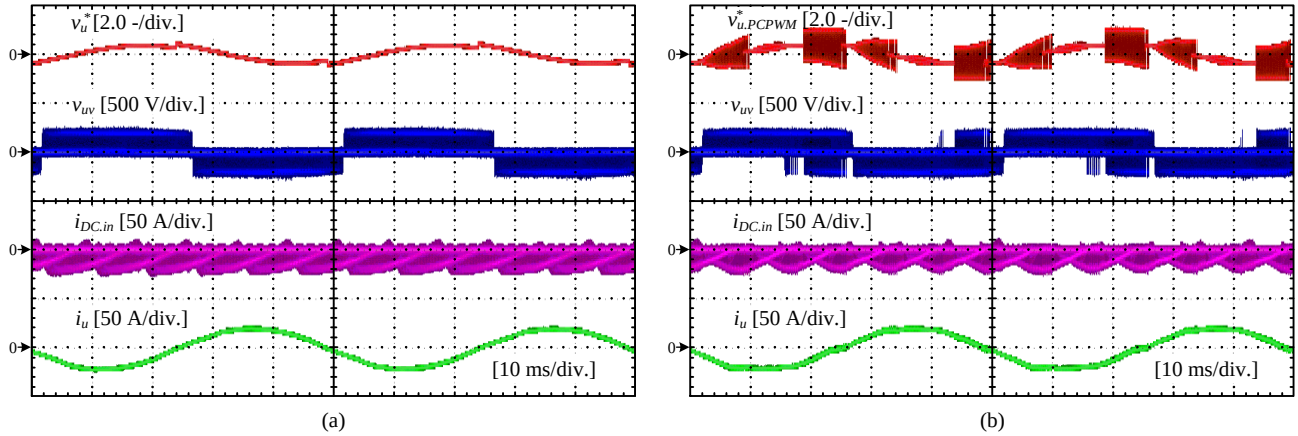



Fig. 16. *u*-phase voltage reference, line-to-line voltage, DC-link current, and output *u*-phase current at $m$ = 0.445 and cos $\varphi$ = –0.766 (140 deg. lagging) in regenerative braking mode. (a) Conventional CPWM. (b) Proposed CPWM.

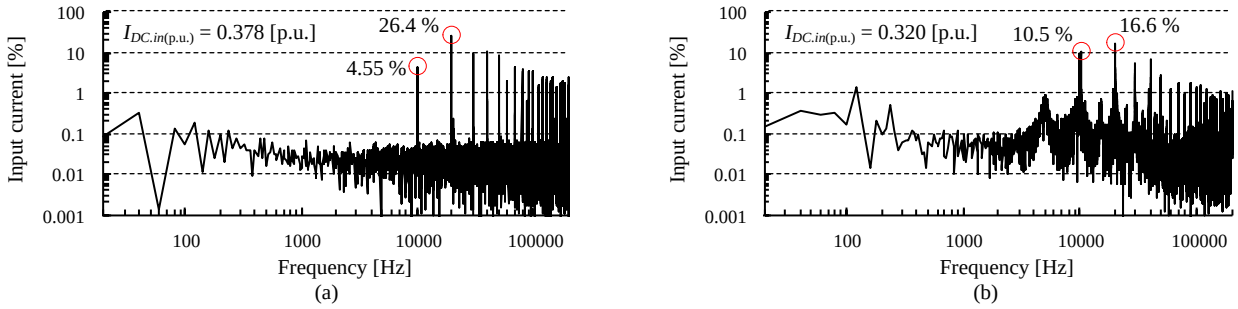



Fig. 17. Harmonic components of DC-link current at $m$ = 0.445 and cos $\varphi$ = –0.766 (under same conditions in Fig. 16). (a) Conventional CPWM. (b) Proposed CPWM.

### *B. Output Phase Current Harmonics*

Fig. 18 shows the total harmonic distortion (THD) of the output *u*-phase current at cos $\varphi$ = 0.866. The harmonic components up to 40$^{th}$-order of the fundamental frequency are considered in this evaluation. These characteristics are similar to the analytic results of the harmonic flux rms value shown in Fig. 10. The proposed CPWM leads to higher distortion of the output phase current compared to those with the conventional CPWM. Therefore, the application of the proposed CPWM results in a trade-off between the improved DC-link current harmonics and the worsened AC current harmonics. Nevertheless, those output current THD with the proposed CPWM is superior to those with the DPWM based DC-link current harmonics reduction modulation method presented in [14], and the almost same level of those with the conventional DPWM method. In addition, the worsened output current THD with the proposed CPWM can be improved by increasing the switching frequency in case with the inductive load. Note that the higher switching frequency leads to the increase of the switching losses; however, those impact on the inverter efficiency can be reduced by applying the wide band gap device such as SiC or GaN.

### C. Inverter Efficiency

Fig. 19 shows the inverter efficiency between the conventional and proposed CPWM at cos $\varphi$ = 0.866. The inverter efficiency is measured using Yokogawa WT 1800 power analyzer. The application of the proposed CPWM does not influence on the inverter efficiency and the same level efficiency with the conventional CPWM to be obtained due to its same number of switching transitions compared with the conventional CPWM, which can be observed from Figs. 2, 4.

## VI. Temperature Rise Test for DC-link Capacitors

Fig. 20 shows the temperature rise test setup. The DC-link capacitor and the inverter are placed inside thermally-insulated container (EPFH-125-2S, ISUZU), whereas the temperature test starts from 25.0°C.

Fig. 21 shows the film capacitor under test as the DC-link capacitor. The thermocouple is built in the central part of the film capacitor. An equivalent series resistance (ESR) is measured using HIOKI 3532-50 LCR tester. At very low frequencies, the ESR is high due to prevalent leakage. At low frequencies, ESR is dominated by the dielectric losses which decrease in inverse proportion to the frequency. At medium to high frequencies, the losses in the conductors are dominant and ESR becomes relatively constant. At high frequencies, ESR increases again due to the skin effect [20].

Figs. 22–23 show the VSI operating waveforms and the harmonic components of the DC-link capacitor current $i_{Cap}$ through the temperature rise test at $m$ = 0.643, cos $\varphi$ = 0.891 and the inverter output power $P_{inv}$ of 2.7 kW. The proposed CPWM reduce the switching frequency component of the capacitor current. Furthermore, the capacitor loss, which can be calculated as follows, is reduced by 31.7% with the proposed CPWM.

$$P_{Cap} = \sum_{n=1} \left( R_{ESR.n} \cdot i_{Cap.n}^2 \right). \tag{10}$$

Fig. 24 shows the measured capacitor core temperature. The temperature rise tests are conducted until the container internal temperature reaches 60°C, the rated temperature of the coated vinyl of wire, while VSI operating under the experimental conditions in Figs. 22–23. Assuming that the container has a sufficient thermal resistance and the leakage heat through the container is negligible, the heat quantity $Q$ of the film capacitor and its temperature $T$ have following relationship.

$$Q = c_{PP} w \cdot \left( T - T_0 \right) \tag{11}$$

where $c_{PP}$ is the specific heat capacity of polypropylene, the value of which is 1.93 J/g·°C [21], $w$ is the capacitor weight, and $T_0$ is the capacitor initial temperature. Note that, the inverter loss does not change with the conventional and proposed CPWM which can be observed from Fig. 19. Thus, the capacitor temperature difference between the cases with

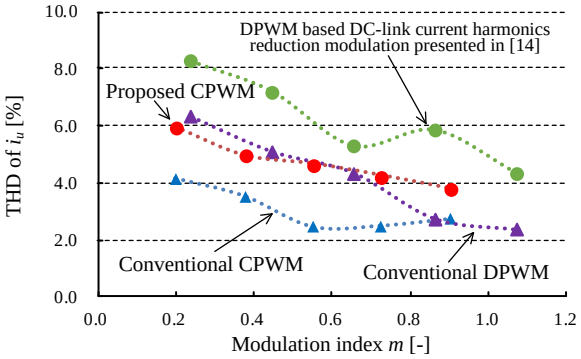



Fig. 18. THD of output $u$-phase current $i_u$ at cos $\varphi$ = 0.866.

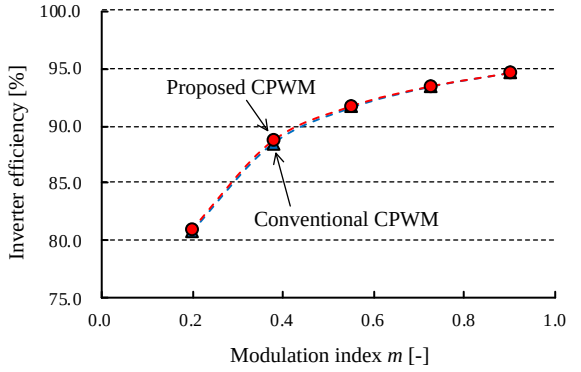



Fig. 19. Inverter efficiency comparison between conventional and proposed CPWM against different modulation index at cos $\varphi$ = 0.866.

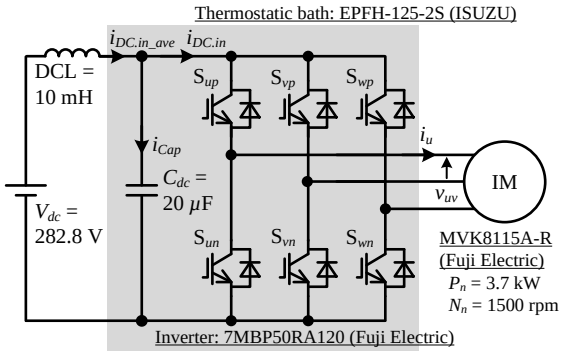
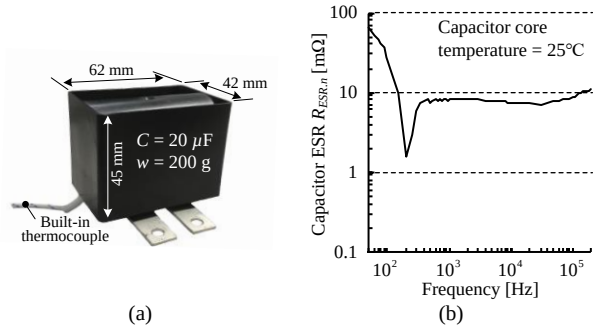



Fig. 20. Temperature rise test setup.




(a) (b)

Fig. 21. Film capacitor under test. (a) Photograph of film capacitor. (b) Measured ESR.

the conventional and proposed CPWM after $t$ seconds is calculated as

$$T_{conv}(t) - T_{prop}(t) = \frac{\left(P_{Cap.conv} - P_{Cap.prop}\right) \cdot t}{c_{\mathrm{PP}} w}. \qquad (12)$$

The estimated capacitor temperature difference after 7200 seconds based on the capacitor losses and (12) is 4.59℃, besides the temperature test results in Fig. 24 confirm the capacitor temperature difference of 4.4℃ after 7200 seconds. Thus, the experimental results agree well with the theoretical value. Furthermore, the proposed CPWM lowers the equilibrium capacitor temperature, which is estimated from the test results using the least-square method, by 6.0℃ compared to the conventional CPWM.

## VII. Conclusion

The novel CPWM was proposed to reduce the DC-link current harmonics of the three-phase VSI, which flowed through the DC-link capacitor, over wide variation of the load power factor. Furthermore, the high cost hardware such as FPGA was not necessary because this PWM strategy was realized with only one triangular carrier. The DC-link capacitor current rms value were reduced by shifting the voltage references in every half control period to reduce the fluctuation of the DC-link current around its average value. On the other hand, the CPWM had a drawback of the large distortion of the VSI output line-to-line voltage and phase current as a result of the DC-link current harmonics reduction.

The experimental results confirmed that the application of the proposed CPWM reduced the rms value of the DC-link current by 24.2% at most, and lowered the equilibrium capacitor temperature by 6.0℃ compared to the conventional CPWM. Furthermore, the proposed CPWM achieves the same level inverter efficiency with the conventional CPWM. Therefore, the proposed CPWM contributed to the current stress reduction on the DC-link capacitor, resulting in the thermal stress reduction and the reliability improvement for the DC-link film capacitors which are the heat-sensitive components without worsening the inverter efficiency. On the other hand, the proposed CPWM led to two drawbacks for being adopted in real practice: the worsened output current distortion, and the heavy computation load for calculating the shifting coefficients $A_x$ online. Note that the worsened motor current THD can be improved by increasing the switching frequency while achieving the same reduction effect on the DC-link current harmonics, which is independent on the switching frequency. Furthermore, the computation load problem can be solved by calculating $A_x$ offline and storing these values in a look-up table with the same current stress reduction effect as the online calculation.

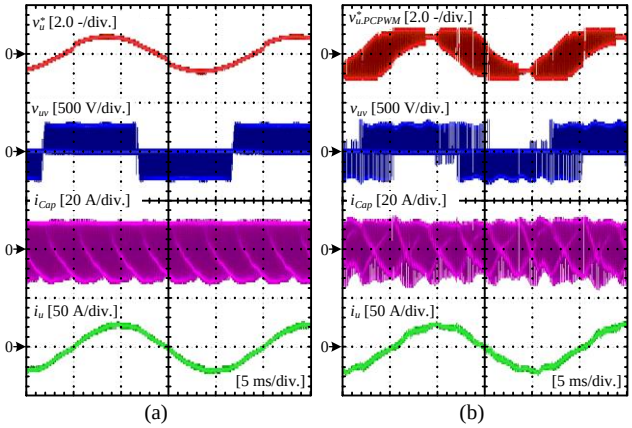



Fig. 22. Operating waveforms through temperature rise test at $m$ = 0.643, cos $\varphi$ = 0.891, and $P_{inv}$ = 2.7 kW. (a) Conventional CPWM. (b) Proposed CPWM.

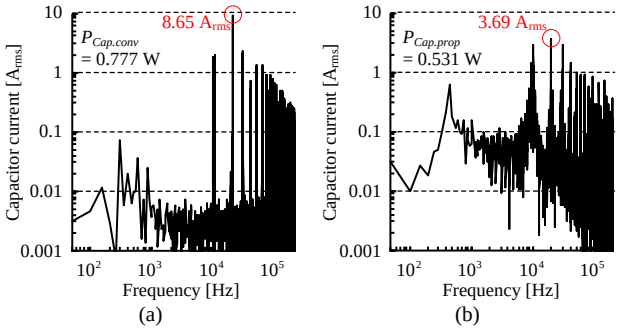



Fig. 23. Harmonic components of DC-link capacitor current at $m$ = 0.643, cos $\varphi$ = 0.891, and $P_{inv}$ = 2.7 kW (under same conditions in Fig. 22). (a) Conventional CPWM. (b) Proposed CPWM.

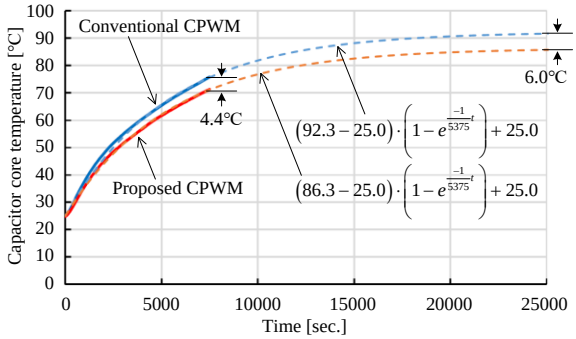



Fig. 24. Measured capacitor core temperature and its approximated curve.

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