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Paper

Microcomputer-based Discontinuous PWM for DC-link Current Harmonic Reduction in Three-phase VSIs

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This paper proposes a novel discontinuous pulse width modulation (DPWM) strategy to reduce the switching-frequency-order DC-link current harmonics for a two-level three-phase voltage source inverter (VSI). The proposed modulation method realizes a long lifetime of the smoothing capacitor to the motor drive system. Furthermore, the proposed strategy requires only one carrier; thus, high cost hardware such as field-programmable gate arrays are unnecessary. The DC-link current harmonics are reduced by shifting two unclamped modulating signals in every half control period. In addition, the injection of the zero sequence signal to all discontinuous modulating signals optimizes the phase of the clamped modulating signal and its clamped value according to the conditions of the output phase currents; consequently, the DC-link current harmonics are reduced even when the load power factor varies. Experiments confirm that the proposed DPWM strategy can reduce the DC-link current harmonics by a maximum of 18.3% at a modulation index of 0.705 and a load power factor of 0.819.

Keywords : Two-level voltage source inverter, Discontinuous PWM, DC-link capacitors, DC-link current harmonics

1. Introduction

Three-phase AC motors are widely utilized in widespread applications such as traction and automotive and so on[(1)–(7)]. Recently, lifetime extension of such system has been actively researched[(8)–(12)]. Generally, electrolytic capacitors are applied in the DC-link of the PWM inverter as a smoothing capacitor. The smoothing capacitor acts as an energy buffer to stabilize the DC-link voltage and guarantees a dynamic performance of the system by suppressing an overshoot voltage during a transient state. These functions are realized by using bulky electrolytic capacitors which make the system large and less reliable.

The DC-link capacitors absorb large switching-frequency harmonics contained in the PWM inverter DC-link current, leading joule losses in the equivalent series resistance (ESR) of the capacitors. The internal heating considerably worsens the capacitor reliability according to the *Arrhenius equation*[(13)]. There are several methods to extend the lifetime of the smoothing capacitor. One of the approaches is the application of film capacitors instead of the electrolytic capacitor as the smoothing capacitor[(14)]. However, this method makes the system larger due to its low energy density.

Meanwhile, it is also possible to extend the lifetime of the smoothing capacitor by reducing the DC-link current harmonics of VSI. So far, numerous modulation methods of VSI, which reduce the DC-link current harmonics of VSI, have been also proposed[(8)–(10), (15)]. In (8)–(10), double carriers, two inverted triangular carriers, are used as a double-carrier-comparison pulse width modulation (PWM). In these modulation methods, the DC-link current harmonics are reduced by comparing only one certain phase modulating signal with the inverse triangular carrier and comparing the other two modulating signals with the original triangular carrier. However, this method leads to a constraint of the digital hardware due to the generation of the inverse triangular carrier. Furthermore, when the load power factor becomes lower than 0.866, the DC-link current harmonics cannot be reduced by these methods.

As another approach to minimize the DC-link current harmonics, a new space vector PWM (SVPWM) has been proposed[(15)]. In this SVPWM, the optimized voltage space vectors for the DC-link current harmonic reduction are selected on the basis of the detected output phase current directions to adapt to the variation of the load power factor. However, the employment of this SVPWM also leads a constraint of the digital hardware such as FPGA because the SVPWM not only compares the on-duties of the selected output voltage space vectors with single carrier but also decides the gating signals based on the carrier comparison results to realize the optimized combinations of the voltage space vectors.

This paper proposes a novel carrier-comparison DPWM which uses only one carrier to reduce the switching-frequency-order DC-link current harmonics of VSI and eliminates the need of the complex digital hardware. In other words, the proposed DPWM is simply implemented with the general-purpose microcomputer without additional digital hardware. In order to reduce the DC-link current harmonics by using just only one carrier, two unclamped phase modulating signals of the conventional DPWM are optimally shifted in every half control period. Furthermore, the injection of the zero sequence signal to all discontinuous modulating signals optimizes the phase of clamped modulating signal and its clamped value according to the conditions of the output phase currents; consequently, the DC-link current harmonics are reduced even when the load power factor varies.

This paper is organized as follows; first, the reduction method of

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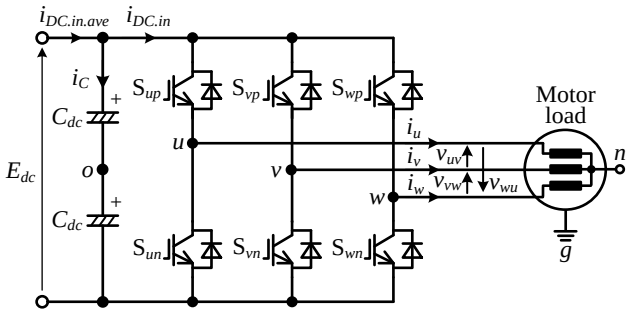


Fig. 1. Three-phase two-level VSI with motor load.

the DC-link current harmonics by using the novel modulating signals of the DPWM is introduced. Next, the mechanism to adapt the variation of the load power factor is explained. Then, the performances on the input current harmonics, the output current harmonics and the inverter efficiency are compared between the conventional and proposed DPWM by analysis and experiment. Finally, the electrolytic capacitor lifetimes with those DPWM are estimated and compared.

2. Proposed PWM method to reduce DC-link current harmonics of VSIs

2.1 Conventional Discontinuous PWM Fig. 1 shows a three-phase two-level VSI with a motor load. This circuit consists of three legs. If IGBTs are treated as ideal switches, the conduction status of any one leg can be represented by binary switching functions:

$$s_x = \begin{cases} 1, & (S_{xp}:\mathrm{ON},\ S_{xn}:\mathrm{OFF}) \\ 0, & (S_{xp}:\mathrm{OFF},\ S_{xn}:\mathrm{ON}) \end{cases}, \quad (x = u, v, w). \quad \text{..... (1)}$$

Fig. 2 shows the modulating signals of the continuous PWM (CPWM), conventional DPWM and its injected zero sequence signal at the modulation index of 0.8. The discontinuous modulating signals are obtained by injecting the zero sequence signal v^*_{offset} into the continuous modulating signals as[16]:

$$\begin{cases} v^*_{u.CPWM} = m\cdot\cos(2\pi ft) \\ v^*_{v.CPWM} = m\cdot\cos(2\pi ft - 2\pi/3), \\ v^*_{w.CPWM} = m\cdot\cos(2\pi ft + 2\pi/3) \end{cases} \quad \text{..... (2)}$$

$$v^*_{offset} = \begin{cases} 1-|v_{\max}| & \text{if } |v_{\max}| \ge |v_{\min}| \\ -1+|v_{\min}| & \text{if } |v_{\min}| < |v_{\max}| \end{cases}$$

$$\text{and} \begin{cases} v_{\max} = \max[v^*_{u.CPWM}, v^*_{v.CPWM}, v^*_{w.CPWM}] \\ v_{\min} = \min[v^*_{u.CPWM}, v^*_{v.CPWM}, v^*_{w.CPWM}] \end{cases}, \quad \text{..... (3)}$$

$$v^*_{x.DPWM} = v^*_{x.CPWM} + v^*_{offset}, \quad (x = u, v, w), \quad \text{..... (4)}$$

where m is the modulation index.

Fig. 3 shows the zoomed-in waveforms of the modulating signals of the conventional DPWM, the three-phase switching functions and the DC-link current at the modulation index of 0.8, the phase angle of 50 degrees and the unity load power factor. The instantaneous value of the DC-link current is a superposition summation of the switched current pulses from each phase leg and calculated as[17]:

$$i_{DC.in} = \sum_{x=u,v,w} (s_x \times i_x). \quad \text{..... (5)}$$

The shaded areas in the DC-link current waveform indicates the time integral of the difference between the instantaneous value and

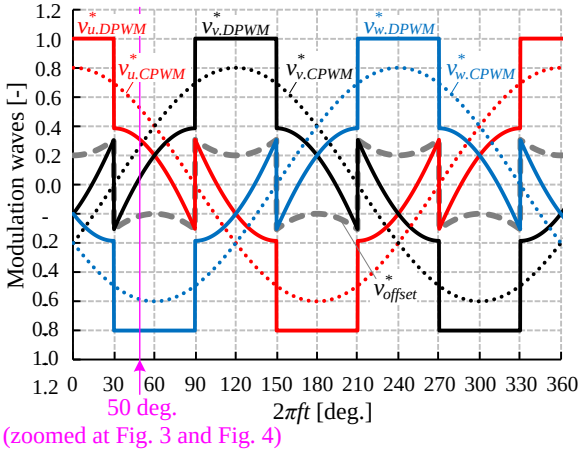


Fig. 2. Modulating signals of CPWM, conventional DPWM and its injected zero sequence signal at m = 0.8.

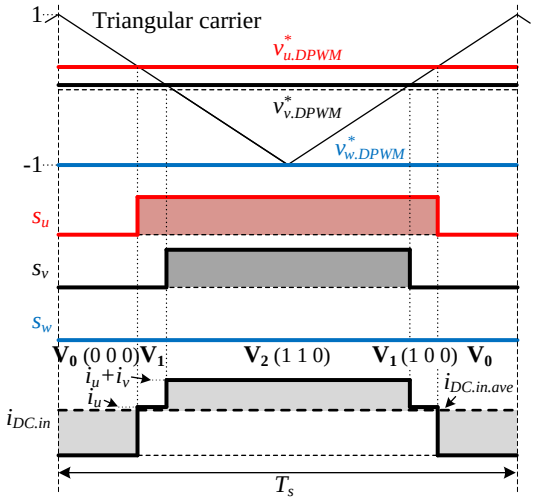


Fig. 3. Zoomed-in waveforms of modulating signals of conventional DPWM, switching functions and DC-link current at m = 0.8, $2\pi ft$ = 50 deg., cos φ = 1.

an average value of the DC-link current. These area correspond to the root-mean-square (RMS) value of the DC-link capacitor current based on the geometrical difference between the RMS value of the DC-link current $i_{DC.in.RMS}$ and the average value of the DC-link current $i_{DC.in.ave}$ as follows:

$$i_{C.RMS}(T_s) = \sqrt{i^2_{DC.in.RMS}(T_s) - i^2_{DC.in.ave}}$$

$$\text{and} \begin{cases} i_{DC.in.RMS}(T_s) = \sqrt{\dfrac{1}{T_s}\int_0^{T_s} i^2_{DC.in}\,dt} \\ i_{DC.in.ave} = \dfrac{3}{4} m \cdot I_m \cos\varphi \end{cases}, \quad \text{..... (6)}$$

where T_s is the control period, I_m is the maximum value of the output phase current and φ is the load power factor angle. Note that a smaller fluctuation of the DC-link current around its average value results in a smaller RMS value of the DC-link capacitor current[18]. In cases where the conventional DPWM is applied, the center of the gate pulses are matched to the center of the control period, leading a long overlap period of the gate pulses. This results in a large fluctuation of the DC-link current around its average value, i.e. the high DC-link capacitor current harmonics.

2.2 Microcomputer-based Approach to Reduce Harmonics Fig. 4 shows the zoomed-in waveforms of the

modulating signals of the proposed DPWM, the three-phase switching functions and the DC-link current at the modulation index of 0.8, the phase angle of 50 degrees and the unity load power factor. The operation of the proposed DPWM changes corresponding to the load power factor. In this section, the load power factor is considered as unity. The basic concept of the proposed DPWM for the DC-link current harmonic reduction is to shorten the zero-vector period, i.e. period where $(s_u\ s_v\ s_w) = (0\ 0\ 0)$ or $(1\ 1\ 1)$, during the control period, leading to the reduction of the DC-link current fluctuation around its average value. Therefore, the basic concept of the proposed DPWM is similar to that of the conventional DC-link current harmonic reduction SVPWM method[15]. In the proposed DPWM, this concept is realized under the premise that the modulating signals can be updated at positive and negative peaks of the triangular carrier, which is constraint of the microcomputer. In order to adjust the gate pulse positions as shown in Fig. 4, only two unclamped phase modulating signals $v^*_{u.DPWM}$ and $v^*_{v.DPWM}$ should be updated, whereas the clamped modulating signal $v^*_{w.DPWM}$ does not change. Each proposed modulating signal is generated by shifting the unclamped original DPWM modulating signal as:

$$\begin{cases} v^*_{xp} = 1 \\ v^*_{xn} = 2 \cdot v^*_{x.DPWM} - 1 \end{cases} \left(\text{if } v^*_{x.DPWM} \geq 0\right)$$
$$\begin{cases} v^*_{xp} = 2 \cdot v^*_{x.DPWM} + 1 \\ v^*_{xn} = -1 \end{cases} \left(\text{if } v^*_{x.DPWM} < 0\right), \quad \text{..... (7)}$$

where v^*_{xp} is the positively-shifted modulating signal, and v^*_{xn} is the negatively-shifted modulating signal. Note that the overlap period between two unclamped phases' switching functions, s_u and s_v in Fig. 4, should be shortened to reduce the fluctuation of the DC-link current around its average value. Therefore, these two phase modulating signals are alternately shifted to the positive side. Besides, the averaged values of the shifted modulating signals in each control period are same as those of the original signals, whereas the pulse widths of the switching functions are unchanged[19].

However, note that the reduction effect on the DC-link current harmonics by the use of the shifted modulation signals is dependent on the load power factor because the instantaneous value of the DC-link current is also dependent on the output phase currents. Thus, it is necessary to deal with the wide variation of the load power factor, which is a typical requirement of the motor drive system.

2.3 Adaption to Wide Load Power Factor Range

Table 1 lists the sector definition of the load current conditions. These sectors are determined by the combination of the detected output phase current directions.

Fig. 5 shows the conventional and proposed discontinuous modulating signals at the modulation index of 0.8 and the load power factor of 0.966 (15 deg. lagging). In order to reduce the DC-link current harmonics at any condition of the load power factor, first, three conventional discontinuous modulating signals $v^*_{x.DPWM}$ ($x = u, v, w$) are added with the offset $v^*_{offset.2}$ to obtain the voltage reference with the offset $v^*_{x.PDPWM}$ as:

$$v^*_{x.PDPWM} = v^*_{x.DPWM} + v^*_{offset.2}$$
$$\text{and } v^*_{offset.2} = \begin{cases} K_{OCV} - v^*_{u.DPWM} & \text{if sector} = \text{A, D} \\ K_{OCV} - v^*_{v.DPWM} & \text{if sector} = \text{B, E} \\ K_{OCV} - v^*_{w.DPWM} & \text{if sector} = \text{C, F} \end{cases} \quad \text{..... (8)}$$

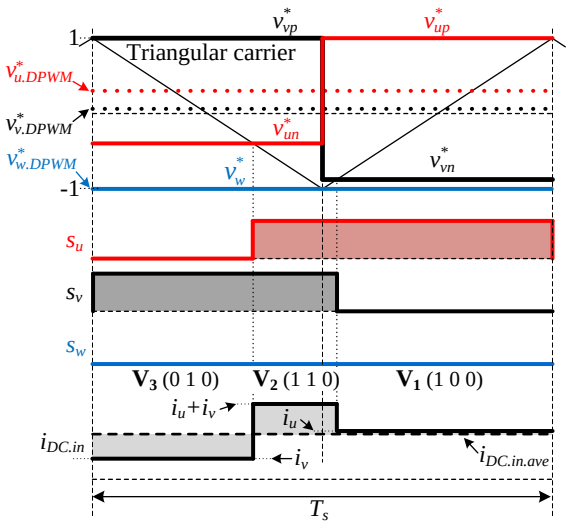


Fig. 4. Zoomed-in waveforms of modulating signals of proposed DPWM, switching functions and DC-link current at $m = 0.8$, $2\pi ft = 50$ deg., $\cos\varphi = 1$.

Table 1. Sector definitions of proposed DPWM.

Sector	Current polarity (P: Positive, N: Negative) i_u	i_v	i_w	Optimized clamped value K_{OCV} Driving	Reg. Braking
A	P	N	N	1	–1
B	P	P	N	–1	1
C	N	P	N	1	–1
D	N	P	P	–1	1
E	N	N	P	1	–1
F	P	N	P	–1	1

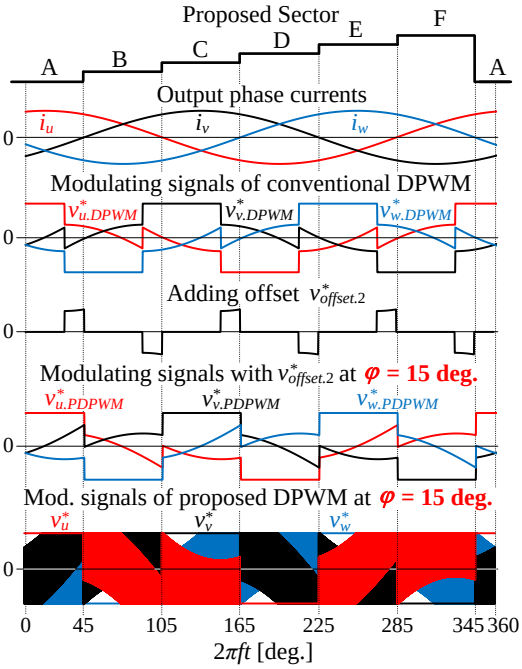


Fig. 5. Proposed modulating signals at $m = 0.8$ $\cos\varphi = 0.966$ (15 deg. lagging). $v^*_{x.PDPWM}$ is generated by adding an offset $v^*_{offset.2}$ to $v^*_{x.DPWM}$ to maintain the clamped period of the modulating signal at each proposed sector. The proposed modulating signals are then generated by shifting two unclamped modulating signals of $v^*_{x.PDPWM}$ in every half control period.

where K_{OCV} is the optimized clamped value of the modulating signal in each proposed sector listed in Table 1. The offset value $v^*_{offset.2}$ is optimized according to the conditions of the output phase currents and the clamped phase of the modulating signals. In the case of sector B, for example, where i_u and i_v are positive and i_w is negative, w-phase switching function s_w must be zero to obtain the minimum fluctuation of the DC-link current around its average value. If s_w becomes 1 during the sector B, the instantaneous value of the DC-link current becomes negative, which leads to a large fluctuation, i.e. the large increase in the DC-link current harmonics. Next, two unclamped offset-added modulating signals $v^*_{x.PDPWM}$ are shifted based on the sub-section 2.2, resulting in the proposed modulating signals v^*_x. With this optimization for the clamped phase and its value of the modulating signal based on the load current conditions, the DC-link current harmonics is reduced even when the load power factor varies[19].

In case of the regenerative braking mode, the average value of the DC-link current become a negative value. Therefore, the optimized clamped value K_{OCV} of the modulating signal for the reduction of the DC-link current fluctuation around its average value in each proposed sector is reversed between driving and regenerative braking modes as listed in Table 1. Note that whether the motor operating mode is driving or regenerative braking can be detected from the polarity combinations of the modulating signals and the detected output phase currents[15]. In addition, the shifting of the other two unclamped offset-added modulating signals in every half control period is also performed in the case of regenerative braking mode as the driving mode.

Fig. 6 shows the conventional and proposed discontinuous modulating signals at the modulation index of 0.8 and the load power factor of 0.707 (45 deg. lagging). In the case where the load power factor is lower than 0.866 ($\varphi < 30$ deg.), the proposed offset-added modulating signals $v^*_{x.PDPWM}$ might be more than 1 or lower than -1 due to the addition of the offset $v^*_{offset.2}$ in each sector, leading an overmodulation operation. Therefore, the conventional DPWM is applied in these periods as shown in the gray-colored periods in Fig. 6. Accordingly, the phase of the clamped modulating signal is not optimized for the reduction of the DC-link current harmonics; thus, the modulating signal shift in every half control period are not performed in these periods.

3. Analytical Evaluations

3.1 DC-link Capacitor RMS Current As explained in the sub-section 2.1, the RMS value of the DC-link capacitor current is dependent on m, φ and the switching patterns. The DC side of the three-phase VSI operates at sixfold fundamental frequency; hence, the normalized DC-link capacitor RMS current can be calculated based on (6) by considering only a sixth of the fundamental period:

$$I_{C.RMS(\mathrm{p.u.})} = \frac{1}{I_m}\sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left(\sum\left[\frac{t_x}{T_s}\left(i_{DC.in.x} - i_{DC.in.ave}\right)^2\right]\right)d\theta} \quad \ldots (9)$$

where t_x is the ON duty of a VSI voltage space vector $\mathbf{V_x}$ (s_u, s_v, s_w) within T_s, and $i_{DC.in.x}$ is the instantaneous DC-link current value with this voltage space vector $\mathbf{V_x}$.

Fig. 7 shows the analytical results of the DC-link capacitor current with regard to the modulation index m and the load power factor angle φ. It can be seen from Fig. 7 that the proposed DPWM performs better in terms of the DC-link capacitor RMS current compared to the conventional DPWM under any cases of m and φ.

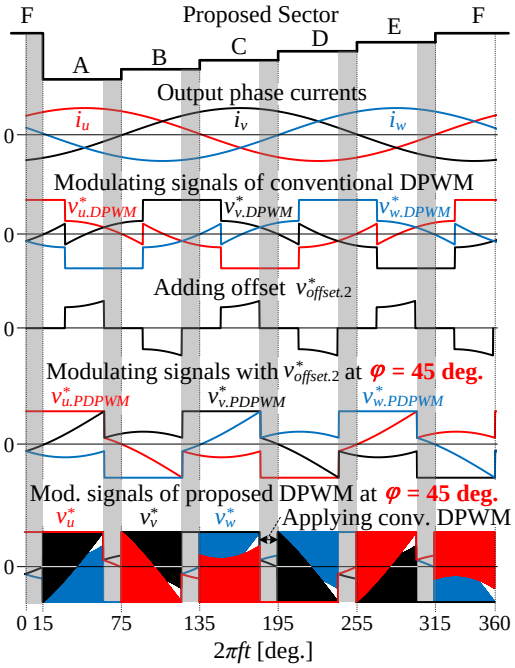
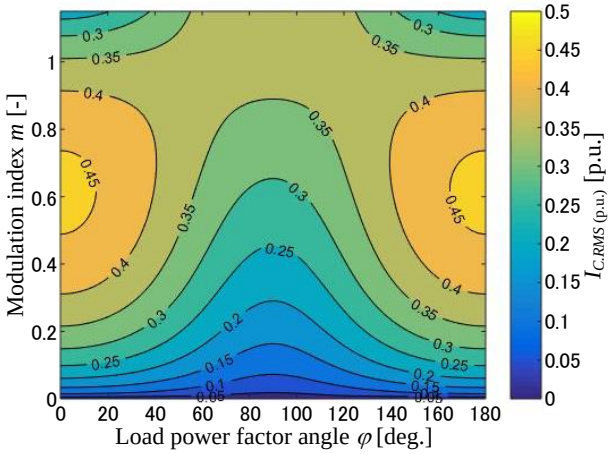
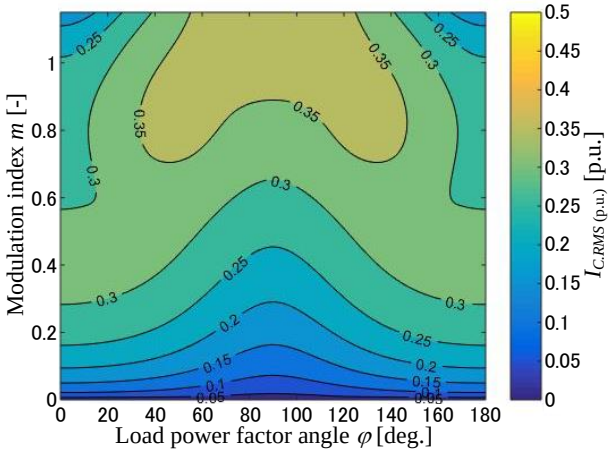


Fig. 6. Proposed modulating signals at m = 0.8 cos φ = 0.707 (45 deg. lagging). In gray-colored periods, the conventional DPWM are applied to avoid the overmodulation operation due to the addition of $v^*_{offset.2}$.



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 7. Analytical results of DC-link capacitor RMS current.

The characteristic to reduce the harmonic components in the DC-link capacitor current is same between driving and regenerative braking modes. In addition, a higher load power factor absolute value |cos φ| leads to a greater reduction effect on the DC-link capacitor RMS current, because the application ratio of the proposed discontinuous modulating signals becomes higher as the |cos φ| is higher. The power factor variation range of the motor loads is dependent on the applications; e.g., the rated speed and rated torque conditions are mainly used in the fan or pump applications, whereas any speed and torque conditions are expected in the traction applications such as train and electric vehicle. Furthermore, the load power factor is also dependent on the motor type such as IM or PMSM. The actual effect on the DC-link capacitor RMS current reduction could be estimated by using this analytical results with the consideration of the expected operating conditions and their occurrence frequencies in each certain application.

3.2 Load Current Quality Since the switching frequency harmonics in the output voltage and output current of VSI have a critical role in the generation of the motor copper losses, the torque ripple of the test motor and the phase current total harmonic distortion (THD), the switching frequency harmonic characteristic of VSI is important to determine the performance of the modulation method. In this paper, the concept of the harmonic flux[20] is used as an evaluation method for the load current quality characterized by the modulation method. This concept does not require the calculation of the harmonic spectrum of the inverter output voltage waveform, which is complicated for the proposed DPWM because of its gate pulse asymmetry in the carrier cycle. Assuming the switching frequency model of the load induction motor as an inductance L, a harmonic load current vector $\mathbf{I_h}$ is proportional to a harmonic flux vector $\boldsymbol{\lambda_h}$, which is the time integral of the instantaneous error voltage vector,

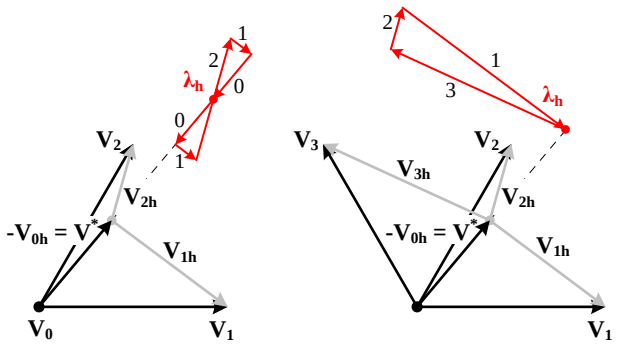
$$\boldsymbol{\lambda}_\mathbf{h} = L\mathbf{I}_\mathbf{h} = \int_{NT_s}^{(N+1)T_s} \left(\mathbf{V}_\mathbf{k} - \mathbf{V}^*\right) dt = \int_{NT_s}^{(N+1)T_s} \mathbf{V}_\mathbf{kh}\, dt \quad \text{..... (10)}$$

where $\mathbf{V_k}$ (k = 0~7) is the output voltage space vector of the 2-level VSI, $\mathbf{V}^*$ is the voltage reference vector, and $\mathbf{V_{kh}}$ is the instantaneous error voltage vector.

Fig. 8 shows the harmonic flux trajectories with the conventional and proposed DPWM at the modulation index of 0.8, and the phase angle of 50 deg., under the same analytical conditions as in Figs. 3 and 4. The calculation of (10) and Fig. 8 visualize and evaluate the ripple current on a per-carrier cycle base. Since the harmonic flux vector characteristic has six-fold space symmetry, the per-fundamental cycle (per 60 deg. in space) harmonic flux RMS value, which characterizes the load current quality and the harmonic losses in the test motor, is calculated as follows:

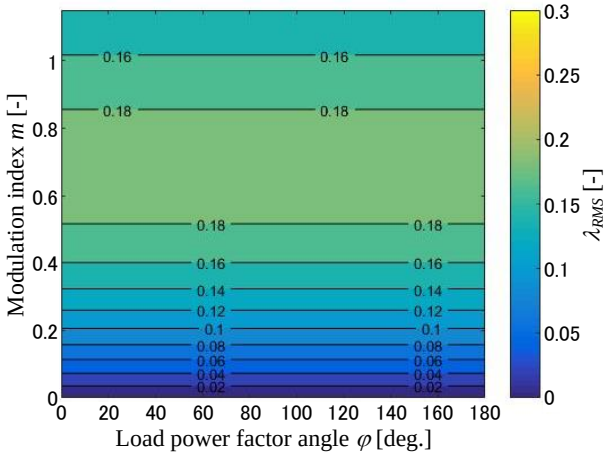
$$\lambda_{RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\int_0^1 \left\|\boldsymbol{\lambda}_\mathbf{h}\right\|^2 dd\,d\theta}. \quad \text{.....(11)}$$

Fig. 9 shows the analytical results of the harmonic flux RMS values with regard to the modulation index and the load power factor angle under the same switching frequency. In case of the conventional DPWM, the modulating signals are only dependent on the modulation index. Therefore, λ_{RMS} obtained with the conventional DPWM is variable by only the modulation index. Nevertheless, in case of the proposed DPWM, the modulating signals are varied to reduce the DC-link capacitor RMS current with regard to m and φ. Furthermore, Figs. 8 and 9 confirm that the proposed DPWM leads to a larger λ_{RMS} compared to the conventional DPWM. Note that the distance between the



(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 8. Harmonic flux trajectories at m = 0.8, $2\pi ft$ = 50 deg under same switching frequency.

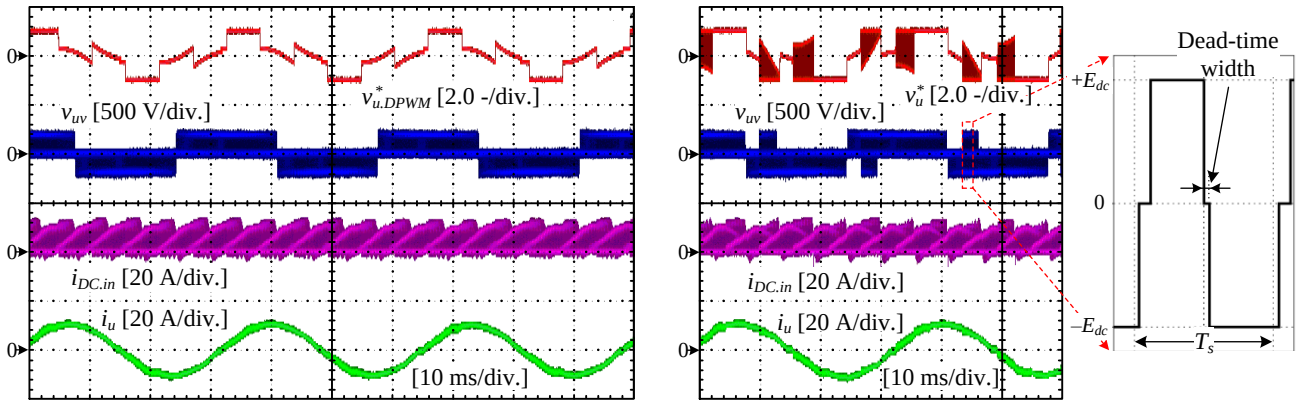


(a) Conventional DPWM.

(b) Proposed DPWM.

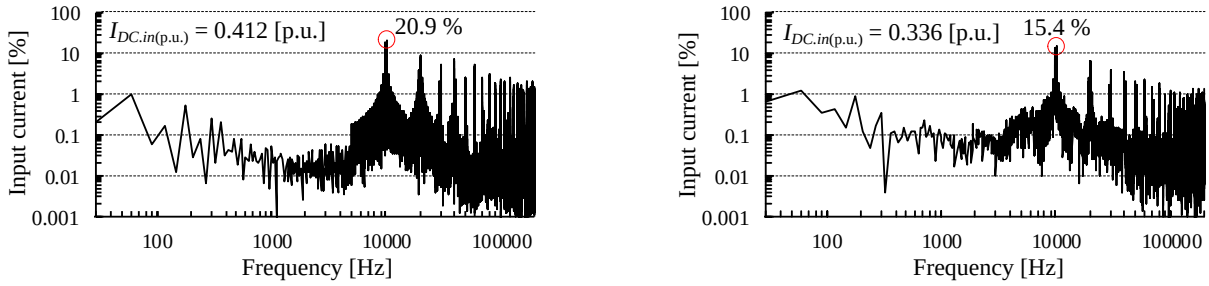
Fig. 9. Comparison of harmonic flux RMS values.

trajectories and the origin, initial value of $\boldsymbol{\lambda_h}$ at the beginning of the carrier cycle, is equal to the magnitude of the harmonic flux[20]. The proposed discontinuous modulating signals result in the application of the voltage space vector which is not the closest to $\mathbf{V}^*$, i.e. $\mathbf{V_3}$ in Fig. 8. On the other hand, only voltage space vectors which are the closest to $\mathbf{V}^*$ are employed in the conventional DPWM. Therefore, the proposed DPWM leads to worse λ_{RMS}. Fig. 9 also confirms that a higher |cos φ| leads to a larger λ_{RMS}, of which characteristics are opposite of the DC-link capacitor RMS current reduction effect shown in Fig. 7.



(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 10. Experimental waveforms at m = 0.705, cos φ = 0.819 (35 deg. lagging), i.e. driving mode; u-phase modulating signal, output line-to-line voltage, DC-link current and output phase current. The zoomed-in waveform of v_{uv} is from the simulation model using PLECS.



(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 11. Harmonic components of DC-link current at m = 0.705, cos φ = 0.819 (35 deg. lagging), i.e. driving mode (under same conditions as in Fig. 10).

4. Simulation and Experimental Results

The performance of the proposed DPWM is verified experimentally. In this experiment, a three-phase induction motor (MVK8115A-R, Fuji Electric Co. Ltd.) of which rated power is 3.7 kW is used as the test motor. The test motor is driven by the three-phase 2-level VSI, composed of IGBT power module (7MBP50RA120, Fuji Electric Co. Ltd.) and operated at the switching frequency of 10 kHz. The VSI is controlled by V/f control with the conventional and proposed DPWM, which are implemented into an evaluation board (TMS320C6713, Texas Instruments). The load power factor is varied by controlling the torque reference of the load motor.

4.1 DC-link Current Harmonics Fig. 10 shows the operating waveforms of VSI with the conventional and proposed DPWM at a modulation index of 0.705, and a load power factor of 0.819 (35 deg. lagging), i.e. driving mode. Under this load power factor condition, the application interval of the proposed DPWM is long; however, the conventional DPWM is also partially applied. Fig. 10 confirms that the width of the step change in the DC-link current is reduced by an application of the proposed DPWM. On the other hand, the larger transitions between $+E_{dc}$ and $-E_{dc}$ seem to occur in the output line-to-line voltage with the proposed DPWM due to the application of the voltage space vector which is not the closest to $\mathbf{V}^*$. However, the zoomed-in waveform of v_{uv} shown in Fig. 10(b) confirms that the instantaneous voltage transition between $+E_{dc}$ and $-E_{dc}$ never occurs due to the dead-time period. Therefore, the proposed DPWM does not increase the motor surge voltage in practice compared to the conventional DPWM.

Fig. 11 shows the harmonic components of the DC-link current under the same conditions as in Fig. 10. Note that 100% of the vertical axis indicates the maximum value of the output phase current. The application of the proposed DPWM reduces the switching frequency component of the DC-link current by 5.49 points.

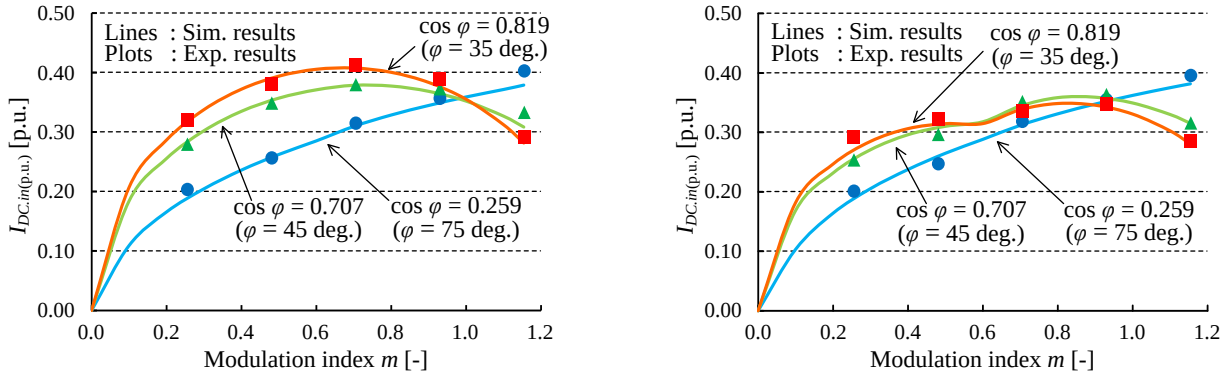
Fig. 12 shows the measured DC-link current harmonics with regard to the modulation index and load power factor in driving mode. The DC-link current harmonics is evaluated as the RMS value of the DC-link current, which is normalized by the maximum value of the output phase current as:

$$I_{DC.in(p.u.)} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(i_{DC.in.RMS.n}\right)^2} \quad \text{.....(12)}$$

where n is the harmonic order and $i_{DC.in.RMS.n}$ is the RMS value of the n-order DC-link current harmonics component. The harmonic components of the DC-link current up to 20th-order of the switching frequency are considered in this evaluation. Fig. 12 confirms that the DC-link current harmonics is reduced under any modulation index and load power factor conditions. In addition, it is also confirmed that higher load power factor leads to a greater DC-link current harmonics-reduction effect with the proposed DPWM.

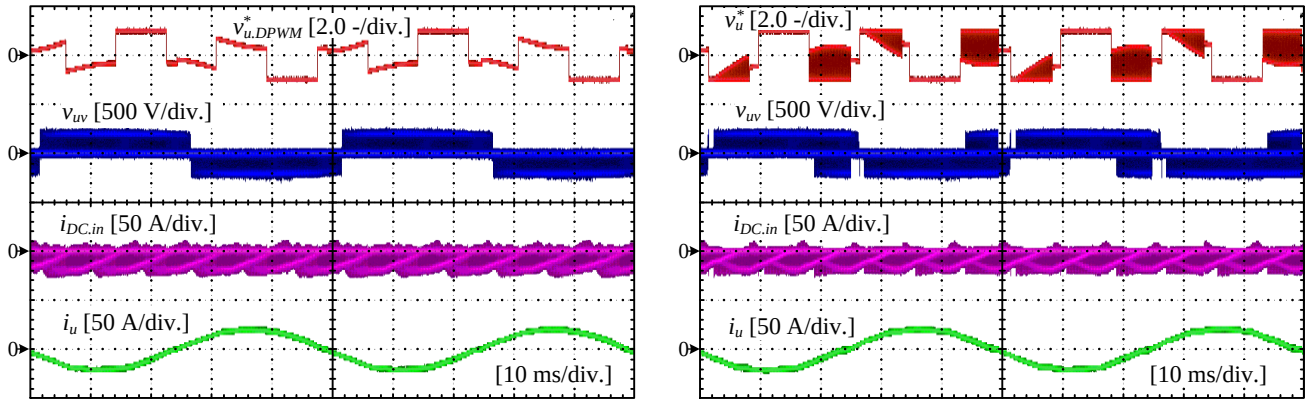
Fig. 13 shows the operating waveforms of VSI at the modulation index of 0.445, and the load power factor of –0.766 (140 deg. lagging), i.e. regenerative braking mode. Even in regenerative braking mode, the width of the step change in the DC-link current can be reduced by the proposed DPWM, resulting in a reduced DC-link current harmonics.

Fig. 14 shows the harmonic components of the DC-link current under the same conditions as in Fig. 13. When the conventional DPWM is applied, the switching frequency component is 17.9%



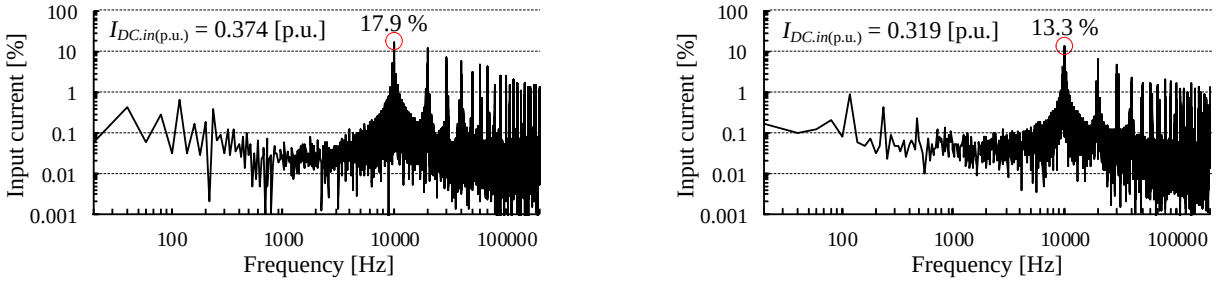
(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 12. Measured DC-link current harmonics in driving mode.



(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 13. Experimental waveforms at m = 0.445, cos φ = –0.766 (140 deg. lagging), i.e. regenerative braking mode; u-phase modulating signal, output line-to-line voltage, DC-link current and output phase current.



(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 14. Harmonic components of DC-link current at m = 0.445, cos φ = –0.766 (140 deg. lagging), i.e. regenerative braking mode (under same conditions as in Fig. 13).

and the DC-link current harmonics is 0.374 p.u. The application of the proposed DPWM reduces the switching frequency component by 4.6 points, and the DC-link current harmonics by 0.319 p.u. The experimental results in Figs. 10–14 confirm that the proposed DPWM is effective to reduce the DC-link current harmonics for the motor drive system, of which the variation of the load power factor is considerably wide.

4.2 Output Phase Current Harmonics Fig. 15 shows THD of the output u-phase current at the load power factor of 0.866. Up to 40th-order harmonic components of the phase current are considered in this evaluation. Even though the analytic criterion of λ_{RMS}, explained in sub-section 3.2, and current THD are different, both of them are used to evaluate the output current quality. Fig. 15 confirms the analytical results shown in Fig. 9 except for the high-modulation index area; in other words, the measured THD of the output phase current obtained with the proposed DPWM is higher than those obtained with the conventional DPWM. One of the reasons for the increase of the current THD with the proposed DPWM is the current detection error around zero-current-crossing points. These errors cause the incorrect selection of the current sector (A–F), listed in Table 1, and increase the output phase current distortion, especially around the output phase current zero-crossing. This worse output phase current distortion might cause an increase of the iron loss in the load motor.

4.3 Inverter Efficiency Fig. 16 shows the inverter efficiency comparison between the conventional and proposed DPWM at the load power factor of 0.866. The inverter efficiency is measured using Yokogawa WT1800 power analyzer. The

application of the proposed DPWM slightly improves the inverter efficiency. In terms of the number of switching transitions, those number are same between the conventional and proposed DPWM, which can be observed from Figs. 3–4. In addition, the proposed DPWM always clamps the phase whose flowed current's absolute value is the maximum among three-phase currents due to the adaption process to the load power factor range, which can be observed from Fig. 5. In other words, the proposed DPWM enables to avoid the larger current chopping, leading to the smaller switching loss compared to those with the conventional DPWM under conditions where the load power factor is not unity.

4.4 Common-mode Voltage Figs. 17–18 show the simulation results for VSI operating waveforms and the harmonic components of the common-mode voltage at the modulation index of 0.705 and the load power factor of 0.819 (under the same conditions as in experimental conditions in Figs 10–11). The common-mode voltage (v_{no}) is defined as the potential difference between the star point of the motor load (n) and the center of the dc-bus (o), which can be calculated as following.

$$v_{no} = \frac{v_{uo} + v_{vo} + v_{wo}}{3}. \quad \text{..... (13)}$$

According to (13), the biggest v_{no} transition occurs when the both switching states of the zero vector ($\mathbf{V_0}$ (0 0 0) and $\mathbf{V_7}$ (1 1 1)) are applied during control period. However, the proposed DPWM uses only one zero vector at a maximum during control period, which is the same as the conventional DPWM. Therefore, the proposed DPWM does not increase the v_{no} transition width. Spectrum of v_{no} shown in Fig. 18 confirm that the proposed DPWM reduces the switching frequency component by 16.5 points; however, increases the high-frequency components (higher than 100 kHz) compared to the conventional DPWM. This worse high-frequency v_{no} component might result in high common-mode current (motor leakage current). This may lead to the motor bearing failures, EMI noise and so on[21]–[22].

5. Electrolytic Capacitor Lifetime Comparison

Expected lifetime of the electrolytic capacitor is calculated as the multiplication of the specified lifetime L_o in the manufacturer datasheet by three acceleration rates which are dependent on the ambient temperature F_T, the ripple current F_I, and the applied voltage F_V[13]. In this section, only the acceleration rate related to the ripple current F_I is considered, and the other two factors F_T and F_V are assumed as 1.

Table 2 lists the frequency coefficient K_f of the rated ripple current flowing through the electrolytic capacitor (RWF series,

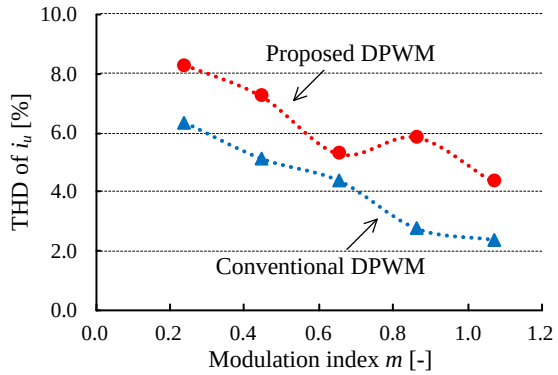


Fig. 15. THD of output u-phase current i_u at cos φ = 0.866.

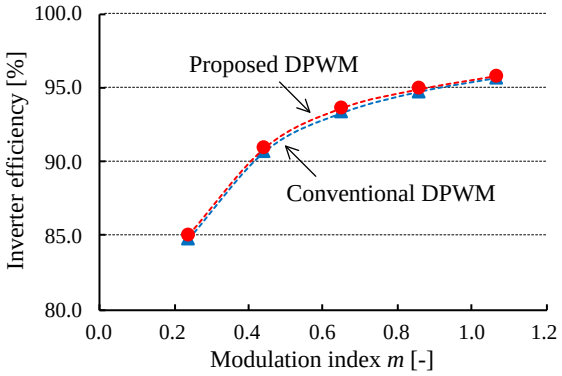
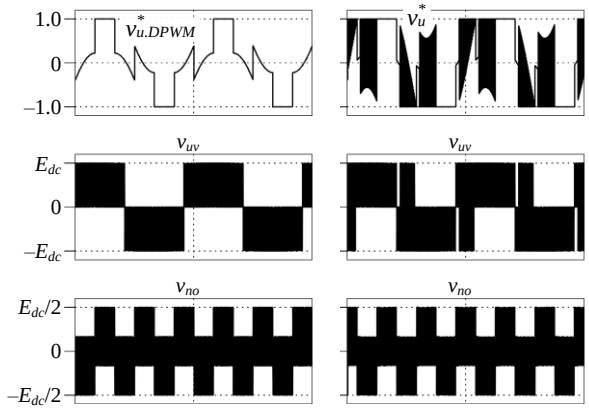
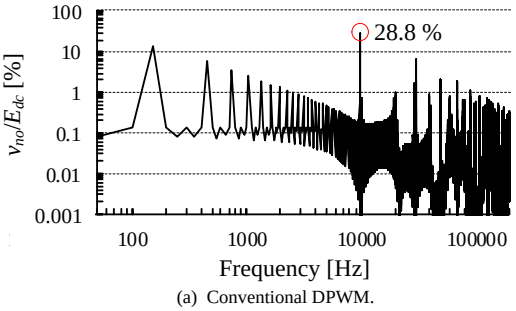


Fig. 16. Inverter efficiency comparison between conventional DPWM and proposed DPWM at cos φ = 0.866.

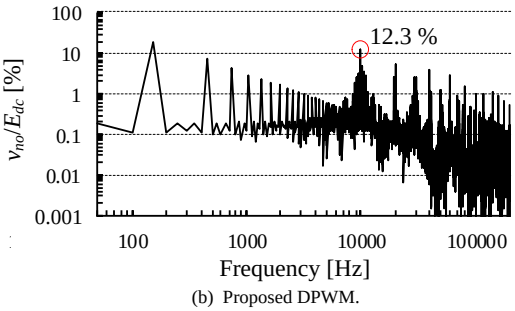


(a) Conventional DPWM. (b) Proposed DPWM.

Fig. 17. Simulation results of common-mode voltage at m = 0.705, cos φ = 0.819 under same conditions as in Figs. 10–11. This waveforms are from simulation model using PLECS.



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 18. Harmonic components of common-mode voltage at m = 0.705, cos φ = 0.819 (under same conditions as in Figs. 10–11, 17).

Nippon Chemi-Con Corp.[23]), which has been used in the laboratory setup. With the consideration for the frequency dependency of the ESR in the electrolytic capacitors, the DC-link current harmonics is recalculated for its lifetime estimation as:

$$I_{DC.in.freq(\mathrm{p.u.})} = \frac{1}{I_m}\sqrt{\sum_{n=1}\left(\frac{i_{DC.in.RMS.n}}{K_f}\right)^2} \quad \text{..... (14)}$$

Fig. 19 shows the harmonic components of the DC-link current at the modulation index of 0.705, and the load power factor of 0.819 (under the same conditions as in Figs. 10–11) with the consideration for the frequency dependency of the ESR in the electrolytic capacitors. The application of the proposed DPWM reduces $I_{DC.in.freq(\mathrm{p.u.})}$ by 18.3% even when the frequency dependency of ESR in the electrolytic capacitor is considered. Note that it is necessary to consider the expected operation range for exact estimation of the capacitor lifetime. However, the actual operation range in motor speed and torque plane is dependent on each applications; therefore, full consideration with those is difficult. Therefore, simplified estimation is provided in this section with the assumption that this operating conditions (at modulation index of around 0.7 and load power factor of around 0.8) are the medium-speed and medium-torque conditions in the variable-speed drive systems, which are the frequent operating conditions. Assuming that the electrolytic capacitors in the VSI, modulated by the conventional DPWM, is designed at the worst case of the rated ripple current as $F_I = 1$, the estimated lifetime L_n of the electrolytic capacitor can be given by:

$$\begin{aligned} L_{n\_Conv.DPWM} &= L_o \cdot F_I = L_o \cdot 1 = 5\,000 \text{ h} \\ L_{n\_Prop.DPWM} &= L_o \cdot F_I = L_o \cdot 1.26 = 6\,300 \text{ h} \end{aligned} \quad \text{..... (15)}$$

where L_o is 5 000 hours in case of RWF series, Nippon Chemi-Con Corp. The ripple current factor F_I is calculated by using the results in Fig. 19 based on the technical notes on electrolytic capacitors[13].

Note that the above lifetime estimation is just one example. However, it can be concluded that the application of the proposed DPWM might extend the lifetime of the electrolytic capacitor about 1.26 times longer than that with the conventional DPWM.

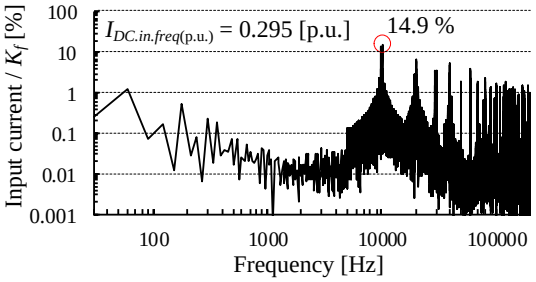
6. Conclusion

A novel DPWM was proposed to reduce the DC-link current harmonics of the three-phase VSI, which flowed through the DC-link capacitor, over the wide variation of the load power factor. This modulation method contributed the long lifetime of the smoothing capacitor in the motor drive system. Furthermore, this strategy required only one carrier; thus, high cost hardware such as FPGA was unnecessary. The DC-link current harmonics were reduced by shifting two unclamped modulating signals in every half control period. In addition, the injection of the zero sequence signal to all discontinuous modulating signals optimized the phase of clamped modulating signal and its clamped value according to the conditions of the output phase currents; consequently, the DC-link current harmonics were reduced even when the load power factor varied.

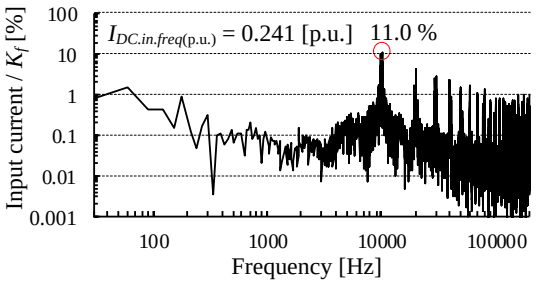
The experimental results confirmed that the application of the proposed DPWM reduced the RMS value of the DC-link current by 18.3% with the consideration for the frequency dependency of the ESR of the electrolytic capacitor. The lifetime estimation results confirmed that the DC-link RMS current reduction of 18.3% could lead to the lifetime extension of 1.26 times for the electrolytic capacitor. Furthermore, the application of the proposed DPWM reduced the DC-link current harmonics over entire range of the load power factor, i.e. in both driving mode and regenerative braking mode.

Table 2. Frequency coefficient of rated ripple current flowing through electrolytic capacitors (RWF series, Nippon Chemi-Con Corp.)

Frequency [Hz]	50	120	300	1 k	3 k~
Coefficient K_f	0.80	1.0	1.1	1.3	1.4



(a) Conventional DPWM.



(b) Proposed DPWM.

Fig. 19. Harmonic components of DC-link current at $m = 0.705$, $\cos\varphi = 0.819$ (under same conditions as in Figs. 10–11) with consideration for frequency dependency of ESR in electrolytic capacitors.

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