電気学会論文誌●（●●●●●●●部門誌）
IEEJ Transactions on ●●●●●●●●●●●●●●●●
Vol.●● No.● pp.●-●● DOI: ●.●●/ieejeiss.●●.●

Paper

Input Current Harmonic Reduction based on Space Vector PWM for Three-level Inverter Operating over a Wide Range Power Factor

Koroku Nishizawa*, Student member, Jun-ichi Itoh*a), Senior member
Akihiro Odaka**, Member, Akio Toba**, Senior member, Hidetoshi Umida**, Fellow

(Manuscript received Jan. 00, 20XX, revised May 00, 20XX)

This paper proposes a space vector pulse width modulation (SVPWM) that reduces current harmonics flowing through DC-link capacitors of a three-level voltage source inverter in a three-phase motor drive system. The inverter input current harmonics are minimized by optimizing the applied voltage space vectors to reduce the fluctuation of the inverter input current around its average value. Furthermore, the proposed strategy can be used for a wide range of load power factors by changing the combination of voltage space vectors according to output phase current conditions. It is experimentally shown that the proposed SVPWM reduces the inverter input current harmonics by 27.4% at most, compared with that of the conventional SVPWM. Moreover, the analytical and experimental results clarify that the proposed SVPWM reduces the inverter input current harmonics at any load power factor.

Keywords : Three-level voltage source inverter, Space vector PWM, Input current harmonics

1. Introduction

Neutral-point-clamped (NPC) three-level voltage source inverters (3LVSIs) [1] have been applied to medium-voltage high-power AC motor drive application such as traction drive system for railway transportation due to their high-voltage high-power capacity [2].

AC-electrified railway systems such as Shinkansen bullet train system are generally composed of traction transformers, single-phase NPC rectifier, three-phase NPC-3LVSI, and induction motors [3]. In the DC-link part of this system, two filter capacitors with the high-voltage capacity are implemented in series to decouple the unbalance between the instantaneous input and output power. Heretofore, oil-filled capacitors have been generally used as filter capacitors; however, these oil-filled capacitors require a periodic maintenance due to theirs low resistance for moisture and heat shock. Consequently, the oil-filled capacitors have been replaced by the film capacitors recently [4]. Nevertheless, the film capacitors may degrade or damage themselves with the self-heating due to the capacitor ripple current [5]. The inverter input current contains numerous high-order switching-frequency harmonics because the current is a superposition summation of the switched current pulses from each phase leg of 3LVSI [6][7]. Therefore, it is necessary to reduce NPC-3LVSI input current harmonics.

So far, the modulation method to reduce the leakage current of 3LVSIs for PV systems by reducing the neutral-point voltage ripple has been proposed [8]. This modulation method also reduces the capacitor current ripple; however, the capacitor current ripple is not to be suppressed to the minimum. In addition, this modulation method is effective in reducing the capacitor current ripple only when the load power factor is around unity. Thus, it is not applicable to the 3LVSIs in motor drive systems, of which the variation of the load power factor is considerably wide.

In this paper, a novel space vector PWM (SVPWM) is proposed to reduce the switching-frequency-order NPC-3LVSI input current harmonics under any load power factor condition, i.e., both driving and regenerative braking modes. The voltage vectors of 3LVSI are optimally selected to minimize a fluctuation of the inverter input current around its average value. Furthermore, the voltage vector selection is based on the detected output phase current directions for an adaptation to variations of the load power factor without a load power factor detection. The analytical calculations ensure that the employment of voltage vectors in this proposed SVPWM reduce the inverter input current harmonics at any modulation indices and load power factor. The original contribution of this strategy is the reduction of the 3LVSI input current harmonics over entire region of the load power factor, which is the crucial problem with past works.

This paper is organized as follows; firstly, the configuration of NPC-3LVSI are explained. Secondly, the analytical results on the 3LVSI input current are presented. Next, the reduction method of the 3LVSI input current by changing the combinations of the voltage space vectors are proposed. Finally, the modulator performances on the input current harmonics, output current harmonics, inverter efficiency, and common-mode voltage are compared between the conventional and proposed SVPWM.

2. Three-level Inverter Input Current Harmonics

2.1 Configurations of Three-level Inverter Fig. 1 shows the configuration of NPC-3LVSI. The NPC inverter leads to low switching losses since two series-connected devices splits the arm blocking voltage. However, it has high conduction losses because there are two devices in the current path regardless of the output voltage level. Therefore, the NPC inverter becomes efficient in the medium-voltage and high-frequency applications [9].

a) Correspondence to: Jun-ichi Itoh.
E-mail: itoh@vos.nagaokaut.ac.jp
* Nagaoka University of Technology.
1603-1, Kamitomioka-machi, Nagaoka, Niigata, Japan 940-2188
** Fuji Electric Co., Ltd.
1, Fuji-machi, Hino, Tokyo, Japan 191-8502

Table 1 lists the relationships between the switching functions and the phase voltage of the NPC inverter. The switching function is defined as:

$$s_{xj} = \begin{cases} 1 & (\mathrm{S}_{xj}:\mathrm{ON}) \\ 0 & (\mathrm{S}_{xj}:\mathrm{OFF}) \end{cases}, \quad (x = u \sim w,\ j = 1 \sim 4) \quad \text{..... (1)}$$

where x is the output phase and j is the number of device defined in Fig. 1. There are three switching states in each leg of the 3LVSI, and the three-level phase voltages are available.

2.2 Conventional Three-level Space Vector PWM

Fig. 2 shows the output voltage space vectors of 3LVSI in the $\alpha\beta$ reference frame. These voltage space vectors are illustrated on the basis of the *Clarke transform* of 3LVSI three-phase output voltages. The switching functions of each phase results in three different values; therefore, there are $3^3 = 27$ switching states in the 3LVSIs. On the other hand, there are nineteen voltage space vectors ($\mathbf{V_0}$–$\mathbf{V_{18}}$) in total due to the switching state redundancy.

Fig. 3 shows the principle of the conventional three-level SVPWM at sector I. Each sector of the conventional three-level SVPWM is regarded as the space vector diagram of the two-level SVPWM. Therefore, the classic two-level SVPWM is applicable in each sector of the three-level SVPWM with an inner voltage reference vector $\mathbf{V^*_{in}}$. The inner vector is obtained by decomposing the voltage reference vector $\mathbf{V}^*$ by the equivalent zero vector of the two-level SVPWM in each sector (e.g., $\mathbf{V_7}$ in the sector I) as:

$$\mathbf{V^*_{in}} = \mathbf{V}^* - \mathbf{V_{6+i}} = \left|\mathbf{V}^* - \mathbf{V_{6+i}}\right| \angle\gamma \quad \text{..... (2)}$$

where γ is the phase angle of the inner voltage reference vector $\mathbf{V^*_{in}}$ and i is the number of sector where the voltage reference vector $\mathbf{V}^*$ exists. The sector I area is also divided into six sub-sectors 1–6 in the same manner as the two-level SVPWM. Then, the three voltage space vectors surrounding the sub sector where the inner vector exists are selected. The inner voltage reference vector sampled in each control period T_s is generated by synthesizing the three voltage space vectors on the volt-second balance principle as [10]:

$$\mathbf{V^*_{in}} = \frac{t_a}{T_s}\mathbf{V_x} + \frac{t_b}{T_s}\mathbf{V_y} + \frac{t_c}{T_s}\mathbf{V_z} \quad \text{..... (3)}$$
$$T_s = t_a + t_b + t_c$$

where t_a–t_c are the duty cycles of each selected voltage space vector, and a–c represent the number of selected voltage space vectors, defined in Fig. 2.

2.3 Instantaneous RMS value of 3LVSI Input Current

Fig. 4 shows the waveforms of the voltage references and the output phase currents at unity load power factor. The output phase currents of 3LVSI are expressed as:

$$\begin{cases} i_u = I_m \cos(2\pi ft - \varphi) \\ i_v = I_m \cos(2\pi ft - 2\pi/3 - \varphi) \\ i_w = I_m \cos(2\pi ft + 2\pi/3 - \varphi) \end{cases} \quad \text{..... (4)}$$

where I_m is the maximum value of the output phase current, f is the fundamental frequency, and φ is the load power factor lagging angle, respectively.

Fig. 5 shows the zoomed-in waveforms of the 3LVSI input current when the conventional SVPWM is applied. The voltage reference vector $\mathbf{V}^*$ is sampled at sub-sector 1 in the sector I as shown in Fig. 3. The instantaneous values of the P-side and N-side input current of the both T-type and NPC 3LVSIs are the superposition summation of the switched current pulses from each phase leg and calculated as:

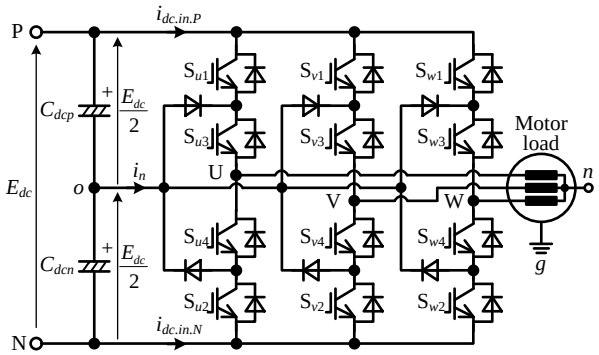


Fig. 1. Configuration of NPC-3LVSI.

Table 1. Switching states of NPC inverter.

Switching state	v_{xo} [V]	Switching functions (x = u, v, w)			
		s_{x1}	s_{x2}	s_{x3}	s_{x4}
P (+)	$+E_{dc}/2$	1	0	1	0
0	0	0	0	1	1
N (–)	$-E_{dc}/2$	0	1	0	1

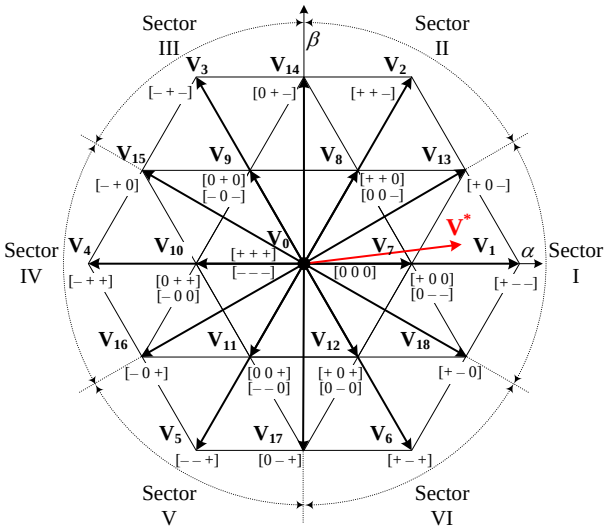


Fig. 2. Output voltage space vectors of 3LVSI in $\alpha\beta$ reference frame.

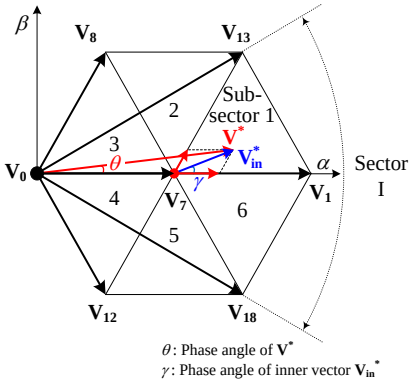


Fig. 3. Conventional three-level SVPWM strategy at sector I.

$$i_{DC.in.P} = \sum_{x=u,v,w} \left(s_{x1} \times i_x\right),$$
$$i_{DC.in.N} = \sum_{x=u,v,w} \left(s_{x2} \times i_x\right). \quad \text{..... (5)}$$

Although this paper focuses on NPC-3LVSI, note that the relationships between 3LVSIs input currents and those switching states are same for both T-type and NPC. Thus, the proposed modulation strategy, explained from following section, is also effective in reducing the capacitor current in the T-type 3LVSI.

In order to analyze the optimized combination of the voltage space vectors for the minimum RMS value of the 3LVSI input current, the RMS value of the 3LVSI input current in the N cycle of the carrier period, defined as the instantaneous RMS value [11], is introduced.

$$i_{DC.in.RMS}\left(T_s\right) = \sqrt{\frac{1}{2T_s}\int_{NT_s}^{(N+1)T_s}\left(i_{DC.in.P}^2 + i_{DC.in.N}^2\right)dt}$$
$$= \sqrt{\sum_{k=a,b,c}\frac{t_k}{2T_s}\left(i_{DC.in.P,k}^2 + i_{DC.in.N,k}^2\right)}. \quad \text{..... (6)}$$

where t_k is the duty cycle of the selected voltage space vector, $i_{DC.in.P,k}$ and $i_{DC.in.N,k}$ are the instantaneous values of the P-side and N-side input current when the selected voltage space vector $\mathbf{V_k}$ is applied.

2.4 Average value of 3LVSI Input Current The average value of the 3LVSI input current over the fundamental period is calculated as:

$$i_{DC.in.ave} = \frac{1}{2\pi}\int_0^{2\pi}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}i_{DC.in.P,k}\right)d\theta$$
$$= \frac{3}{4}m \cdot I_m \cos\varphi. \quad \text{..... (7)}$$

Note that the average value of the input current over the fundamental period is not dependent on the choice of the voltage space vectors, but the modulation index, load current, and load power factor.

2.5 Instantaneous RMS value of DC-link Capacitor Current The instantaneous RMS value of the current flowing into the DC-link capacitors is derived by the difference between the instantaneous RMS value of the 3LVSI input current (6) and the average value over the fundamental period (7) as follows:

$$i_{C.RMS}\left(T_s\right) = \sqrt{i_{DC.in.RMS}^2\left(T_s\right) - i_{DC.in.ave}^2}. \quad \text{..... (8)}$$

Since only the instantaneous RMS value of the 3LVSI input current is dependent on the choice of the voltage space vectors, the instantaneous RMS value of the DC-link capacitor current is also dependent these choices. Thus, the lifetime of the DC-link capacitors, which is affected by the instantaneous RMS value of the DC-link capacitor current (8), is extended by the selection of the voltage space vectors that minimize the instantaneous RMS value of 3LVSI input current (6).

Note that a small difference between the instantaneous values of $i_{DC.in.P}$ and $i_{DC.in.N}$, and these average values of the 3LVSI input current $i_{DC.in.ave}$ results in a small instantaneous RMS value of 3LVSI input current [12]. These fluctuations of $i_{DC.in.P}$ and $i_{DC.in.N}$ are expressed as the shaded areas in Fig. 5. When the conventional three-level SVPWM is applied, the equivalent zero vectors $\mathbf{V_7}$, of which switching states are [+ 0 0] and [0 – –], are equally used during each control period in the sector I. In particular, when the equivalent zero vector $\mathbf{V_7}$ [0 – –] is applied, the instantaneous value

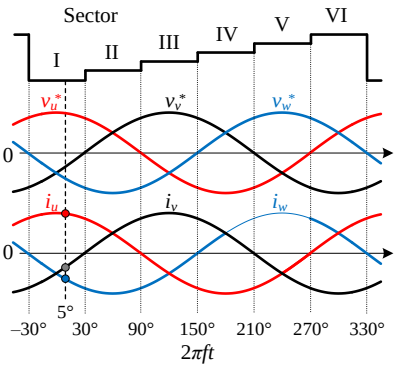


Fig. 4. Waveforms of voltage references and output phase current at unity load power factor. Sector I-VI are determined by the phase angle.

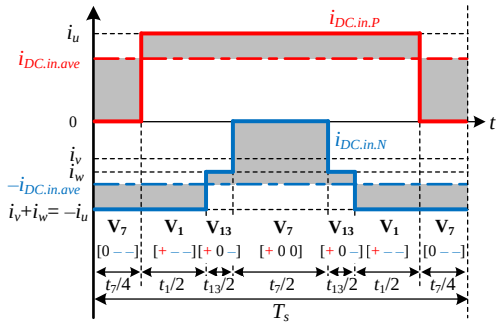


Fig. 5. Zoomed-in waveforms of 3LVSI input current at m = 1.0, $2\pi ft$ = 5°, and cos φ = 1.0 with conventional three-level SVPWM. The voltage reference vector $\mathbf{V}^*$ is located at sub-sector 1 in sector I as shown in Fig. 3.

of the P-side input current $i_{DC.in.P}$ becomes zero, which leads to the large P-side input current $i_{DC.in.P}$ fluctuation around its average value. Another equivalent zero vector $\mathbf{V_7}$ [+ 0 0] worsens the N-side input current $i_{DC.in.N}$ fluctuation around its average value in the same manner.

3. Reduction of 3LVSI Input Current Harmonics

3.1 Combinations of Voltage Space Vectors for Minimum RMS value of 3LVSI Input Current Fig. 6 shows an example of optimized combination of the voltage space vectors to minimize the RMS value of the 3LVSI input current at high-modulation indices, and when the phase currents i_u is positive, and i_v and i_w are negative. The fluctuations of $i_{DC.in.P}$ and $i_{DC.in.N}$ around its average value expressed as the shaded area in Fig. 6(b) become smaller with the selection of the voltage space vectors $\mathbf{V_6}$, $\mathbf{V_{18}}$, $\mathbf{V_{13}}$ than those of the conventional three-level SVPWM shown in Fig. 5, resulting in the minimization of the RMS value of the 3LVSI input current. Note that there are errors between the average value of 3LVSI input current over the fundamental period ($i_{DC.in.ave}$) and the average values over the control period. This is because the average value of the 3LVSI input current over the control period fluctuates at three-fold fundamental frequency due to the dc-bus neutral point potential variation. In order to optimize the combination of the voltage space vectors for the minimum RMS value of the 3LVSI input current, first, the instantaneous values of the 3LVSI input current with all possible voltage space vectors are calculated off-line based on (5). Next, the three voltage space vectors, which make the instantaneous values become close to the average value of the 3LVSI, are selected. Note that the triangle

formed by the tips of these selected three voltage space vectors must contain the tip of the voltage reference vector. These off-line calculations and selections result in the voltage vectors for the minimum RMS value of the 3LVSI input current at unity load power factor are $\mathbf{V_2}$, $\mathbf{V_{13}}$, $\mathbf{V_1}$, $\mathbf{V_{18}}$, and $\mathbf{V_6}$ in the high-modulation index region shown as the green area in Fig. 6(a). On the other hand, the voltage vectors in the low-modulation index region shown as the purple area in Fig. 6(a) at unity load power factor are $\mathbf{V_2}$, $\mathbf{V_8}$, $\mathbf{V_0}$, $\mathbf{V_{12}}$, and $\mathbf{V_6}$[13]. In other words, there are some optimized combinations of the voltage space vectors for the minimum RMS value of the 3LVSI input current. In the proposed three-level SVPWM, the final combination of the applied voltage space vectors is selected from these optimized combinations for the minimum RMS value of the 3LVSI input current, considering the 3LVSI output current quality.

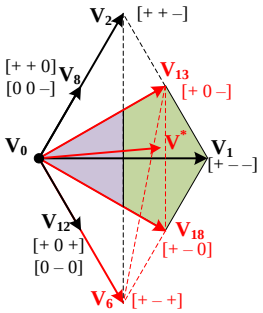
3.2 Load Current Quality Consideration

In order to evaluate the 3LVSI output current quality, the concept of a harmonic flux [14] is used as an evaluation function of the load current quality characterized by the modulation method because this concept does not require the calculation of the output voltage harmonic spectrum, which is difficult to obtain for the proposed SVPWM due to its complicated selection of the voltage space vectors. If the switching frequency model of the load motor is assumed as a pure inductance L, the harmonic load current vector $\mathbf{I_h}$ is a proportional to the harmonic flux vector $\boldsymbol{\lambda_h}$ (time integral of the instantaneous voltage error vector) in the N^{th} carrier cycle, as:

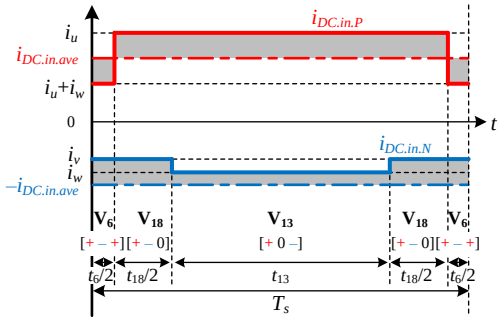
$$\boldsymbol{\lambda}_{\mathbf{h}} = L\mathbf{I}_{\mathbf{h}} = \int_{NT_s}^{(N+1)T_s} \left(\mathbf{V}_{\mathbf{k}} - \mathbf{V}^*\right) dt \quad \cdots\cdots (9)$$

where $\mathbf{V_k}$ (k = 0–18) is the applied voltage space vector.

Fig. 7 shows the harmonic flux trajectories of all vector patterns to achieve the minimum RMS value of the 3LVSI input current at

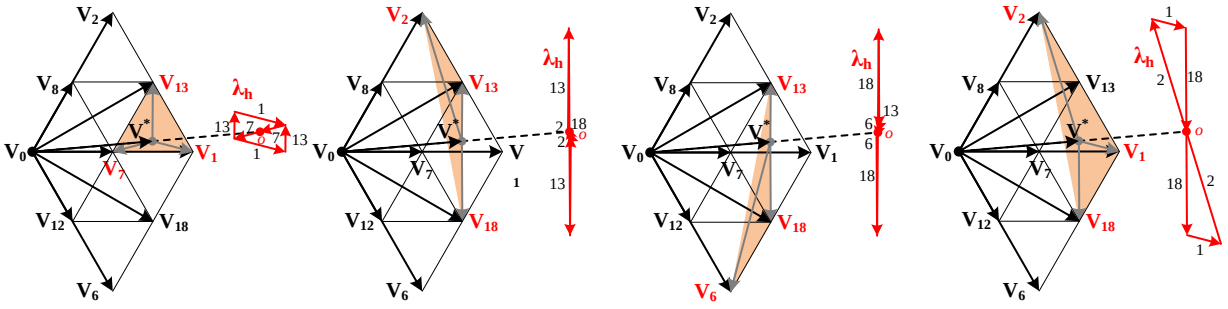


(a) Combination of voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_{13}}$).

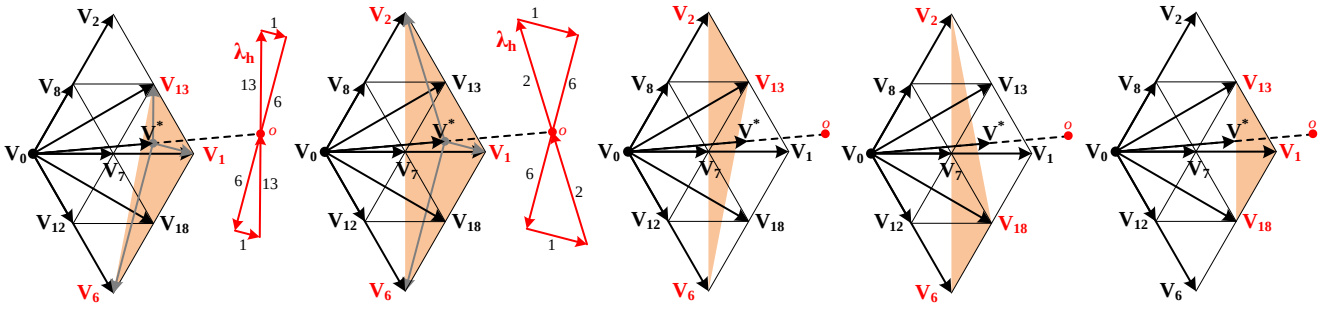


(b) Instantaneous waveform of 3LVSI input current.

Fig. 6. One example of optimized combination of voltage space vectors ($\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_{13}}$) for minimum RMS value of 3LVSI input current at m = 1.0, $2\pi ft$ = 5°, cos φ = 1.0, and when i_u is positive, i_v and i_w are negative.



(a) Conventional 3-level SVPWM. (b) $\mathbf{V_2}$–$\mathbf{V_{13}}$–$\mathbf{V_{18}}$. (c) $\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_{13}}$. (d) $\mathbf{V_{18}}$–$\mathbf{V_1}$–$\mathbf{V_2}$.



(e) $\mathbf{V_{13}}$–$\mathbf{V_1}$–$\mathbf{V_6}$. (f) $\mathbf{V_2}$–$\mathbf{V_1}$–$\mathbf{V_6}$. (g) $\mathbf{V_2}$–$\mathbf{V_{13}}$–$\mathbf{V_6}$. (h) $\mathbf{V_6}$–$\mathbf{V_{18}}$–$\mathbf{V_2}$. (i) $\mathbf{V_{13}}$–$\mathbf{V_1}$–$\mathbf{V_{18}}$.

Fig. 7. Harmonic flux trajectories of all vector patterns to achieve minimum RMS value of 3LVSI input current at m = 1.0, and $2\pi ft$ = 5°. The trajectories are expressed as the red lines. The distance between the origin (o) and the trajectory is equal to the magnitude of the harmonic flux, and continuously fluctuates. Figs. 7(b)–(i) are with the optimized combinations of the voltage space vectors for the minimum RMS value of the 3LVSI input current in the high-modulation indices region. With the combinations of the voltage space vectors shown in (g)–(i), the voltage reference vector is not to be generated under these conditions of the modulation index and the phase angle.

the modulation index of 1.0, and the phase angle of 5°. Within the carrier cycle the trajectories are drawn according to the selected switching sequence. In Fig. 7(a) as an example, two triangles are formed as the harmonic flux trajectory according to the selected switching sequence (**V7–V1–V13–V7–V7–V13–V1–V7**). Since the distance between the origin and the trajectory is equal to the magnitude of the harmonic flux [14], Fig. 7 demonstrates that the optimized vector combinations for the minimum RMS value of 3LVSI input current worsen the load current quality compared to those with the conventional three-level SVPWM. The RMS value of the harmonic flux over each control period is calculated as:

$$\lambda_{RMS(T_s)} = \sqrt{\int_{T_s}^{(N+1)T_s} \left\| \boldsymbol{\lambda}_{\mathbf{h}} \right\|^2 dt}. \quad \text{..... (10)}$$

Fig. 8 shows the phase angle dependencies of the RMS value of the harmonic flux over each control period (10) at the modulation index of 1.0. Fig. 8 demonstrates that the optimized vector combinations for the minimum RMS value of 3LVSI input current worsen the values of $\lambda_{RMS(Ts)}$ with regard to any phase angle compared to the conventional 3-level SVPWM. However, it is also demonstrated that the optimized combinations of voltage space vectors **V2–V13–V18**, **V6–V18–V13**, **V2–V13–V6**, and **V6–V18–V2** suppress the increase of the harmonic flux at the modulation index of 1.0. For example, **V2–V13–V6** combination leads to the smallest increase of $\lambda_{RMS(Ts)}$ in the phase range of 18°–30° as observed in Fig. 8. Note that $\lambda_{RMS(Ts)}$ value has both the phase angle dependency and the modulation index dependency. So, the proposed 3-level SVPWM vector patterns are determined by selecting the combination to achieve the smallest value of $\lambda_{RMS(Ts)}$ from the optimized vector combinations for the minimum RMS value of 3LVSI input current with respect to the phase angle and the modulation index. Note that the selection for the final combination of the applied voltage space vectors is also performed off-line and any on-line calculations of (9) or (10) are not necessary.

Fig. 9 shows the proposed vector patterns to minimize the RMS value of the 3LVSI input current when the phase currents i_u is positive, and i_v and i_w are negative with the consideration of the load current quality.

Fig. 10 shows the flowchart for determining the detailed area i-x in Fig. 9 and applied voltage space vectors. First, the duty cycles corresponding to the applied voltage space vectors, listed in Fig. 9, are calculated. Next, those calculated duty cycles are verified whether those are realistic values or not. If there is only one realistic case, it is identified as the area where the voltage reference vector $\mathbf{V}^*$ locates. If not, the phase angle (γ) of the inner voltage reference vector determines the correct area. For example, duty cycles are realistic values both in the parts of area ii and iii in Fig. 9. In this case, area ii and iii are identified whether γ exceeds 180° or not. Note that this area identification process is just one example. In practical use, the detailed area i-x is identified using look-up tables, avoiding the heavy on-line computation load.

3.3 DC-bus Neutral Point Potential of 3LVSI The neutral current flowing out or into the neutral point of the DC-link causes the variation of the dc-bus neutral point potential. Its current is related to the common-mode voltage of 3LVSI and calculated from the switching functions and load currents as following.

$$i_n = \sum_{x=u,v,w} \left(s_{x3} \times s_{x4} \times i_x \right). \quad \text{.....(11)}$$

The variation of the dc-bus neutral point potential includes [15]:

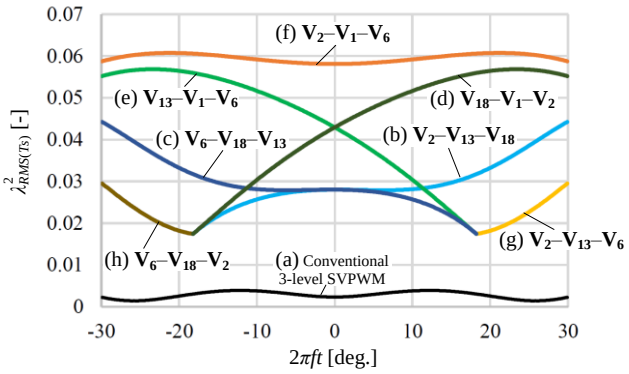
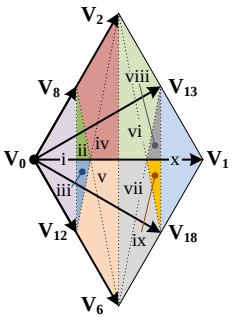


Fig. 8. Phase angle dependencies of RMS value of harmonic flux over control period at m = 1.0.



Area	Vectors
i	**V8–V0–V12**
ii	**V6–V12–V8**
iii	**V2–V8–V12**
iv	**V2–V8–V6**
v	**V6–V12–V2**
vi	**V2–V13–V6**
vii	**V6–V18–V2**
viii	**V6–V18–V13**
ix	**V2–V13–V18**
x	**V13–V1–V18**

Fig. 9. Proposed vector patterns to minimize RMS value of 3LVSI input current when i_u is positive and i_v and i_w are negative with consideration of load current quality.

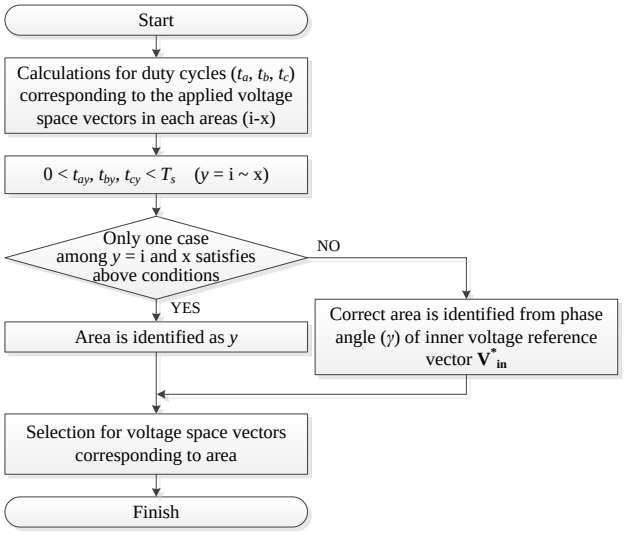


Fig. 10. Flowchart for determining detailed area i-x and applied voltage space vectors.

- the dc components due to the error of the common-mode voltage of 3LVSI or the capacitance mismatch connected in series,
- and the fluctuation at triplen frequency of the fundamental waveform due to the common-mode voltage fluctuation.

Both of them cause an excessive high voltage across the switching devices, load current distortion, and motor torque ripple; thus, the dc-bus neutral point potential control is necessary. Note

that these problems occur both in the conventional and proposed SVPWM unless the switching state (0) with the phase voltage of zero is not used. Generally, the duty cycle of redundant vectors, of which have redundant switching states such as **V**7 [+ 0 0] and [0 – –], is rearranged in order to reduce the variation of the dc-bus neutral point potential [16]. However, in the high-modulation index region of the proposed SVPWM, no redundant vectors are selected; thus, the dc-bus neutral point potential control is not achievable. Note that the following two approaches have the potential to achieve the neutral potential control in the high-modulation index region of the proposed SVPWM:

- applying only large active vectors (e.g., **V**1 [+ – –], **V**2 [+ + –], **V**3 [– + –], **V**4 [– + +], **V**5 [– – +], **V**6 [+ – +] for proposed sector A), which do not depend on the dc-bus neutral point potential, with the sacrificed load current quality, or
- partially (e.g., one-sixth phase angle period of all proposed sectors) applying the conventional SVPWM, which uses the redundant vectors during every switching period, with the sacrificed reduction effect on the input current harmonics.

4. Adaptation to Wide Load Power Factor Range

The reduction of the RMS value of the 3LVSI input current through the use of these optimized combinations of the voltage space vectors is dependent on the load power factor because the instantaneous values of the input current is dependent on not only the switching patterns but also the output phase current. Therefore, the adaption to the load power factor variation is important to reduce the 3LVSI input current harmonics over wide load power factor range, which is a typical requirement of the motor drive system.

Table 2 lists the sector definitions of the proposed SVPWM. These sectors A–F are determined by the combination of the detected output phase current directions and used as the information to recognize the load conditions.

Fig. 11 shows the layout of the proposed sectors in the $\alpha\beta$ reference frame at the load power factor of 0.766 (40° lagging). The proposed vector patterns shown in Fig. 9 reduces the RMS value of the 3LVSI input current only when i_u is positive and i_v and i_w are negative, i.e., the sector A. These proposed sectors are rotated by the phase shift angle φ according to the variation of the load power factor. As a result, the proposed sectors A-F will lead by the load power factor angle φ from the corresponding conventional sectors I-VI. As shown by the mesh area in Fig. 11, a part of sector A is not available with the optimized combinations of the voltage space vectors for the sector A because the mesh area is not covered by the proposed vector patterns. In these mesh areas, new combinations of the space vectors are ineffective in reducing the RMS value of 3LVSI input current; hence, the conventional SVPWM is applied.

5. Analytical Evaluations

5.1 RMS value of DC-link Capacitor Current Since the DC-side of the three-phase VSI operates at six-fold fundamental frequency and the P-side and N-side operate symmetrically, the RMS value of 3LVSI input current is calculated from the P-side input current by considering only a third of the fundamental period as:

Table 2. Sector definitions of proposed SVPWM.

Sector	Current polarity (P: Positive, N: Negative) i_u	i_v	i_w
A	**P**	**N**	**N**
B	P	P	N
C	N	P	N
D	N	P	P
E	N	N	P
F	P	N	P

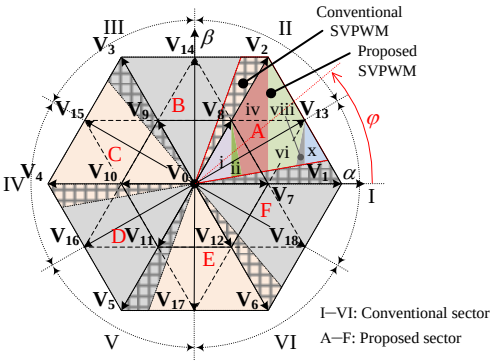


Fig. 11. Layout of proposed sectors in $\alpha\beta$ reference frame at load power factor of 0.766 (40° lagging). The proposed sector A leads by 40° from the conventional sector I.

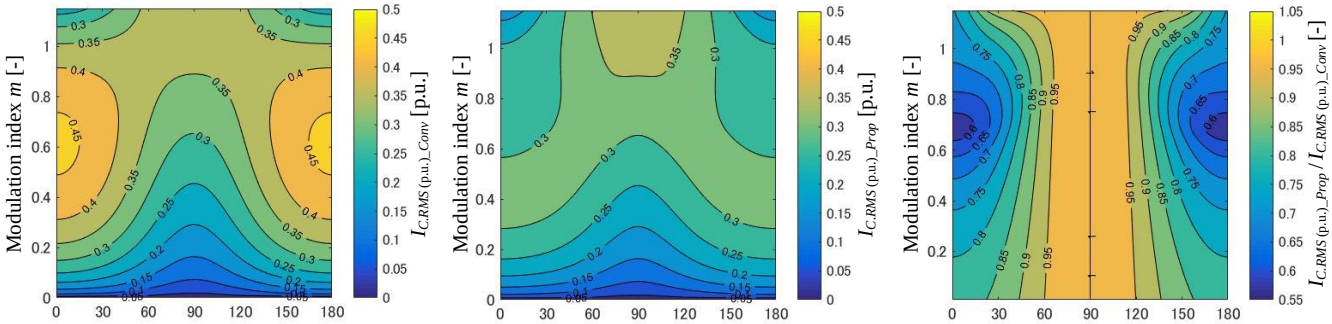
$$I_{DC.in.RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \frac{1}{2}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}\left(i_{DC.in.P,k}^2 + i_{DC.in.N,k}^2\right)\right)d\theta} = \sqrt{\frac{3}{2\pi}\int_0^{\frac{2\pi}{3}}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}\left(i_{DC.in.P,k}^2\right)\right)d\theta}, \quad (12)$$

The normalized DC-link capacitor RMS current is calculated based on (7), (8), and (12) as:

$$I_{C.RMS(\text{p.u.})} = \sqrt{\frac{3}{2\pi}\int_0^{\frac{2\pi}{3}}\left(\sum_{k=a,b,c}\frac{t_k}{T_s}\left(i_{DC.in.P,k} - i_{DC.in.ave}\right)^2\right)d\theta}. \quad (13)$$

Fig. 12 shows the analytical results of the DC-link capacitor RMS current with regard to the modulation index and the load power factor angle. Fig. 12(a) demonstrates that $I_{C.RMS(\text{p.u.})\_Conv}$ becomes the maximum at around $m = 0.6$ and absolute value of the load power factor $|\cos\varphi| = 1.0$ with the conventional SVPWM. On the other hand, Figs. 12(b) and (c) demonstrate that the proposed SVPWM reduces $I_{C.RMS(\text{p.u.})}$ under almost conditions of m and φ except for $\varphi = 90°$. In addition, a higher $|\cos\varphi|$ leads to a greater reduction effect on $I_{C.RMS(\text{p.u.})}$. This trend is resulted from the relationship between φ and the application ratio of the optimized combination of the voltage space vectors. When $|\cos\varphi|$ is lower than 0.866, the conventional SVPWM is partially applied in whole phase range as observed in Fig. 11. The application ratio of the optimized vector patterns decreases as $|\cos\varphi|$ becomes small, and there is no $I_{C.RMS(\text{p.u.})}$ difference between the conventional and proposed SVPWM when $\cos\varphi = 0$.

5.2 RMS value of Harmonic Flux Since the voltage space vectors which are symmetric with regard to every 60° of phase angle are applied in the modern PWM strategy for three-phase system, the characteristics of $\lambda^2_{RMS(Ts)}$ have the six-fold symmetry. So, the RMS value of the harmonic flux over



(a) Conventional SVPWM. (b) Proposed SVPWM. (c) $I_{C.RMS\,(p.u.)\_Prop} / I_{C.RMS\,(p.u.)\_Conv}$ ratio.

Fig. 12. Analytical results of DC-link capacitor RMS current.

fundamental period is calculated as:

$$\lambda_{RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \lambda_{RMS(T_s)}^2 \, d\theta}. \quad \text{..... (14)}$$

The load current quality with respect to the modulation index is evaluated without any load information by calculating the above formula. In addition, relative comparison is possible by using λ_{RMS}.

Fig. 13 shows the RMS values of the harmonic flux over fundamental period in the linear modulation range. The distance between the harmonic flux trajectories and the origin, which is the initial value of $\boldsymbol{\lambda_h}$ at the beginning of the carrier cycle, corresponds to the magnitude of the harmonic flux [14]. Thus, Fig. 13 confirms that the proposed SVPWM worsens the harmonic flux compared with those obtained with the conventional SVPWM. This is because the proposed vector patterns result in the application of the voltage space vector which is not the closest to $\mathbf{V}^*$, i.e., $\mathbf{V_6}$ and $\mathbf{V_{13}}$ in Fig. 6.

6. Simulation Results

Fig. 14 shows the PLECS simulation results with each modulation method at the modulation index of 0.930 and the load power factor of 0.866. The zoomed-in waveforms of the input current demonstrate that the width of the step change in the input current is reduced by the proposed SVPWM.

7. Experimental Results

The performances of the conventional and proposed SVPWM are verified in experiment. In this experiment, 3LVSI, composed of IGBT power modules (2MBI150U2A-060, Fuji Electric Co., Ltd.), is operated at the switching frequency of 10 kHz. A test three-phase induction motor (MVK8115A-R, Fuji Electric Co., Ltd.), the rated power of which is 3.7 kW, is controlled by V/f control with the conventional and proposed SVPWM, which are implemented into an evaluation board (TMS320C6713, Texas Instruments).

7.1 Input Current Harmonics Fig. 15 shows the operating waveforms of 3LVSI with each modulation method at the modulation index of 0.930 and the load power factor of 0.866. The width of the envelope in the input current is reduced by the proposed SVPWM. On the other hand, the transitions between $+E_{dc}$ and $-E_{dc}$ occur at worst in the line-to-line voltage with the proposed SVPWM due to the proposed selection of the voltage space vectors, whereas the voltage transition range with the conventional SVPWM is $E_{dc}/2$.

Fig. 16 shows the harmonic components of the input current under the same conditions in Fig. 15. The 100% of the vertical axis

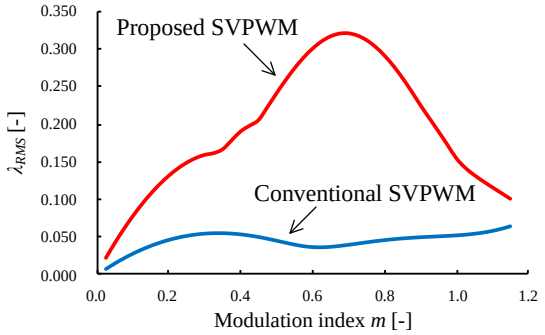
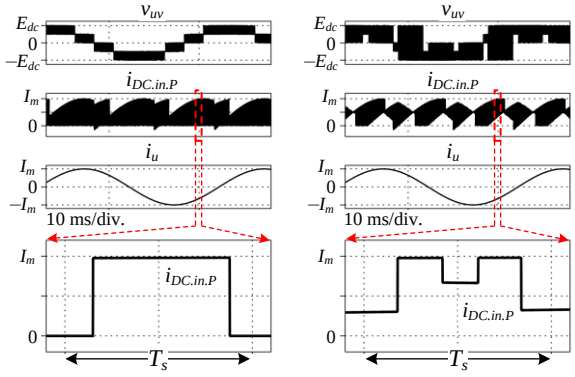


Fig. 13. Comparison of harmonic flux RMS value. In the proposed SVPWM calculations, the load power factor is set to 1.



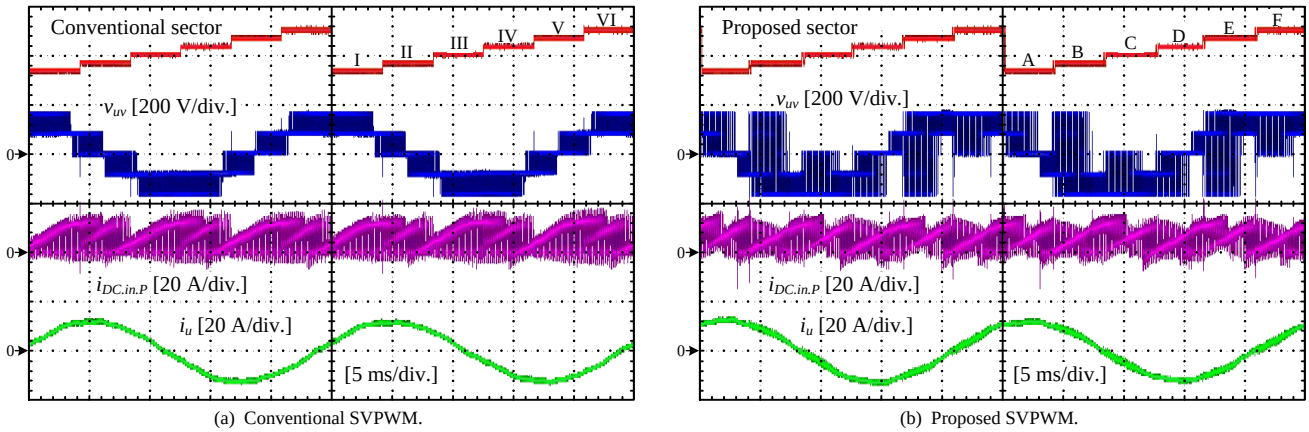
(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 14. Simulation results at m = 0.930 and cos φ = 0.866 (30° lagging); output line-to-line voltage, P-side input current, and output phase current.

indicates the maximum value of the output phase current. The proposed SVPWM reduces the switching frequency component by 16.6 points at most. Furthermore, the normalized input current harmonics, estimated as follows, is reduced by 27.4%.

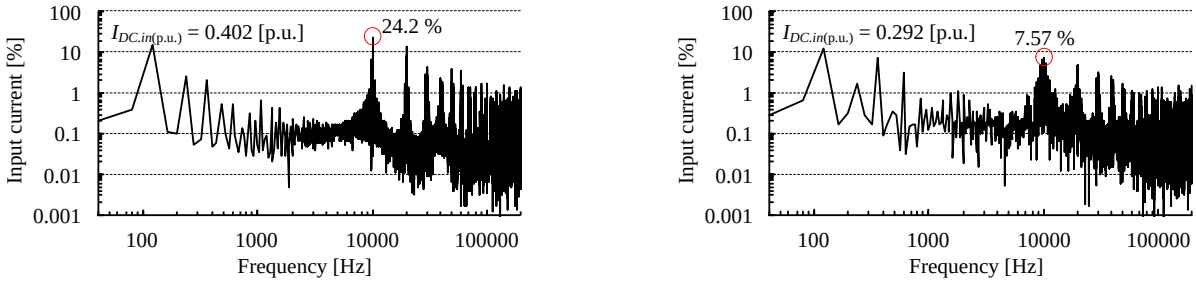
$$I_{DC.in(p.u.)} = \frac{I_{DC.in.RMS}}{I_m} = \frac{1}{I_m}\sqrt{\sum_{l=1}\left(\frac{1}{\sqrt{2}} i_{DC.in.l}\right)^2} \quad \text{..... (15)}$$

where $I_{DC.in.RMS}$ is the RMS value of the input current harmonics, l is the harmonic order, and $i_{DC.in.l}$ is the l-order component of the input current. The harmonic components of the input current up to 20th-order of the switching frequency are considered in this evaluation.



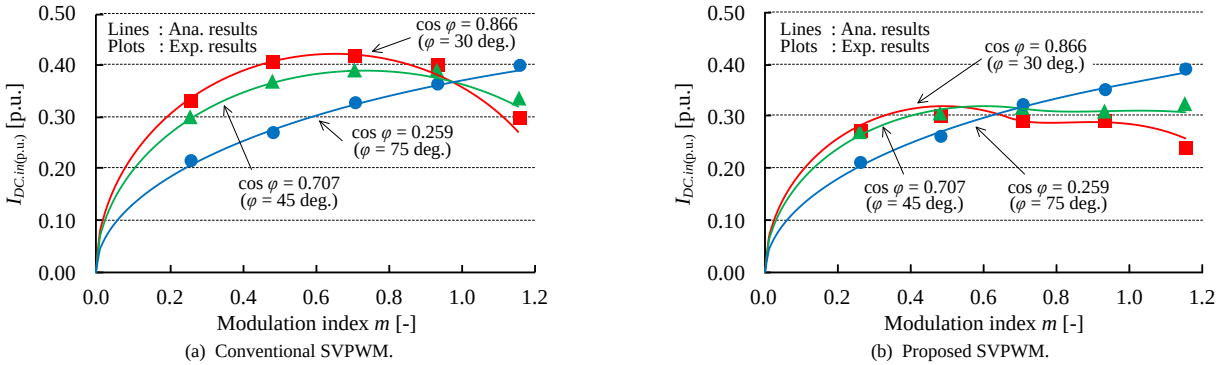
(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 15. Experimental waveforms at $m = 0.930$ and $\cos\varphi = 0.866$ (30° lagging); sector, output line-to-line voltage, P-side input current, and output phase current.



(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 16. Harmonic components of input current at $m = 0.930$ and $\cos\varphi = 0.866$ (30° lagging) (under same conditions as in Fig. 15).



(a) Conventional SVPWM. (b) Proposed SVPWM.

Fig. 17. Analytical and experimental results of input current harmonics.

Fig. 17 shows the analytical and experimental results of the input current harmonics at the load power factor from 0.259 to 0.866. The proposed SVPWM reduces the input current harmonics under any conditions of the modulation index and the load power factor. Furthermore, these results confirm that the experimental results of the input current harmonics match the analytical values well. A higher load power factor enables a greater reduction effect on the input current harmonics to be obtained.

7.2 Output Phase Current Harmonics Fig. 18 shows the total harmonic distortion (THD) of the output u-phase current at the load power factor of 0.866. The harmonic components up to 40th-order of the fundamental frequency are considered in this evaluation. The proposed SVPWM leads to the higher distortion of the output phase current than those with the conventional SVPWM, which is also observed from harmonic flux analysis in Fig. 13.

7.3 Inverter Efficiency Fig. 19 shows the 3LVSI efficiency, measured using Yokogawa WT 1800 power analyzer, at the load power factor of 0.866. Fig. 19 demonstrates that the proposed SVPWM improves the efficiency. The proposed SVPWM may lead to the increased number of the voltage vector area changing timing. However, the occurrence frequency of the voltage vector area changing in the proposed SVPWM is much smaller than the switching frequency. Figs. 5 and 6 demonstrate that the proposed SVPWM leads to less number of switching transitions in each switching period compare to the conventional SVPWM. Therefore, the proposed SVPWM reduces the total number of switching transitions over the fundamental period compared to the conventional, leading to the small switching loss.

7.4 Common Mode Voltage The common-mode voltage of the three-phase inverter (v_{ng} in Fig. 1) is defined as the potential of the star point of the motor load (n in Fig. 1) with respect

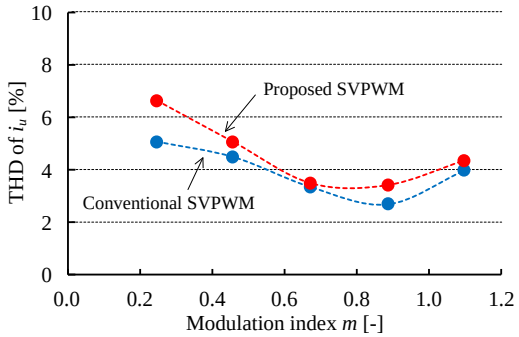


Fig. 18. Output u-phase current THD comparison between conventional and proposed SVPWM against different modulation index at cos φ = 0.866.

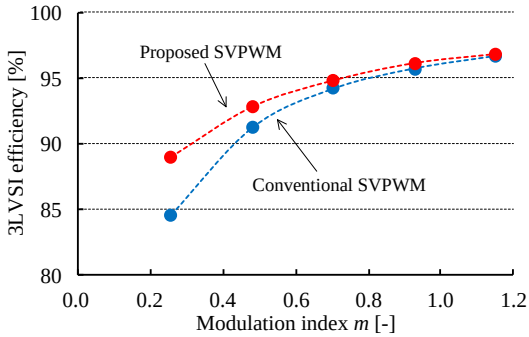


Fig. 19. 3LVSI efficiency comparison between conventional and proposed SVPWM against different modulation index at cos φ = 0.866.

to the motor-frame ground (g in Fig. 1). In practical, the potential of the center of the dc-bus (o in Fig. 1) with respect to the ground v_{og} is small and slowly varies compared to v_{no}. Therefore, the common-mode voltage v_{com} is defined as the potential difference between n and o as [17]:

$$v_{com} = v_{ng} = v_{no} + v_{og} \approx v_{no} = \frac{v_{uo} + v_{vo} + v_{wo}}{3}. \quad \text{..... (16)}$$

The common-mode voltage with large magnitude might result in high common-mode current (CMC, motor leakage current). This may lead to the motor bearing failures, EMI noise and so on [18]–[20]. Note that CMC (motor leakage current) flows to ground through the parasitic capacitances between the motor wirings and frame [19].

Fig. 20 shows the measured common-mode voltage with each modulation method at the modulation index of 0.930 and the load power factor of 0.866. Note that the star point of the several hundred kΩ resistances connected to 3LVSI three-phase outputs is probed to observe v_{com} as the imaginary star point of the motor load. Fig. 20 demonstrates that the peak to peak value of v_{com} is increased with the proposed SVPWM compared to the conventional SVPWM. However, the dv/dt of v_{com} is important for the electromagnetic interference (EMI) [21]. When the conventional SVPWM is applied, the equivalent zero vector of the two-level SVPWM in each conventional sector (e.g., $\mathbf{V}_7$ in the sector I) is always applied during the switching period. The both switching states of the equivalent zero vector (e.g., [+ 0 0] and [0 – –] as $\mathbf{V}_7$) leads to the v_{com} step change of $E_{dc}/2$ over an entire period. On the other hand, the proposed vector patterns to minimize the RMS value of 3LVSI

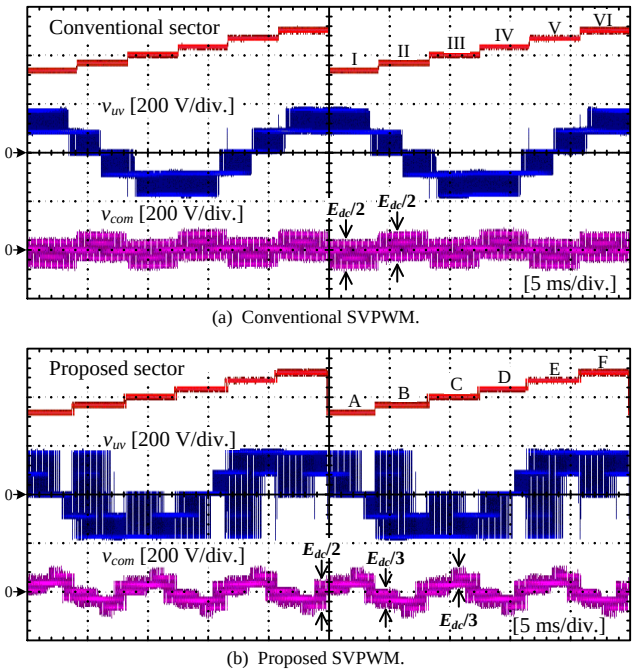


Fig. 20. Measured common-mode voltage at m = 0.930 and cos φ = 0.866 (30° lagging).

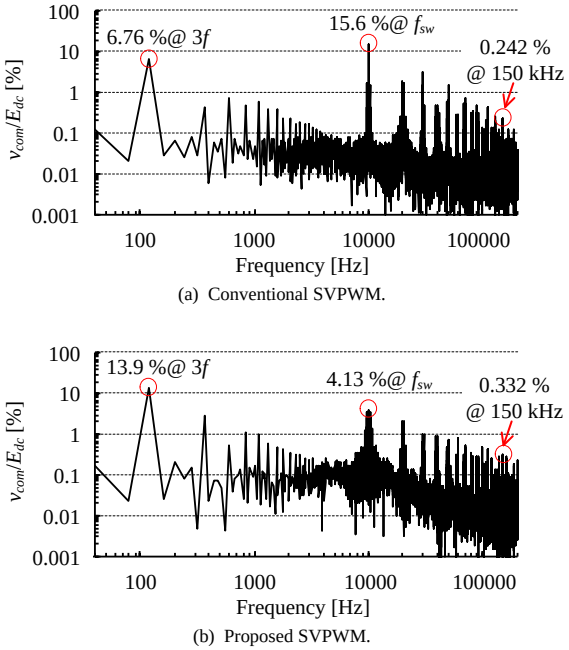


Fig. 21. Harmonic components of common-mode voltage at m = 0.930 and cos φ = 0.866 (30° lagging) (under same conditions as in Fig. 20). The fundamental frequency f is 40 Hz. The switching frequency f_{sw} is 10 kHz.

input current do not contain the application of the equivalent zero vectors, leading the smaller v_{com} step change of $E_{dc}/3$.

Fig. 21 shows the harmonic component of the common-mode voltage under the same conditions in Fig. 20. Note that the common-mode voltage is normalized by E_{dc}. By reducing the step change in v_{com} with the proposed SVPWM, the switching frequency component of 10 kHz is reduced by 11.5 points, might be leading to the smaller motor leakage current peak. On the other hand, the proposed SVPWM worsens the 3rd-order v_{com} component by 7.14

points compared to the conventional SVPWM. In the proposed SVPWM, the positive switching state (+) is mainly applied in the following proposed sectors (A, C, E), whereas the negative switching state (–) is mainly applied in the following proposed sectors (B, D, F). This asymmetric selection of the switching states during the consecutive proposed sectors results in the larger v_{com} fluctuation at triple frequency of the fundamental waveform, which is observed in Fig. 20(b). Furthermore, the high-frequency component such as of 150 kHz is increased by 0.0897 points due to the complicated voltage space vector selections in the proposed SVPWM. Assuming that CMC component of 150 kHz is dominant to design common-mode filter attenuation, the worsened v_{com} component of 150 kHz with the proposed SVPWM indicates that the proposed SVPWM might lead to the bulkier common-mode filter than those with the conventional SVPWM.

8. Conclusion

A novel SVPWM was proposed to reduce 3LVSI input current harmonics over wide variation of the load power factor. This proposed SVPWM contributed to the current stress reduction of the smoothing capacitor and its lifetime extension. The input current harmonics was reduced by optimizing the combinations of the applied voltage space vectors to minimize the fluctuation of the instantaneous input current value around its average value. In addition, this strategy could adapt to the wide range of load power factor by changing the combinations of the applied voltage space vectors according to the directions of the output phase currents.

The experimental results confirmed that the proposed SVPWM reduce the rms value of 3LVSI input current by 27.4%, while it worsened 3LVSI output current THD. For the film capacitors in the dc-bus of 3LVSI, the 27.4% input current harmonics reduction might lead to 47.3% reduction of the capacitor loss and its heating. Assuming that the electrolytic capacitors (NX series [22], Nichicon Corp.) is applied in the dc-bus of 3LVSI, it might lead to 1.36 times capacitor lifetime extension based on the estimated lifetime equation [12][23]. Furthermore, the proposed SVPWM reduced 3LVSI input current harmonics over entire range of the load power factor, which is the typical requirement of the motor drive system. On the other hand, the dc-bus neutral point potential control is not achievable in the high-modulation index region of the proposed SVPWM because no redundant vectors are used. However, by sacrificing the load current quality or the reduction effect on the input current harmonics, the dc-bus neutral point potential control is achievable. In addition, the effect on EMI might be another drawback of the proposed SVPWM and will be future task.

References

(1) A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523 (1981)

(2) W. Song, X. Feng, and K. Ma Smedley, "A Carrier-Based PWM Strategy With the Offset Voltage Injection for Single-Phase Three-Level Neutral-Point-Clamped Converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083–1095 (2013)

(3) X. Ge, J. Pu, B. Gou, and Yong-Chao Liu, "An Open-Circuit Fault Diagnosis Approach for Single-Phase Three-Level Neutral-Point-Clamped Converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2559–2570 (2018)

(4) Fuji Electric Co., Ltd., Tokyo, Japan. *Fuji Electric Journal*, vol. 79, no. 2, pp. 110–117 (2006) (in Japanese)

(5) Rubycon Corp., Nagano, Japan. *Film Capacitor Technical Notes*. [Online]. Available: http://www.rubycon.co.jp/en/products/film/technote.html

(6) M. H. Bierhoff and F. W. Fuchs, "DC-link Harmonics of Three-Phase Voltage-Source Converters Influenced by the Pulsewidth-Modulation Strategy—An Analysis," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2085–2092 (2008)

(7) B. P. McGrath and D. G. Holmes, "A General Analytical Method for Calculating Inverter input current Harmonics," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1851–1859 (2009)

(8) J. S. Lee and K. B. Lee, "New Modulation Techniques for a Leakage Current Reduction and a Neutral-Point Voltage Balance in Transformerless Photovoltaic Systems Using a Three-Level Inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp 1720–1732 (2014)

(9) M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527 (2013)

(10) A. R. Beig, G. Narayanan, and V. T. Ranganathan, "Modified SVPWM Algorithm for Three Level VSI With Synchronized and Symmetrical Waveforms," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 486–494 (2007)

(11) T. Takeshita, "Output Voltage Harmonics Suppression of Matrix Converters Using Instantaneous Effective Values," in *Conf. Proc. IEEE Energy Convers. Congr. Expo.*, 270_0839 (2010)

(12) K. Nishizawa, J. Itoh, A. Odaka, A. Toba, and H. Umida, "Current Harmonic Reduction Based on Space Vector PWM for DC-Link Capacitors in Three-Phase VSIs Operating Over a Wide Range of Power Factor," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4853–4867 (2019)

(13) K. Nishizawa, J. Itoh, A. Odaka, A. Toba, and H. Umida, "Reduction of Input Current Harmonics based on Space Vector Modulation for Three-level Inverter with varied Power Factor," in *Conf. Proc. International Conf. on Electrical Machines and Systems*, DS1G-2-17 (2016)

(14) A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple Analytical and Graphical Methods for Carrier-Based PWM-VSI Drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61 (1999)

(15) S. Ogasawara and H. Akagi, "Analysis of Variation of Neutral Point Potential in Neutral-Point-Clamped Voltage Source PWM Inverters," in *Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, pp. 965–970 (1993)

(16) A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-Vector Pulsewidth Modulation for Three-Level NPC Converter With the Neutral Point Voltage Control," *IEEE Trans. on Ind. Electron.*, Vol. 58, No. 11, pp. 5076–5086 (2011)

(17) A. M. Hava and E. Ün, "A High-Performance PWM Algorithm for Common-Mode Voltage Reduction in Three-Phase Voltage Source Inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008 (2011)

(18) A. von Jouanne, P. Enjeti, and W. Gray, "Application Issues for PWM Adjustable Speed AC Motor Drives," *IEEE Ind. Appl. Mag.*, vol. 2, pp. 10–18 (1996)

(19) J. M. Erdman, R. J. Kerkman, D.W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC Motor Bearing Currents and Shaft Voltages," *IEEE Trans. Ind. Appl.*, vol. 32, pp. 250–259 (1996)

(20) E. Zhong and T. A. Lipo, "Improvements in EMC Performance of Inverter-Fed Motor Drives," *IEEE Trans. Ind. Appl.*, vol. 31, no. 6, pp. 1247–1256 (1995)

(21) X. Chen, D. Xu, F. Liu, and J. Zhang, "A Novel Inverter-Output Passive Filter for Reducing Both Differential- and Common-Mode dv/dt at the Motor Terminals in PWM Drive Systems," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 1, pp. 419–426 (2007)

(22) Nichicon Corp., Tokyo, Japan. *Datasheet of Aluminum Electrolytic Capacitors (NX Series)*, Cat. 8100D. [Online]. Available: http://www.nichicon.co.jp/english/products/pdfs/e-nx.pdf

(23) Nichicon Corp., Tokyo, Japan. *Technical Notes on Aluminum Electrolytic Capacitors*, Cat. 8101E-1. [Online]. Available: http://www.nichicon-us.com/english/products/pdf/aluminum.pdf

Koroku Nishizawa (Student member) received the B.S. degree in electrical, electronics and information engineering from Nagaoka University of Technology, Niigata, Japan, in 2015, where he is currently working toward the Ph.D. degree. He is a student member of IEEJ and IEEE. His current research focuses on the modulation strategy of converters.

Jun-ichi Itoh

(Senior member) received his M.S. and Ph.D. degree in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan in 1996, 2000, respectively. From 1996 to 2004, he was with Fuji Electric Corporate Research and Development Ltd., Tokyo, Japan. He was with Nagaoka University of Technology, Niigata, Japan as an associate professor. Since 2017, he has been a professor. His research interests are matrix converters, dc/dc converters, power factor correction techniques, energy storage system and adjustable speed drive systems. He received IEEJ Academic Promotion Award (IEEJ Technical Development Award) in 2007. In addition, he also received Isao Takahashi Power Electronics Award in IPEC-Sapporo 2010 from IEEJ, 58th OHM Technology Award from The Foundation for Electrical Science and Engineering, November, 2011, Intelligent Cosmos Award from Intelligent Cosmos Foundation for the Promotion of Science, May, 2012, and Third prize award from Energy Conversion Congress and Exposition-Asia, June, 2013. Prizes for Science and Technology (Development Category) from the Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology, April 2017. He is a senior member of the Institute of Electrical Engineers of Japan, the Society of Automotive Engineers of Japan and the IEEE.

Akihiro Odaka

(Member) received the B.S. and M.S. degrees from Tokyo Denki University, Tokyo, Japan, in 1996 and 1998, respectively. Since 1998, he has been with Fuji Electric Co., Ltd., Tokyo. He is a member of IEEJ and IEEE. His research interests include static converters and power semiconductor applications.

Akio Toba

(Senior member) received the M.E. and Ph.D. degrees from Tokyo Metropolitan University, Tokyo, Japan, in 1994 and 2006, respectively. In 1994, he joined Fuji Electric Co. Ltd., Tokyo, where he has been conducting the research and development of power electronics, motor drives, and electric machines. From 1997 to 1999, he was a Visiting Researcher with Wisconsin Electric Machines and Power Electronics Consortium, University of Wisconsin, Madison, USA. He is a senior member of IEEJ and a member of IEEE.

Hidetoshi Umida

(Fellow) received the B.E., M.E. and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1970, 1981 and 1984, respectively. Since 1984, he has been with Fuji Electric Co., Ltd., Tokyo. He is currently a Chief Engineer with Fuji's Corporate R&D Headquarters. His research interests include control theory and its application to motor drives and converters. He is a fellow of IEEJ and a member of IEEE.