

Hybrid Multiple Chopper Cells of PWM and Square-wave Operation for Solid-state Transformer

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Keywords

«Smart grids», «Modulation strategy», «Wide bandgap devices», «ZVS converters», «Solid-state transformer».

Abstract

This paper proposes a modulation method combining PWM and square-wave drive for solid-state transformers (SSTs). Modular multilevel configurations based on input series and output parallel (ISOP) have been widely used. The advantage of ISOP configuration is that low on-resistor and low-switching-loss devices are available because the applied voltage on each cell is divided by the number of cells. For this reason, SST based on the ISOP configuration is widely used in a medium-voltage system. However, this configuration has a problem that a high number of medium frequency devices, such as SiC-MOSFET, increases the cost of SST. In order to solve above problem, a reduction method of medium frequency devices are proposed. In the proposed method, one cell is driven with the PWM operation in order to compensate for the harmonic component. The other cells are driven by square-wave operation. Thus, the power factor correction (PFC) is held by different switching frequencies in each cell converter operated.

Owing to the proposed operation, the medium frequency driving devices can be replaced with low-frequency devices, such as Si-IGBT, for cost-saving. As the drawback of the proposed control, the conduction time is unbalanced in the square wave cells. Thus, this paper also proposes the sorting operation to balance the output power of cells operated with square-wave drive. From the experimental results, THD of the input current is 2.91%, the input power factor is 0.99, the maximum efficiency is 94.2% at 0.3p.u.(1.p.u.=1.0 k W).

Introduction

In recent years, the smart grid has attracted much attention due to the increasing demand for renewable resources. The solid-state transformer (SST) is known as a critical component in the smart grid system. SST consists of power converters and a medium frequency transformer for galvanic isolation. The power converter provides power flow control and compensation of the reactive power. The medium frequency transformer enables to increase the power density of the converter.

Focusing on the circuit topology of SST, various circuit topologies have been proposed in this decade from the view of efficiency, cost, and protection functions [1-20]. In [8-9], the ISOP configuration based on the PWM rectifier and dual active bridge has been proposed. The advantage of this topology is achieving soft-switching in a wide load range. However, a lot of switching devices are required for the multistage cell. Also, the DC link capacitor with a large capacity is needed in order to keep the DC-link voltage in the primly side. In [10-11], AC/AC-based ISOP configuration to reduce conversion stage and passive component has been proposed. This topology increases the number of components because the converter needs bidirectional switches. For these topologies, SiC-MOSFETs have been widely used because of them high-switching speed and low on-resistance. The use of SiC-MOSFETs has a problem with the cost of the SiC devices. The SiC devices are still more expensive than Si-IGBT, even if the demand for SiC devices is increased.

In this paper, the hybrid modulation method for ISOP is proposed in order to reduce the cost of SST. The new modulation method is that one of the cells is driven with PWM in order to compensate for the harmonic components of the input current. The other cells are driven by square-wave operation in order to correct the input power factor. It is possible to use the devices with the slower switching speed because these switches are operated at the double of the grid frequency. It will contribute to the cost-saving because Si-IGBT will be an option for these cells.

Besides, the proposed method causes the unbalance of the power loss among the cells operated with the square-wave operation due to the different conduction time of switching devices. Therefore, this paper also proposes the sorting operation, which improves the unbalance of power loss among square wave cells. The new contribution of this paper is reducing the cost of SST by replacing the high-frequency wide-bandgap devices to low-cost Si devices, in which only low-frequency operation is available.

Circuit configuration

System configuration

Figure 1 shows the circuit configuration of the single-phase SST with multiple cells. Each cell has PFC stages and isolated resonant DC/DC converter. The input of the PFC stage in the cells is connected in series. The outputs of the isolated resonant DC/DC converters, which ensure the galvanic isolation [16], are connected in parallel. The input diode rectifier is common for all cells to reduce the number of components. The high-frequency operation contributes to minimizing the isolation transformer. The transformer of the isolated resonant DC/DC converter is smaller than the conventional commercial frequency transformer because the switching frequency f_{sw_re} is higher than the grid frequency. Besides, the resonant capacitor C_r is connected to the primary side of the isolated transformer in series for the zero-voltage switching (ZVS) of the DC-DC converter with open-loop control. For the ZVS operation, the leakage inductance is designed to be negligibly smaller than the excitation inductance.

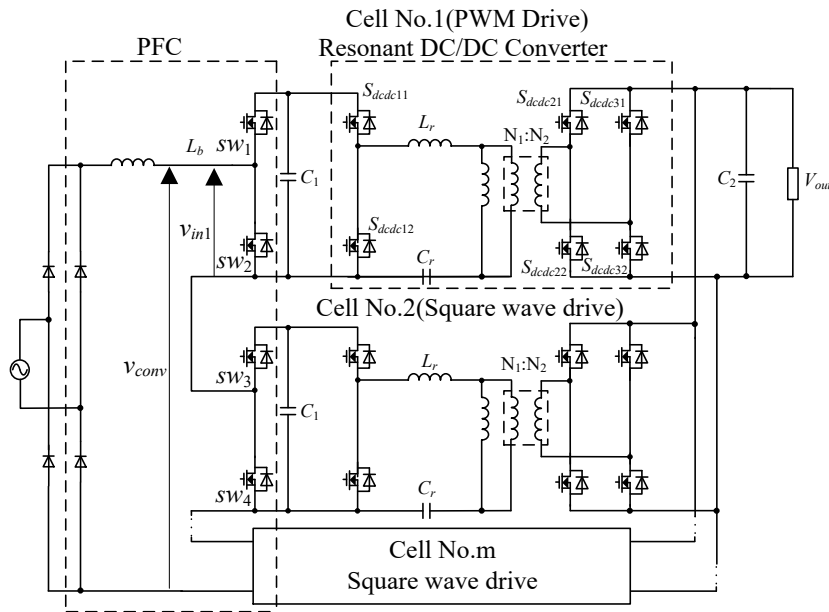


Fig. 1. Circuit configuration of the single-phase SST.
The new modulation method is applied into the PFC stage.

Conventional control of PFC stage

Figure 2 shows the block diagram of the conventional control method of the PFC stages. The conventional method controls output voltage with PWM for all cells. The overall PFC circuit controls output voltage and phase and amplitude of the input current to correct the input power factor. The phase of the inductor current is detected from the grid voltage. The output voltage of the overall cell converter is equally divided into each cell. Note that the phase-shifted carrier is used to reduce the current ripple.

The reference of the input current is a full wave rectified sine wave because the current reference is fed to the inductor on the PFC stage. The current reference is multiplied by the phase, which is generated by PLL of the grid voltage. The operation value of PI control is the total voltage of all cells. Thus, the voltage divided by the number of cells is the reference voltage for each cell. The switching timing of the PFC stage is shifted in each cell using the phase shift-carriers. Hence, the equivalent switching frequency is increasing in proportional to the number of cells. Equivalent switching frequency f_{eq} is given by

$$f_{eq} = mf_{sw_pfc} \quad (1),$$

where f_{sw_pfc} is the switching frequency of the PFC stage in each cell.

Figure 3 shows the switching pulse generation of the secondary-side rectifier. The full-bridge converter on the secondary side operates as a synchronous rectifier. The switching pulse is the same as the pulse of the primary side. In the primary side, resonant current i_{re} is positive when S_{dcdc11} , S_{dcdc21} , S_{dcdc32} are turn-on. Note that phase of primary side resonant current is a little different in order to design resonant DC/DC converter. Similarly, S_{dcdc12} , S_{dcdc22} , S_{dcdc31} are turn-on when the resonant current is negative.

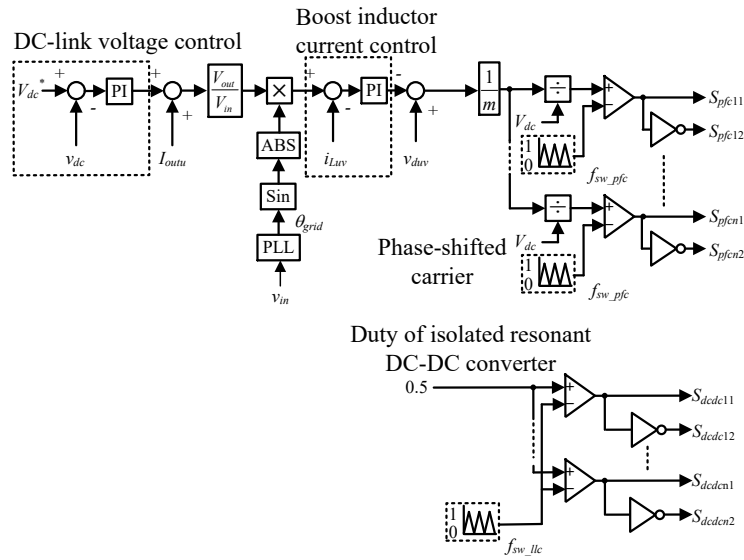


Fig. 2. Control diagram of conventional method in single-phase SST.

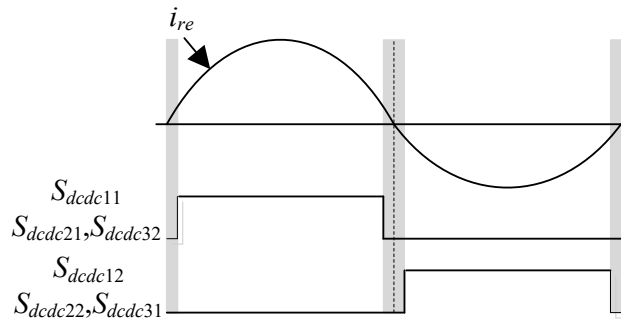


Fig. 3. Pulse generation for secondly side rectifier

Proposed modulation method of PFC stage

Control with square-wave operation

Figure 4 shows the relationship between the input voltage and output voltage of cell #1-3. The one of cells #1 is driven by the PWM operation in order to compensate for the harmonic component of other cells. The other cells #2 and 3 are driven by the square-wave operation. The output voltage of the cell operated with square wave is determined by the comparison with the reference voltage of the PFC stage and the DC-link voltage of each cell. The switching device on the upper arm of cell #2 sw_3 turns on when the output voltage reference v_{inv} is higher than DC-link voltage of cell #2. Similarly, the switching

PFC stage is different in each cell. It may accelerate the aging of capacitors or switching devices and shorten the running time of a specific cell by centering power loss.

Figure 6 shows the sorting operation with a PWM cell and five cells operated by square-wave drive. When the sorting operation is not worked, the output power of cell #2 is the largest in the all cell, and the output power of cell #6 is the smallest in all cell. It causes the problem that the advantage of the ISOP configuration is disappeared from the view of equally sharing load in each cell.

The proposed modulation has the freedom on the option which cell output in the long term. Therefore, the cell is selected to average the conduction time by the sorting operation. The sorting operation has five modes in five square-wave cells. First, the cell #2 output the maximum power, and #6 output the minimum power in the mode I. Second, the operation mode is shifted to mode II. The cell #6 outputs the maximum power and the cell #5 outputs the minimum power. Similarly, the mode is shifted in sequence from I to V. The average output power of each cell is balanced in 2.5 times of the output grid period.

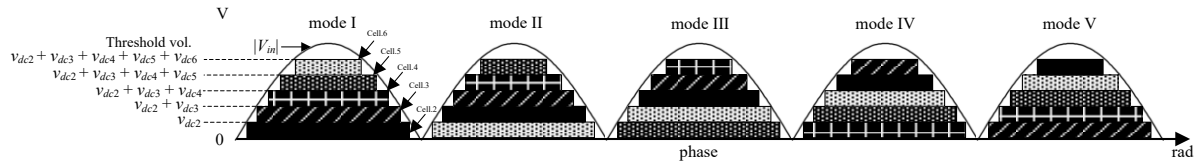


Fig. 6. Sharing input voltage in sorting operation with proposed method ($m = 6$).

Table II. Sorting operation of square wave cell with proposed method.

| | $v_{dc2} < v_{in} < \sum_{i=2}^6 v_{dci}$ | $\sum_{i=2}^5 v_{dci} < v_{in} < \sum_{i=2}^6 v_{dci}$ | $\sum_{i=2}^4 v_{dci} < v_{in} < \sum_{i=2}^6 v_{dci}$ | $\sum_{i=2}^3 v_{dci} < v_{in} < \sum_{i=2}^6 v_{dci}$ | $\sum_{i=2}^2 v_{dci} < v_{in} < \sum_{i=2}^6 v_{dci}$ |
|----------|---|--|--|--|--|
| mode I | Cell.2 | Cell.3 | Cell.4 | Cell.5 | Cell.6 |
| mode II | Cell.6 | Cell.2 | Cell.3 | Cell.4 | Cell.5 |
| mode III | Cell.5 | Cell.6 | Cell.2 | Cell.3 | Cell.4 |
| mode IV | Cell.4 | Cell.5 | Cell.6 | Cell.2 | Cell.3 |
| mode V | Cell.3 | Cell.4 | Cell.5 | Cell.6 | Cell.2 |

Simulation and Experimental Results

Simulation result of balancing control in conduction loss

In this section, the simulation result of the sorting operation is shown. Table III presents the simulation conditions. In this simulation, a constant voltage source of 200 V is used as the primary side DC link voltage of each cell because of evaluating the effects by eliminating the power ripple of DC-link voltage. The switching devices for cell driven by PWM is SiC-MOSFET (Rohm, SCT3040KR)[21]. The switching devices for the cells driven by square-wave is Si-IGBT (Fairchild, FGA20N120FTD)[22]. Figure 7 shows the simulation result with or without sorting operation. In this simulation, cell #1 is driven by PWM, and cell #2-6 are driven by square-wave. The conduction loss of each cell is given by

$$P_{con_PFC} = f_{sw} \int_{t_{on}}^{t_{off}} d \cdot i_{out} v_{ce} dt \quad (3),$$

where f_{sw} is the switching frequency of PFC in each cell. d is the duty ratio of PFC. The current i_{out} is RMS value of input current. v_{ce} is the corrector-emitter voltage of IGBT. The relationship between collector-emitter voltage is approximated as

$$v_{ce} = v_0 + r_{on} i_{out} \quad (4),$$

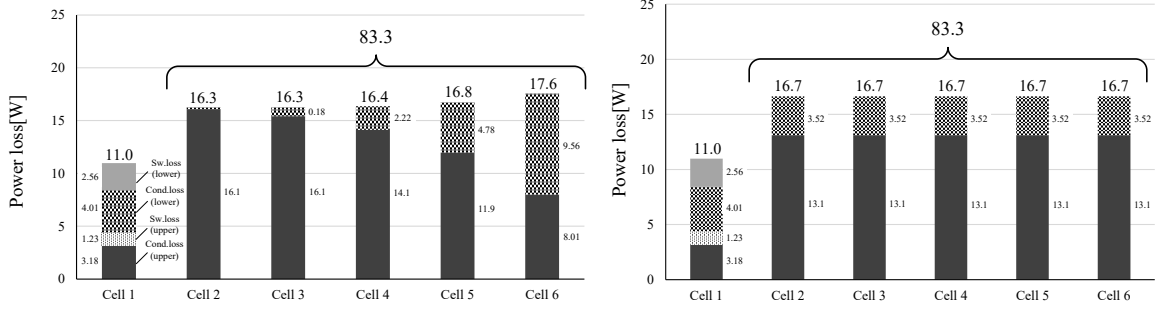
whereas v_0 is the corrector-emitter voltage at zero current of corrector-emitter, r_{on} is approximated on-resistance, and i_{out} is the instantaneous value of the conduction current.

Fig. 7(a) shows the conduction loss and switching loss without sorting operation. In the cell #2, the conduction loss of FWD is dominant because the conduction time of the upper arm is the longest in all cells. In contrast, in cell 6, conduction loss of lower IGBT is dominant because the conduction time of the lower arm is the second-longest in all cells.

Fig. 7(b) shows the simulation result of loss analysis with sorting algorithm. Meanwhile, the power loss of cells #2-6 is 16.7 W. It means that conduction loss of the upper and lower arm is balanced. Note that total loss is 83.3 W, which is equivalent to a total loss of the result without sorting operation of 83.3 W. Therefore, the loss balancing is achieved by the proposed method.

Table III. Simulation condition in sorting operation of square-wave cell.

| | | |
|------------------------------|---------------|----------------------|
| Input voltage | V_{in} | 800 V _{rms} |
| Rated output power | P_{out} | 16 kVA |
| Rated output voltage | V_{out} | 100 V |
| Switching frequency of PFC | f_{sw_pfc} | 30 kHz |
| Resonant frequency | f_o | 50 kHz |
| Number of cells | m | 6 |
| Boost inductor | L_b | 4 mH |
| Primary side capacitor | C_1 | 48 μ F |
| Resonant capacitor | C_r | 204 nF |
| Leakage inductor | L_r | 50 μ H |
| Secondary side capacitor | C_{out} | 3000 μ F |
| Trans turns ration | $N_1:N_2$ | 1:1 |
| Switching device(SiC-MOSFET) | | SCT3040KR |
| Switching device(Si-IGBT) | | FGA20N120FTD |



(a) Simulation result of power loss without sorting operation. (b) Simulation result of power loss with sorting operation.

Fig. 7. Simulation result of power loss in each cell.

Experimental result with conventional method

Table IV shows the parameters for the experiment. The input voltage is 200 V, the rated power is 1.0 kW, and the number of cells is three. Moreover, the prototype is operated with the conventional control block diagram, as shown in Fig. 3, and the proposed control, as shown in Fig. 5. The switching frequency of the PWM cell in the proposed control is three-times higher than the switching frequency of the conventional control for a fair comparison.

Figure 9 shows the operation waveforms of the conventional method. Fig. 9(a) shows that the input current THD is 2.91%, and the input power factor is 0.99. Fig. 9(b) shows that each cell is driven by PWM against grid voltage.

Experimental result with proposed method

Figure 10 shows the operation of the proposed method. In the proposed modulation, the switching frequency of the PFC circuits is 30 kHz. It means that the equivalent switching frequency f_{sw_eq} is 30 kHz. Whereas the switching frequency of the PWM cell in the proposed control method is 30 kHz for the fair comparison. Fig. 10(a) shows the result of the proposed modulation method. The input power factor is also 0.99. The input current THD is 2.91%. In addition, Fig. 10(b) shows the output square-wave driving in each cell with double of the grid frequency. The PWM cell compensates for the harmonic components by the square-wave cell.

Figure 11 shows that input current THD against the rotted power with the conventional and proposed method. PFC shows to compensate the harmonic component of input current. However, in light load, THD of the input current exceeded 5% with both controls. Improving the THD is future work.

Figure 12 shows the efficiency characteristic. The maximum efficiency is 94.2% at a load of 0.3 kW.. The efficiency at rated load is 84.4%.

Experimental result of the sorting operation

In this experiment, the output power is measured with or without the sorting operation. Experimental parameters are common shown in Table IV. The square-wave cell outputs in double of the grid frequency.

Figure 13 shows the operation waveform with sorting operation. The power factor of the input current is 0.99.

Figure 14 shows the experimental result of output power with or without the operation. The output power of cell #1 is 242 W, the output power of cell #2 is 485 W, and the output power of cell #3 is 233W without the sorting operation. It means that concentrating power loss occurs at a specific cell. In contrast, the output power of each cell is 304 W, 329 W, and 332W, respectively with the sorting operation. It clearly shows that unbalancing output power improves.

Table IV. Experiment parameter.

| | | |
|----------------------------|---------------|----------------------|
| Input voltage | V_{in} | 200 V _{rms} |
| Rated output power | P_{out} | 1.0 kW |
| Rated output voltage | V_{out} | 50 V |
| Switching Device | | SCT2080KE |
| Grid Frequency | f_s | 50 Hz |
| Primary side capacitor | C_1 | 1500 μ F |
| Resonant capacitor | C_r | 204 nF |
| Leakage inductor | L_l | 50 μ H |
| Secondary side capacitor | C_2 | 3600 μ F |
| Trans turns ration | $N_1:N_2$ | 1 : 1 |
| Number of cells | m | 3 |
| Switching frequency of PFC | f_{sw_pfc} | 30 kHz |
| Switching frequency of LLC | f_{sw_llc} | 50 kHz |

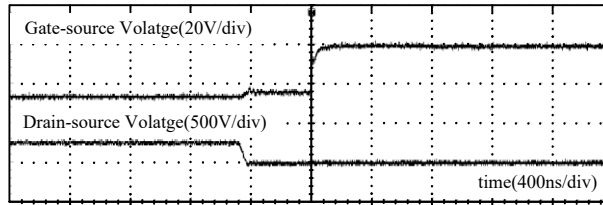
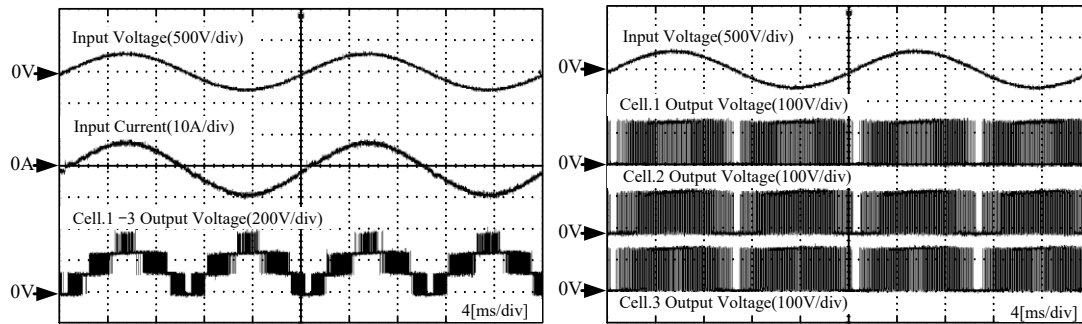
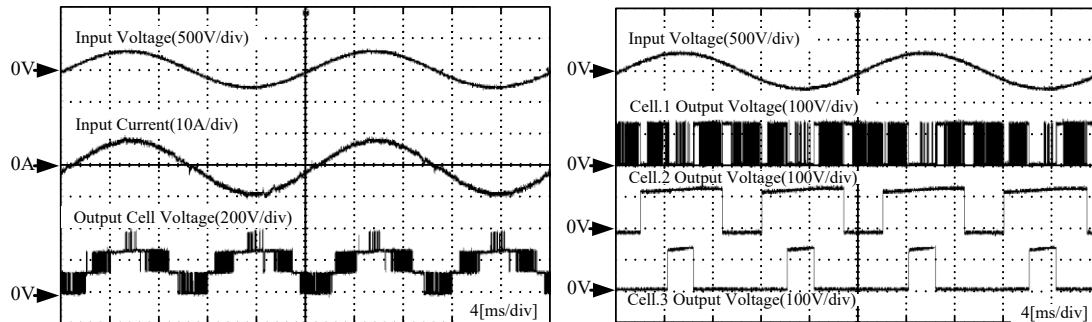


Fig. 8. Waveforms of ZVS operation in resonant DC/DC converter. The converter achieves ZVS of upper switches on resonant DC/DC.



(a) Operation waveform of SST with conventional method. (b) Operation waveform of SST with conventional method.

Fig. 9. Waveforms of SST, using conventional method.



(a) Operation waveform of SST with proposed method. (b) Output voltage of each cell with proposed method.

Fig. 10. Waveforms of SST, using proposed method.

Conclusion

This paper has proposed the hybrid modulation method, which combines PWM and square-wave operation for ISOP based SST. In the proposed method, one of the cells is driven by PWM in order to compensate for the harmonic component. The other cells are driven by square-wave operation in order to share the load. Moreover, this paper proposed the sorting operation in order to improve unbalancing power in each cell when the proposed modulation is used. As the experimental result, the input current THD is 2.91% at an output power of 1.0 kW whereas the input current THD of conventional modulation is 3.18%. The efficiency of the total system is 82.0% at 1.0 kW. Besides, the output power of the cell with the square-wave operation is balanced with the sorting operation.

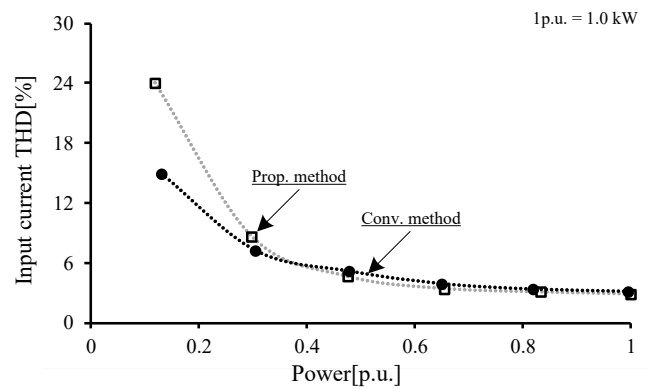


Fig. 11. Relationship between input current THD and input power with conventional and proposed modulation

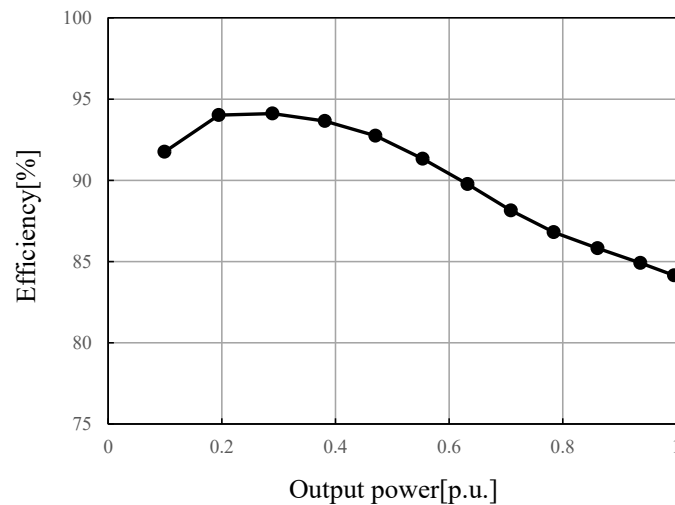


Fig. 12. Efficiency characteristic with proposed method.

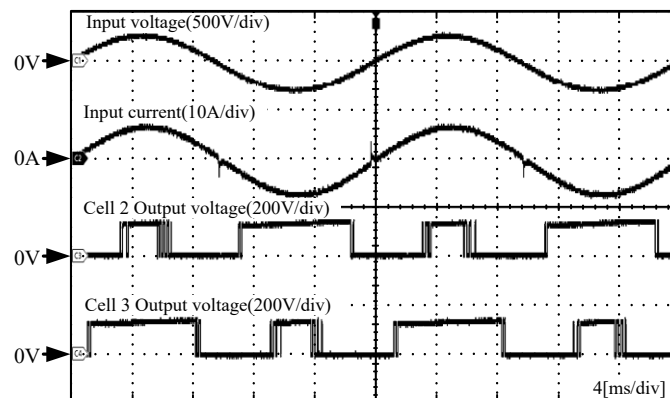


Fig. 13. Operation waveform with sorting operation.

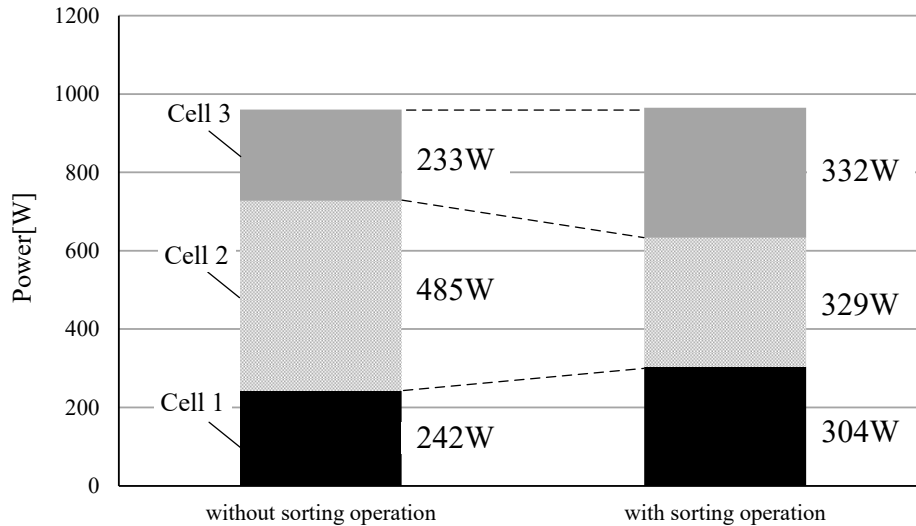


Fig. 14. Measured output power with no using sorting operation and using sorting operation.

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