Parasitic Parameters Analysis and Design of Snubber Circuit on PCB for High-frequency Wireless Power Transfer

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***Abstract*— This paper presents an analysis of the PCB pattern, which is for a high-frequency inverter circuit. In a high-frequency inverter circuit, the design of the snubber circuit, which suppresses surge voltage, is essential to achieve kilowatt operation. The authors are aiming to simulate a surge voltage in order to decide the parameters of the snubber circuit. In this paper, the surge voltage is simulated using the analysis result of the PCB and the models of the passive components. Furthermore, the surge voltage with changing the snubber capacitor is evaluated in order to make the relationship between the surge voltage and the snubber circuit parameters as the first step of the parameters design by using simulation.**

Keywords—Parasitic parameters, PCB, Surge voltage, Snubber circuit

I. Introduction

In recent years, the demand for the higher power density of a wireless power transfer (WPT) system is increasing. Notably, passive components such as inductors and capacitors should be miniaturized to reduce the circuit volume. Employing a high switching frequency is one of the methods to achieve high power density. Thus, the megahertz operation, which employs a GaN-transistor of a WPT system for EV charger, has been actively studied [1–2].

However, the effect of the parasitic parameters on a printed circuit board (PCB) should not be ignored when the switching frequency is high such as megahertz [3–4]. The parasitic inductance on the DC-bus or snubber circuit pattern will cause a surge voltage between a drain and a source of FETs. Thus, parasitic parameters on a PCB should be accurately analyzed.

In this paper, the parasitic parameters on the PCB are analyzed to estimate the surge voltage of the devices. First, the parasitic parameters on the PCB are analyzed by using electromagnetic analysis. In order to confirm the validation of the analysis result, analysis results are compared to the measurement result. Furthermore, the surge voltage between a drain and a source of FETs is simulated using the analysis result. The simulated waveform is compared to the measurement waveform. Finally, the maximum surge voltage value with changing the snubber capacitor is investigated as the first step of the circuit parameters design with simulation.

II. Electromagnetic Analysis of PCB Pattern

Figure 1 shows the circuit configuration of the megahertz resonant inverter. The GaN-transistors (PGA26E07BA: 600 V, 26 A, Panasonic) are used for megahertz switching (6.78–13.56 MHz). Parasitic parameters of the DC-bus are one of the causes of the surge voltage between the drain and the source of the switching devices. Therefore, the DC-bus pattern is analyzed and compared to the measurement result in order to confilme the accuracy of the electromagnetic analysis result.

Figure 2 shows a circuit pattern of the DC-bus on the PCB. Port 1 is the input side of the DC-bus, and Port 2 is the H-bridge side of the DC-bus. PCB consists of four conductive layers and three dielectric layers. Table 1 shows the layer parameters of the PCB. Furthermore, the copper conducting rate is 58.7 MS/m, the relative permittivity of the FR4 is 4.5

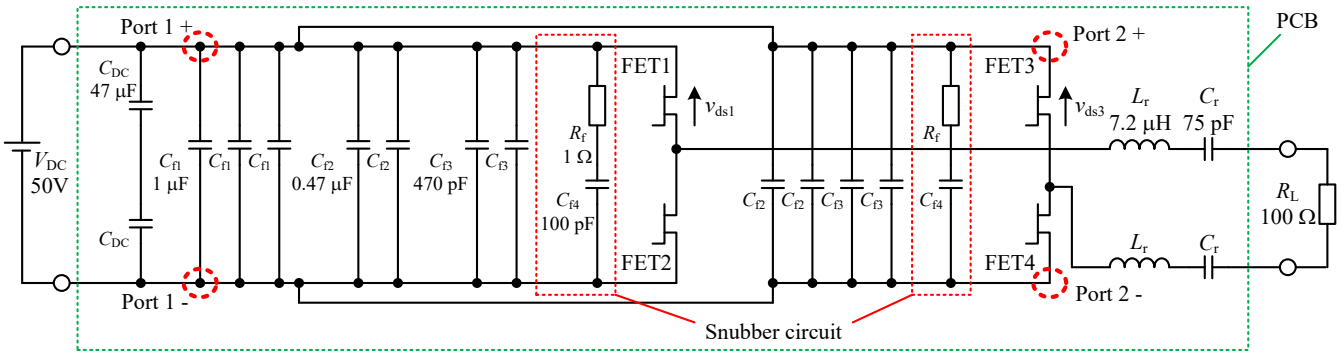


Fig. 1. High-frequency resonant inverter.

and loss tangent is 0.02 in the simulation. Electromagnetic analysis software: ADS (Advanced Design System, Keysight), is used to analyze the DC-bus pattern.

The two-ports S-parameter, which is used for the analysis in ADS, is converted to the Y-parameter. Then, the parasitic inductance and resistance are calculated from the Y-parameters. Figure 3 shows the model of the parasitic components between Port 1 and Port 2. The conversion formula from Y-parameter to the parasitic components is expressed as

$$L_{12} = \mathrm{Im}\left[\frac{1}{-\boldsymbol{Y}_{12}}\right] = \mathrm{Im}\left[\frac{1}{-\boldsymbol{Y}_{21}}\right] \quad \text{..... (1)},$$

$$R_{12} = \mathrm{Re}\left[\frac{1}{-\boldsymbol{Y}_{12}}\right] \quad \text{..... (2)},$$

where $\boldsymbol{Y}_{12}$, $\boldsymbol{Y}_{21}$ is the Y-parameters.

In order to confirm of the accuracy of the electromagnetic analysis result, the parasitic conponents is measured in the test board. The vector network analyzer (E5061B, Keysight) is used to measure parasitic components. The shunt-through method, which is able to measure impedance in milliohm, is used to measure the tiny parasitic components. Figure 4 shows the PCB measurement. For the measurement of parasitic parameters on DC bus, two probes is connected to Port 2 in parallel, and the jig shorts Port 1. In order to compensate the effect in impedance of the jig, the impedance of the jig is subtracted from the measurement impedance of the DC bus. Figure 5 shows the measurement result of the parasitic parameters on the jig.

Figure 6 shows the analysis and measurement result of the DC-bus pattern. The parasitic inductance of the analysis is 54.5 nH and the measurement is 52.5 nH at 6.78 MHz. The parasitic resistance of the analysis is 93 mΩ , and the measurement is 82 mΩ at 6.78 MHz. The error rate of the parasitic inductance is 3.8% and parasitic resistance is 13%. The parasitic inductance and resistance measured by the experiment show good agreement with the simulation. Thus, the accuracy of the analysis result is confirmed. Therefore, the analysis result is able to be used to evaluate the effect of parasitic parameters in the PCB and design of the circuits such as snubber circuit parameters.

III. Simulation and Experiment of the Surge Voltage

In order to evaluate the effect on the surge voltage due to the parasitic parameters, the analysis result of the PCB pattern, which includes parasitic parameters, is used in the time domain simulation. The Spice model of the GaN-transistor is used in the simulation. Table 2 shows the parameters of the GaN-transistor model. The other circuit components are the ideal model.

Figure 7 shows the drain-source voltage of FET1 with experiment and simulation. For the comparison of the effect of the parasitic parameters, the simulation with an ideal DC-bus pattern, which has no parasitic inductance, is also simulated. The surge voltage in the drain-source occurs in the simulated waveform with the results of the analysis of the PCB. On the other hand, the surge voltage does not occur in the waveform without analyzed board data. The amplitude of the surge voltage is 53.4 V in the simulation, and the experimental result in the same condition with the simulation is 32.0 V. The error rate of the surge voltage amplitude is

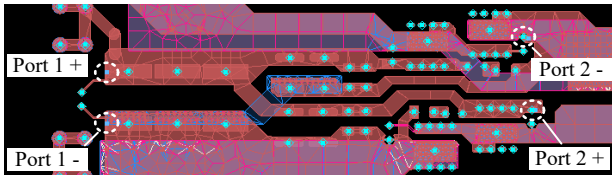


Fig. 2. Layout of DC-bus.

Table 1. PCB layer parameter.

Layer	Material	Thickness
Dielectric	Air	–
Top layer	Copper	0.040 mm
Dielectric	FR4	0.1 mm
2nd layer	Copper	0.035 mm
Dielectric	FR4	0.2 mm
3rd layer	Copper	0.035 mm
Dielectric	FR4	0.1 mm
Bottom layer	Copper	0.04 mm
Dielectric	Air	–

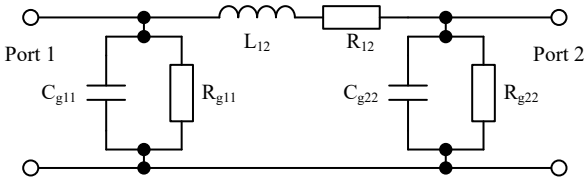


Fig. 3. Parasitic-parameter model.

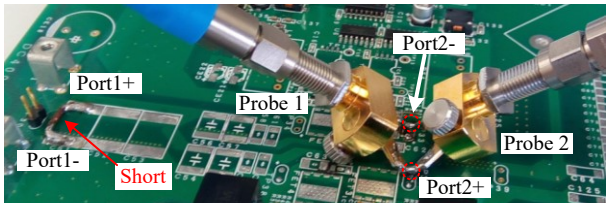
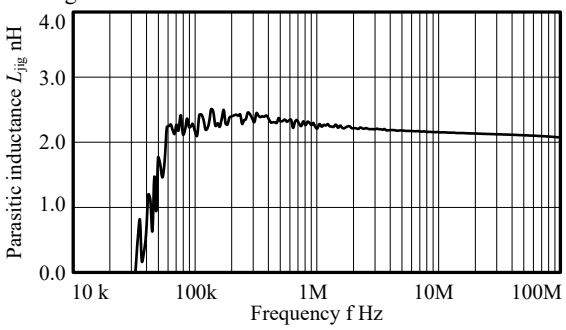
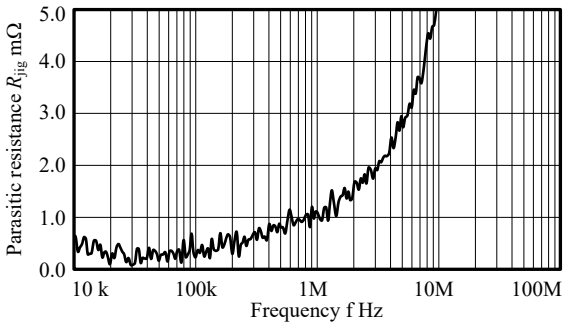


Fig. 4. Measurement of the DC-bus line on PCB.



(a) Inductance of jig.



(b) Resistance of jig.

Fig. 5 Parasitic-parameter of jig.

66.9%. The resonant frequency of the surge voltage in the experiment shows good agreement with the simulation in the first period. However, the frequency and decay of the oscillation of surge voltage do not match after the second period.

The difference in the waveforms is caused by employing ideal components in the simulation. In particular, the effect of ESR (equivalent series resistance) and ERL (equivalent series inductance) in the capacitor should not be ignored in megahertz switching circuits.

In order to simulate the waveform more accurately, parasitic parameters, such as ESR and ESL, should be considered. Hence, the parasitic parameters of passive components are measured using the vector network analyzer. Table 3 shows the measured value of the passive components and reference value. The capacitance C_{f1} cannot be measured by the test fixture for SMD due to the size, so only the reference value is shown. The measured value of the passive components is modeled and used in the following simulation.

Figure 8 shows the simulated waveform with the passive components model. The surge voltage amplitude is almost the same compared to the ideal model waveform, and the error of the ringing period remains. However, the decay of the surge voltage, especially the end of the ringing, shows more good agreement by employing passive components model based on the measurement.

IV. Snubber Circuit Parameter and Surge Voltage

The surge voltage is simulated accurately by employing the model of passive components. It is possible to consider methods to suppress the surge voltage at the circuit design phase.

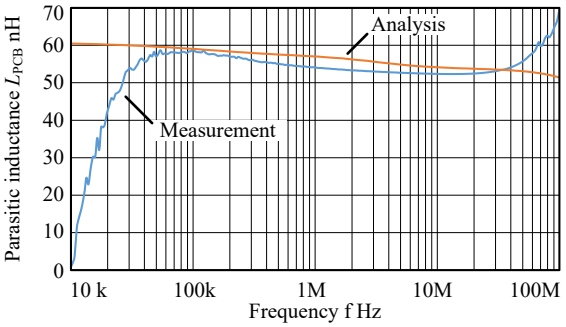
As the first step of the design of snubber circuit parameters, the snubber capacitance C_{f4} and the resistance R_{f4} is changed to investigate the effect to the amplitude of the surge voltage in the simulation. Snubber capacitance C_{f4} is changed from the capacitance as same as the output capacitance C_{oss} of the devices. The capacitance of 0 pF(without capacitor), 100 pF (half of the C_{oss}), 200 pF(the same value to the C_{oss}), and 400 pF (two times of the C_{oss}) is selected for the simulation.

Figure 9 shows the surge voltage rate of the drain-source. The surge voltage rate is expressed as

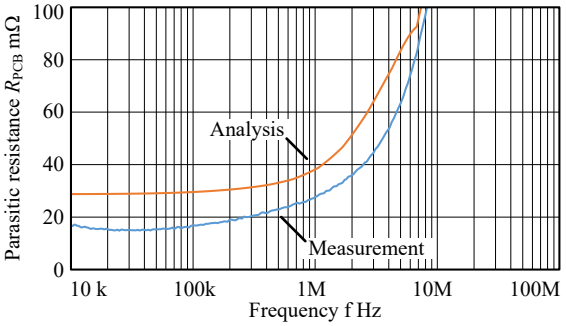
$$Surge\_voltage\_rate = \frac{v_{surge\_max} - V_{DC}}{V_{DC}} \times 100 \quad \text{..... (3).}$$

The surge voltage rate, which is evaluated with passive components models, is more accurate in comparison with the result without the models of the passive components. The error is 16.4% between simulated surge voltage rate with the passive components models, and experimental result at a capacitance C_{f4} of 100 pF.

However, the difference in the surge voltage rate is still high when the snubber capacitance C_{f4} is 0 pF and 400 pF. Because the errors, such as the measurement or the modeling error of the passive components, the models error of the GaN-transistor, or the error of the analysis result of the PCB, still remain.



(a) Parasitic inductance



(b) Parasitic resistance

Fig. 6. Parasitic-parameter.

Table 2. Parameter of device model.

Drain side inductance	L_d	1.5 nH
Source side inductance	L_s	1.0 nH
Drain side resistance	R_d	40 mΩ
Source side resistance	R_s	8.5 mΩ
Output capacitance	C_{oss}	200 pF (at. 6.78MHz)

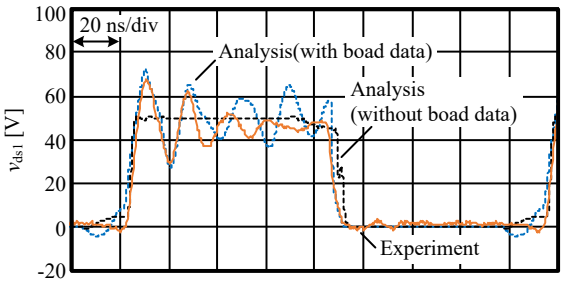


Fig. 7. Analyzed and measured v_{ds1} waveform.

Table 3. Parameter of the passive components.

	Reference			Measurement		
components	L	C	R	L	C	R
C_{f1} (B58031I5105M062)	3 nH	1 uF	12 mΩ	-	-	-
C_{f2} (C5750X7T2J474M250KE)		0.47 uF	11 mΩ	6.3 nH	496 nF	195 mΩ
C_{f3} (C3216C0G2J471J085AA)	1.2 nH	470 pF	102 mΩ	4.4 nH	456 pF	269 mΩ
C_{f4} (C3216C0G2J101J060AA)	1.2 nH	100 pF	171 mΩ	7.0 nH	98 pF	-
Rf (RC1206FR-071RL)	-	-	1Ω	4.9 nH	-	790 mΩ

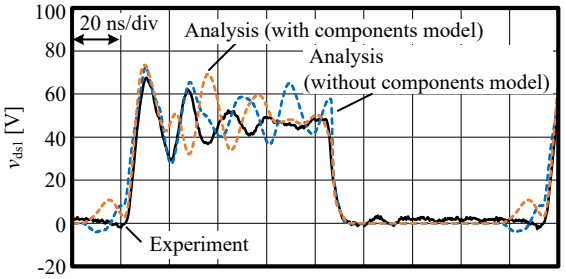


Fig. 8. Analyzed and measured v_{ds1} waveform with passive components model.

V. CONCLUSION

This paper presented the surge voltage simulation using the analysis result of the PCB pattern. The parasitic parameters on the PCB pattern are analyzed accurately using electromagnetic analysis. Comparing to the measurement result, the error rate of the analyzed parasitic inductance is only 3.8% at 6.78MHz.

The surge voltage is simulated accurately by using the analyzed PCB pattern and passive components model, which is based on the measurements. The maximum surge voltage and the decay of the ringing show good agreements between analysis and experiment, comparing to the case without passive components model. However, the error of the ringing period still remains.

The surge voltage with changing the snubber capacitor is evaluated in order to make the relationship between the surge voltage and the snubber circuit parameters as the first step of the parameter design by using simulation. The maximum surge voltage value with changing the snubber capacitor is investigated.

In the future work, the error between the measurement and analysis will be compensated for more accurate simulation.

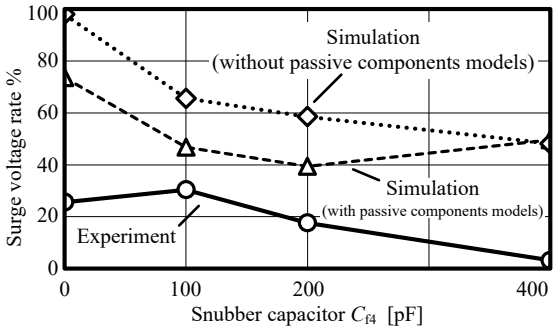


Fig. 9. Surge voltage rate.

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